Sun™ StorEdge™ A7000 External Interrupt and Clock Cable Diagnostic Reference Manual

THE NETWORK IS THE COMPUTER™

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Part No. 805-6662-10
October 1998, Revision A

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Preface

Sun StorEdge A7000 External Interrupt and Clock Cable Diagnostic Reference Manual is specific to the Extended Diagnostic provided for testing the external interrupt and clock cables. This manual contains the following information:

- Cable connections
- Program initialization procedures
- Test descriptions
- Descriptions of messages produced by this program

How This Book Is Organized

Chapter 1 “Diagnostic Overview” describes the Extended Diagnostic used for testing the external interrupts and clock cables. This chapter also describes the cable connections.

Chapter 2 “Program Initialization” describes the initialization options provided when running this diagnostic in interactive mode.

Chapter 3 “Program Tests” describes the individual diagnostic tests.

Chapter 4 “Program Messages” describes the messages produced by the diagnostic during program execution.

Typographic Conventions

TABLE P-1 Typographic Conventions

Typeface or Symbol	Meaning	Examples
`AaBbCc123`	The names of commands, files, and directories; on-screen computer output.	`Do you need help? Enter Y or N (CR)`
`AaBbCc123`	What you type, when contrasted with on-screen computer output.	`Enable milestone messages = N ;[cr,?,^,Y,N]?Y`
AaBbCc123	Book titles, new words or terms, words to be emphasized. Variable expressions; replaced with a real name or value.	Read Chapter 2 in the *Sun StorEdge A7000 ROM Monitor Reference Manual.* `slot n:Loading extended image xintdiag`
`[ ]`	In system output examples, brackets indicate optional values. If several values are placed inside brackets, any or none of them can be displayed. Brackets are also used in system prompts to enclose the response choices.	In the following example, displaying the slot number is optional: `[Slot` *`n`*`:]`

Related Documentation

TABLE P-2 Related Documentation

Type	Title
User interface	*Sun StorEdge A7000 ROM Monitor Reference Manual*
Diagnostic reference	*Sun StorEdge A7000 Diagnostics Reference Manual*

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CHAPTER 1

Diagnostic Overview

Introduction

The External Interrupt and Clock Cable Diagnostic is an Extended Diagnostic used to verify the functionality of external interrupt and clock cables. This program performs the following functions:

- Verifies the ability to generate and receive external interrupts.
- Checks for shorts and opens in external interrupt cabling.
- Verifies the functionality of external clocks.
- Checks for shorts and opens in external clock cabling.
- Provides scope loops for troubleshooting external interrupt and clock cable connections.

This is a disk based diagnostic normally executed with individual ROM Monitor commands. Refer to the *Sun StorEdge A7000 Diagnostics Reference Manual* for Extended Diagnostic commands and execution procedures.

Cable Connections

External interrupt and clock test cables are coaxial cables connected to the I/O Panel on the back of the system cabinet. Descriptions of the I/O Panel and the external interrupt and clock connections are supplied in the *Sun StorEdge A7000 Service Guide.*

External Interrupt Cables

Up to eight external interrupt cables are installed to connect the interrupt acknowledge and request signals associated with the external interrupt to be tested. The cable part number is 530-2607. Connect the signals by installing the cable between the correct J connectors as follows:

External Interrupt	Source	Destination
0	J9 (XIACK0)	J1 (XIRQ0)
1	J10 (XIACK1)	J2 (XIRQ1)
2	J11 (XIACK2)	J3 (XIRQ2)
3	J12 (XIACK3)	J4 (XIRQ3)
4	J13 (XIACK4)	JS (XIRQ4)
5	J14 (XIACK5)	J6 (XIRQ5)
6	J15 (XIACK6)	J7 (XIRQ6)
7	J16 (XIACK7)	J8 (XIRQ7)

External Clock Cables

One or two external clock test cables are installed for testing external clocks. The cable part number is 530-2607. To enable testing an external clock cable, install the cable between the correct J connectors as follows:

External Clock	Source	Destination
0	J9 (XIACK0)	J19 (XCLK0)
1	J16 (XIACK7)	J21 (XCLK1)

Note – To test both an external clock and its related external interrupt during the same pass of the diagnostic, use cable part number 530-2607. Connect XIACK0 (J9) to XIRQ0 (J1) to XCLK0 (Jl9) for interrupt 0 and clock 0 testing. Connect XIACK7 (J16) to XIRQ7 (J8) to XCLK1 (J21) for interrupt 7 and clock 1 testing

CHAPTER 2

Program Initialization

Initialization Options

When running in interactive mode, the External Interrupt and Clock Cable Diagnostic provides initialization options for:

- Enabling and disabling milestone messages
- Enabling and disabling debug messages
- Enabling and disabling scope loops
- Checking a single external interrupt cable
- Checking a single external clock cable

Select the `Initialize Diag.` option from the Interactive Mode Options Menu to initialize the diagnostic. The interactive mode options are described in the *Sun StorEdge A7000 Diagnostics Reference Manual*.

Initialization Procedure

Once you select `Initialize Diag.` from the Interactive Mode Options Menu, the program displays a series of initialization prompts. The following responses are standard for all initialization prompts:

TABLE 2-1 Standard Prompt Responses

Response	Description
`cr`	Press the return key to select the default response displayed in the prompt.
`?`	Display help information.
`^`	Return to the Interactive Mode Options Menu.

1. The diagnostic first displays the following help information prompt:

```
Do you need help? Enter Y or N (CR)
```

   Enter `Y` to display a help message. Enter `N` or press the Return key to bypass displaying help information. The default response is `N`.

2. The program then displays:

```
Do you wish to enable milestones? = No ;[cr,?,^,Y,N]?
```

   Enter one of the following or a standard response:

Response	Description
`Y`	Enables displaying all milestone messages.
`N`	Inhibits displaying milestone messages.

3. The program displays:

```
Do you wish to enable debug messages? = No ;[cr,?,^,Y,N]?
```

Enter one of the following or a standard response:

Response	Description
Y	Enables displaying debug messages during diagnostic execution.
N	Inhibits displaying debug messages during diagnostic execution.

4. The program displays:

```
Do you wish to enable scope loops? = No ;[cr,?,^,Y,N]?
```

Enter one of the following or a standard response:

Response	Description
Y	Enables scope loops.
N	Inhibits scope loops.

Scope loops are useful for troubleshooting a specific cable connection. If scope loops are enabled, all messages except the test starting milestone message are disabled.

Note – After running the diagnostic with scope loops enabled, you must enter Control-C to exit the scope loops and return to the ROM>> prompt.

When using scope loops, enable only the interrupt or clock to which the scope is attached and use the interactive mode `t` option to select the test related to the cable connection under observation (Test 1 for an interrupt or Test 2 for a clock).

5. The program displays:

```
Do you wish to check for all external
interrupt cables? = Yes ;[cr,?,^,Y,N]?
```

Enter one of the following or a standard response:

Response	Description
Y	Enables testing all external interrupt cables.
N	Enables testing a single external interrupt cable.

If you entered Y, go to Step 6. If you entered N, the program displays:

```
Which external interrupt cable do you wish
to test? = 0 ;[cr,?,^,(0-7)]?
```

Enter the number of the external interrupt cable to be tested or enter one of the standard responses. Valid cable numbers are 0 through 7.

6. The program displays:

```
Do you wish to check for all external
clock cables? = Yes ;[cr,?,^,Y,N]?
```

Enter one of the following or a standard response:

Response	Description
Y	Enables testing all external clock cables.
N	Enables testing a single external clock cable.

If you entered Y, program initialization is complete. If you entered N, the program displays:

```
Which external clock cable do you wish
to test? = 0 ;[cr,?,^,(0-1)]?
```

Enter the number of the external clock cable to be tested or enter one of the standard responses. Valid cable numbers are 0 and 1.

Note – To run tests in interactive mode, use the a, e, or t option from the Interactive Mode Options Menu to select the desired tests. Then use the r option to start test execution. The interactive mode options are described in the *Sun StorEdge A7000 Diagnostics Reference Manual*.

If an invalid selection is entered at an initialization prompt, the diagnostic displays an Invalid Response message and redisplays the prompt.

CHAPTER 3

Program Tests

Test Summary

The External Interrupt and Clock Cable Diagnostic contains the following tests:

Test	Test Name
1	External Interrupts
2	External Clocks

Test 1 External Interrupts

This test verifies the external interrupt cables. The test is used to verify either a single external interrupt cable or all external interrupt cables. You select the level of testing during program initialization. Refer to Chapter 2 for a description of the initialization options.

Test 1 uses the external interrupt acknowledge signal line (XIACK0 through XIACK7) as the source of the external interrupt under test. The output from this signal is connected to the corresponding input signal line (XIRQ0 through XIRQ7). For example, XIACK7 is connected to XIRQ7. The test generates the XIACK output signal by writing to the corresponding ISTS register in the TS80. Refer to Chapter 1 for cabling information.

Test 2 External Clocks

This test verifies the external clock cables. The test is used to verify either a single external clock cable or all external clock cables. You select the level of testing during program initialization. Refer to Chapter 2 for a description of the initialization options.

The external interrupt acknowledge signals for interrupts 0 and 7 (XIACK0 and XIACK7) should be connected to the corresponding input signal lines (XIRQ0 and XIRQ7) and the external clock signal lines (XCLK0 and XCLK1) respectively. Refer to Chapter 1 for cabling information.

CHAPTER 4

Program Messages

Introduction

The following types of messages are associated with the External Interrupt and Clock Cable Diagnostic:

- Monitor
- Start
- Milestone
- Debug
- Pass and Error Count
- Error

Monitor Messages

Prior to starting test execution, the program checks the ROM Monitor revision level. If the existing version of the ROM Monitor is not at the expected level, the program displays:

```
*** WARNING: ROM Monitor Version should be 2.56 or higher.
```

Start Messages

Once loaded, the External Interrupt and Clock Cable Diagnostic displays its start message on the operator's console in the following format:

```
Extended XINT Diagnostic
Diagnostic Revision: y.y
[Copyright year Sun Microsystems, Inc.]
```

Variable	Description
y.y	Specifies the current revision of the diagnostic.
year	Specifies the year the program was copyrighted.

The diagnostic then displays the Interactive Mode Options Menu.

Milestone Messages

As each test starts execution, the diagnostic displays a test milestone message:

```
Running Test tt: testname
```

Variable	Description
tt	Specifies the test number.
testname	Specifies the name of the test.

If you enabled milestones messages during program initialization, the program also displays the following milestone messages during program execution:

- As each external interrupt is tested, the program displays:

```
XIACKx is connected to XIRQx
```

Variable	Description
x	Specifies the number (0 through 7) associated with the interrupt acknowledge and request signals under test.

- As each external clock is tested, the program displays:

```
Test for clock n
```

Variable	Description
n	Specifies the number (0 or 1) associated with the external clock signal under test.

If the clock test is successful, the program appends `...PASSED!` to the milestone message. If the clock test fails, the program appends `...FAILED!` to the milestone message and displays an error message. If an error is detected and the `Stop on Error` option is enabled, this milestone message is not displayed.

Debug Messages

Debug messages provide detailed test information during the execution of the External Interrupt and Clock Cable Diagnostic. You enable or disable displaying debug messages during program initialization. Refer to Chapter 2 for a description of the initialization options.

Test 1 Debug Messages

During the execution of the External Interrupts test, the program displays the status of all interrupts in the following format if you enabled debug messages during program initialization:

```
int_count[21]=c int_active=a int_rcvd=r Timer 5

int_count[23]=c int_active=a int_rcvd=r XIRQ0
int_count[24]=c int_active=a int_rcvd=r XIRQ1
int_count[25]=c int_active=a int_rcvd=r XIRQ2
int_count[26]=c int_active=a int_rcvd=r XIRQ3
int_count[27]=c int_active=a int_rcvd=r XIRQ4
int_count[28]=c int_active=a int_rcvd=r XIRQ5
int_count[29]=c int_active=a int_rcvd=r XIRQ6
int_count[30]=c int_active=a int_rcvd=r XIRQ7
```

The first line of the display is associated with the local timer used to establish the test timeout value and the other lines are associated with the individual external interrupt request signals.

Variable	Description
c	Specifies the number of interrupts.
a	Specifies 1 if the interrupt is active or 0 if the interrupt is not active.
r	Specifies 1 if an interrupt has been received or 0 if no interrupt was received.

The program then displays the contents of the TS80 interrupt registers in the following format:

```
GIE=0xgie IEL=0xiel MASK=0xmask ISTS=0xists
IPEND=0xipend OPEND=0xopend OVERRUN=0xover
```

Variable	Description
gie	Specifies the contents of the Global Interrupt Enable register.
iel	Specifies the contents of the Interrupt on Edge not Level register.
mask	Specifies the contents of the Symmetric Interrupt Unmask register.
ists	Specifies the contents of the Interrupt Status register.

Variable	Description
ipend	Specifies the contents of the Symmetric Interrupt Pending register.
opend	Specifies the contents of the Symmetric Overrun Pending register.
over	Specifies the contents of the Interrupt Overrun register.

Both the interrupt status and interrupt register displays are repeated before the interrupt under test is generated, after the interrupt is received, and after the timeout timer interrupt occurs.

The program then displays one of the following messages:

- This message is displayed before the interrupt is generated:

```
Just Before ISTS is written
```

This message is displayed after the interrupt is received:

```
XIACKn is connected to XIRQn
```

Variable	Description
n	Specifies the number associated with the external interrupt acknowledge and request signals.

- The following message is displayed after the timeout timer interrupt is received:

```
 Timer interrupt
```

Test 2 Debug Messages

If you enabled debug messages during program initialization, the External Clocks test displays the contents of the TS80 interrupt registers in the following format:

```
GIE=0xgie IEL=0xiel MASK=0xmask ISTS=0xists
IPEND=0xipend OPEND=0xopend OVERRUN=0xover
MSTC=0xmaster LTSTC=0xlocal LTR0=timer0 LTR1=timer1
```

Variable	Description
gie	Specifies the contents of the Global Interrupt Enable register.
iel	Specifies the contents of the Interrupt on Edge not Level register.
mask	Specifies the contents of the Symmetric Interrupt Unmask register.
ists	Specifies the contents of the Interrupt Status register.
ipend	Specifies the contents of the Symmetric Interrupt Pending register.
opend	Specifies the contents of the Symmetric Overrun Pending register.
over	Specifies the contents of the Interrupt Overrun register.
master	Specifies the contents of the Master Status and Control register.
local	Specifies the contents of the Local Timer Status and Control register.
timer0	Specifies the contents of the Local Timer 0 Read register.
timer1	Specifies the contents of the Local Timer l Read register.

The program then displays the following message and starts testing the clock:

```
Start of testing for Clock n
```

Variable	Description
n	Specifies the external clock under test.

After the clock is tested, the program redisplays the TS80 interrupt registers and displays the following message:

```
Clock n done
```

Variable	Description
n	Specifies the external clock under test.

The test then displays the `...PASSED` or `...FAILED` milestone message.

Pass and Error Count Messages

The following message is displayed after each pass of the diagnostic is completed:

```
Pass Count: pppppppp
```

Variable	Description
pppppppp	Specifies the number of program passes completed.

If an error occurs, the program displays the number of errors at the end of each pass in the following format:

```
Pass Count: pppppppp, Error Count: eeeeeeee
```

Variable	Description
pppppppp	Specifies the number of program passes completed.
eeeeeeee	Specifies the number of errors encountered since the program started execution.

Error Messages

If an error is detected during testing, the diagnostic displays an error header in the following format:

```
Extended XINT Diagnostic Failed        Time:hh:mm:ss
```

Variable	Description
hh:mm:ss	Specifies the system elapsed time when the error occurred.

The program then displays an additional error message in one of the following formats:

```
Error: Slot 0: CPU n: XINT: error message

Error: Slot 0: CPU n: XINT: Test t: test name
                error message
```

Variable	Description
n	Specifies the number of the CPU running the diagnostic.
t	Specifies the number of the failing test. If an error occurs during the initialization sequence, the test number is reported as 0.
test name	Specifies the name of the failing test.
error message	Specifies an Interrupt Error message in the first format and either a Timeout or Clock Error message in the second format.

Interrupt Error Messages

If an unexpected interrupt occurs, the diagnostic displays:

```
Spurious interrupt on level x
```

Variable	Description
x	Specifies the failing interrupt level.

If an external interrupt is received from the wrong input signal, the program displays:

```
XIACKx is connected to XIRQy ---> ERROR
```

Variable	Description
x	Specifies the interrupt under test.
y	Specifies the failing interrupt.

This error may be caused by a short in the cable.

Timeout Error Messages

If a timeout occurs while testing an external interrupt during Test 1, the program displays:

```
Timeout occurred while testing XIACKx to XIRQx connection
```

Variable	Description
x	Specifies the interrupt level under test.

This failure indicates that no connection exists between the interrupt acknowledge and request signals and may be caused by an open in the cable.

If the external clock does not timeout when expected, the program displays:

```
LTSTC does not report timeout for timer n
```

Variable	Description
n	Specifies the external clock under test.

Clock Error Messages

If the external clock under test fails to count correctly, the program displays:

```
External Clock n
Expected clock ticks = ee
Actual clock ticks = aa
```

Variable	Description
n	Specifies the external clock under test.
ee	Specifies the expected number of clock ticks.
aa	Specifies the actual number of clock ticks.