Netra™ CP2160 CompactPCI Board Installation and Technical Reference Manual

Sun Microsystems, Inc.
www.sun.com

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Safety Agency Compliance Statements

Read this section before beginning any procedure. The following text provides safety precautions to follow when installing a Sun Microsystems product.

Safety Precautions

For your protection, observe the following safety precautions when setting up your equipment:

- Follow all cautions and instructions marked on the equipment.
- Ensure that the voltage and frequency of your power source match the voltage and frequency inscribed on the equipment's electrical rating label.
- Never push objects of any kind through openings in the equipment. Dangerous voltages may be present. Conductive foreign objects could produce a short circuit that could cause fire, electric shock, or damage to your equipment.

Symbols

The following symbols may appear in this book:

Caution – There is a risk of personal injury and equipment damage. Follow the instructions.

Caution – Hot surface. Avoid contact. Surfaces are hot and may cause personal injury if touched.

Caution – Hazardous voltages are present. To reduce the risk of electric shock and danger to personal health, follow the instructions.

On – Applies AC power to the system.

Depending on the type of power switch your device has, one of the following symbols may be used:

Off – Removes AC power from the system.

Standby – The On/Standby switch is in the standby position.

Modifications to Equipment

Do not make mechanical or electrical modifications to the equipment. Sun Microsystems is not responsible for regulatory compliance of a modified Sun product.

Placement of a Sun Product

Caution – Do not block or cover the openings of your Sun product. Never place a Sun product near a radiator or heat register. Failure to follow these guidelines can cause overheating and affect the reliability of your Sun product.

Noise Level

In compliance with the requirements defined in DIN 45635 Part 1000, the workplace-dependent noise level of this product is less than 70Db(A).

SELV Compliance

Safety status of I/O connections comply to SELV requirements.

Power Cord Connection

Caution – Sun products are designed to work with power systems having a grounded neutral (grounded return for DC-powered products). To reduce the risk of electric shock, do not plug Sun products into any other type of power system. Contact your facilities manager or a qualified electrician if you are not sure what type of power is supplied to your building.

Caution – Not all power cords have the same current ratings. Household extension cords do not have overload protection and are not meant for use with computer systems. Do not use household extension cords with your Sun product.

The following caution applies only to devices with a Standby power switch:

Caution – The power switch of this product functions as a standby type device only. The power cord serves as the primary disconnect device for the system. Be sure to plug the power cord into a grounded power outlet that is nearby the system and is readily accessible. Do not connect the power cord when the power supply has been removed from the system chassis.

The following caution applies only to devices with multiple power cords:

Caution – For products with multiple power cords, all power cords must be disconnected to completely remove power from the system.

Battery Warning

Caution – There is danger of explosion if batteries are mishandled or incorrectly replaced. On systems with replaceable batteries, replace only with the same manufacturer and type or equivalent type recommended by the manufacturer per the instructions provided in the product service manual. Do not disassemble batteries or attempt to recharge them outside the system. Do not dispose of batteries in fire. Dispose of batteries properly in accordance with the manufacturer's instructions and local regulations. Note that on Sun CPU boards, there is a lithium battery molded into the real-time clock. These batteries are not customer replaceable parts.

System Unit Cover

You must remove the cover of your Sun computer system unit to add cards, memory, or internal storage devices. Be sure to replace the cover before powering on your computer system.

Caution – Do not operate Sun products without the cover in place. Failure to take this precaution may result in personal injury and system damage.

Rack System Warning

The following warnings apply to Racks and Rack Mounted systems.

Caution – For safety, equipment should always be loaded from the bottom up. That is, install the equipment that will be mounted in the lowest part of the rack first, then the next higher systems, etc.

Caution – To prevent the rack from tipping during equipment installation, the anti-tilt bar on the rack must be deployed.

Laser Compliance Notice

Sun products that use laser technology comply with Class 1 laser requirements.

Class 1 Laser Product
Luokan 1 Laserlaite
Klasse 1 Laser Apparat
Laser Klasse 1

CD and DVD Devices

The following caution applies to CD, DVD, and other optical devices.

Caution – Use of controls, adjustments, or the performance of procedures other than those specified herein may result in hazardous radiation exposure.

Nordic Lithium Battery Cautions

Norge

Advarsel – Litiumbatteri — Eksplosjonsfare.Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

Sverige

Varning – Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

Danmark

Advarsel! – Litiumbatteri — Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

Suomi

Varoitus – Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

Regulatory Compliance Statements

Your Sun product is marked to indicate its compliance class:

- Federal Communications Commission (FCC) — USA
- Industry Canada Equipment Standard for Digital Equipment (ICES-003) — Canada
- Voluntary Control Council for Interference (VCCI) — Japan
- Bureau of Standards Metrology and Inspection (BSMI) — Taiwan

Please read the appropriate section that corresponds to the marking on your Sun product before attempting to install the product.

FCC Class A Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy, and if it is not installed and used in accordance with the instruction manual, it may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Modifications: Any modifications made to this device that are not approved by Sun Microsystems, Inc. may void the authority granted to the user by the FCC to operate this equipment.

FCC Class B Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

Modifications: Any modifications made to this device that are not approved by Sun Microsystems, Inc. may void the authority granted to the user by the FCC to operate this equipment.

Shielded Cables

Hardwire connections between the workstations and peripherals must be made using shielded cables to comply with radio frequency emission limits. Hardwire Network connections can be made using unshielded twisted-pair (UTP) cables.

ICES-003 Class A Notice - Avis NMB-003, Classe A

This Class A digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.

ICES-003 Class B Notice - Avis NMB-003, Classe B

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

VCCI 基準について

クラス A VCCI 基準について

クラス A VCCI の表示があるワークステーションおよびオプション製品は、クラス A 情報技術装置です。これらの製品には、下記の項目が該当します。

この装置は、情報処理装置等電波障害自主規制協議会 (VCCI) の基準に基づくクラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

クラス B VCCI 基準について

クラス B VCCI の表示  があるワークステーションおよびオプション製品は、クラス B 情報技術装置です。これらの製品には、下記の項目が該当します。

この装置は、情報処理装置等電波障害自主規制協議会 (VCCI) の基準に基づくクラス B 情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。取扱説明書に従って正しい取り扱いをしてください。

BSMI Class A Notice

The following statement is applicable to products shipped to Taiwan and marked as Class A on the product compliance label.

警告使用者：
這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻 干擾，在這種情況下，使用者 會被要求採取某些適當的對策。

Declaration of Conformity

Compliance Model Number: CP2160F
Product Family Name: Netra CP2160 (Universal CompactPCI Board)

EMC

USA—FCC Class B

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This equipment may not cause harmful interference.
2. This equipment must accept any interference that may cause undesired operation.

European Union

This equipment complies with the following requirements of the EMC Directive 89/336/EEC:

As Telecommunication Network Equipment (TNE) in Both Telecom and Other Than Telecom Centers per (as applicable)*:*

EN300-386 V.1.3.1 (09-2001) Required Limits:

EN55022/CISPR22	Class B
EN61000-3-2	Pass
EN61000-3-3	Pass
EN61000-4-2	6 kV (Direct), 8 kV (Air)
EN61000-4-3	3 V/m 80-1000MHz, 10V/m 800-960 MHz and 1400-2000 MHz
EN61000-4-4	1 kV AC and DC Power Lines, 0.5 kV Signal Lines
EN61000-4-5	2 kV AC Line-Gnd, 1 kV AC Line-Line and Outdoor Signal Lines, 0.5 kV Indoor Signal Lines > 10m.
EN61000-4-6	3 V
EN61000-4-11	Pass

As Information Technology Equipment (ITE) Class B per (as applicable)*:*

EN55022:1998/CISPR22:1997 Class B

EN55024:1998 Required Limits:

EN61000-4-2	4 kV (Direct), 8 kV (Air)
EN61000-4-3	3 V/m
EN61000-4-4	1 kV AC Power Lines, 0.5 kV Signal Lines and DC Power Lines
EN61000-4-5	1 kV AC Line-Line and Outdoor Signal Lines, 2kV AC Line-Gnd, 0.5 kV DC Power Lines
EN61000-4-6	3 V
EN61000-4-8	1 A/m
EN61000-4-11	Pass
EN61000-3-2	Pass
EN61000-3-3	Pass

Safety

This equipment complies with the following requirements of the Low Voltage Directive 73/23/EEC:

EC Type Examination Certificates:

UL 60950, 3rd Edition, CSA C22.2 No. 60950-00 File: E138989 Vol. 37 Sec. 1

Supplementary Information: This product was tested and complies with all the requirements for the CE Mark.

/S/
DATE

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Declaration of Conformity

Compliance Model Number: CP2160R
Product Family Name: Netra CP2060-TRN Universal CompactPCI Board

EMC

USA—FCC Class B

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This equipment may not cause harmful interference.
2. This equipment must accept any interference that may cause undesired operation.

European Union

This equipment complies with the following requirements of the EMC Directive 89/336/EEC:

As Telecommunication Network Equipment (TNE) in Both Telecom and Other Than Telecom Centers per (as applicable)*:*

EN300-386 V.1.3.1 (09-2001) Required Limits:

EN55022/CISPR22	Class B
EN61000-3-2	Pass
EN61000-3-3	Pass
EN61000-4-2	6 kV (Direct), 8 kV (Air)
EN61000-4-3	3 V/m 80-1000 MHz, 10 V/m 800-960 MHz and 1400-2000 MHz
EN61000-4-4	1 kV AC and DC Power Lines, 0.5 kV Signal Lines
EN61000-4-5	2 kV AC Line-Gnd, 1 kV AC Line-Line and Outdoor Signal Lines, 0.5 kV Indoor Signal Lines > 10m.
EN61000-4-6	3 V
EN61000-4-11	Pass

As Information Technology Equipment (ITE) Class B per (as applicable)*:*

EN55022:1998/CISPR22:1997 Class B

EN55024:1998 Required Limits:

EN61000-4-2	4 kV (Direct), 8 kV (Air)
EN61000-4-3	3 V/m
EN61000-4-4	1 kV AC Power Lines, 0.5 kV Signal Lines and DC Power Lines
EN61000-4-5	1 kV AC Line-Line and Outdoor Signal Lines, 2kV AC Line-Gnd, 0.5 kV DC Power Lines
EN61000-4-6	3 V
EN61000-4-8	1 A/m
EN61000-4-11	Pass
EN61000-3-2	Pass
EN61000-3-3	Pass

Safety

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Preface

The *Netra CP2160 CompactPCI Board Installation and Technical Reference Manual* describes the hardware specifications, function and physical properties of the Netra™ CP2160 board with a description of connector pinouts, boot sequence, diagnostics, and installation and removal procedures.

The *Netra CP2160 CompactPCI Board Installation and Technical Reference Manual* is written for customers, system integration engineers, field applications and service engineers, and others involved in the integration of these board into systems.

How This Book Is Organized

Chapter 1 provides an overview of the Netra CP2160 board.

Chapter 2 provides instructions on software configurations and hot swap.

Chapter 3 provides instructions on hardware installation.

Chapter 4 provides information on the Netra CP2160 system OpenBoot™ firmware and Power-on Self Test (POST).

Chapter 5 provides a description of the various blocks on the Netra CP2160 boards.

Appendix A provides information on the Netra CP2160 specifications.

Appendix B provides pinouts of the CompactPCI connectors on the Netra CP2160 and some othe rkey connectors on the boards.

Appendix C describes how to access the Solaris Sun FRU ID information for a Netra CP2160 board.

Appendix D provides a comprehensive list of references for the Netra CP2160 board.

The Glossary lists definitions of many of the special terms used in this publication.

Related Documentation

Related documentation is listed in Appendix D.

Using UNIX Commands

This document might not contain information on basic UNIX® commands and procedures such as shutting down the system, booting the system, and configuring devices.

See one or more of the following for this information:

- *Solaris Handbook for Sun Peripherals*
- AnswerBook2™ online documentation for the Solaris™ operating environment
- Other software documentation that you received with your system

Typographic Conventions

TABLE P-1

Typeface or Symbol	Meaning	Example
`AaBbCc123`	The names of commands, files, and directories; on-screen computer output	Edit your `.login` file. Use `ls -a` to list all files. `machine_name% You have mail.`

TABLE P-1

Typeface or Symbol	Meaning	Example
AaBbCc123	What you type, contrasted with on-screen computer output	`machine_name% su` `Password:`
AaBbCc123	Command-line placeholder: replace with a real name or value	To delete a file, type `rm` *filename*.
AaBbCc123	Book titles, new words or terms, or words to be emphasized	Read Chapter 6 in *User's Guide*. These are called *class* options. You *must* be root to do this.

Accessing Sun Documentation

You can view, print, or purchase a broad selection of Sun documentation, including localized versions, at:

`http://www.sun.com/documentation`

CHAPTER 1

Overview of the Netra CP2160 CompactPCI Board

The Netra CP2160 CompactPCI board is a crucial building block that network equipment providers (NEPs) and carriers can use when scaling and improving the availability of next-generation, carrier-grade systems. Based on industry standards, the Netra CP2160 board provides high performance and is easily customized for satellite processing. Powered by a 650 MHz UltraSPARC IIi processor, the board is also capable of host processing.

The Netra CP2160 board enables customers to mix and match third-party PCI mezzanine cards (PMCs), making it easier for them to tailor solutions to their specific application needs. The Netra CP2160 boardprovides PCI Industrial Computers Manufacturers' Group (PICMG) CompactPCI compliance (for details, see TABLE 1-1) and are NEBs Level 3 certified to meet the CompactPCI system requirements of the communications and service provider environments. An example of a typical Netra CP2160 board is illustrated in FIGURE 1-1.

This chapter contains the following sections:

1.1 Features of the Netra CP2160 CompactPCI Board

The Netra CP2160 board is a CompactPCI single-board computer designed for high-performance embedded, compute density applications. Powered by a 650 MHz UltraSPARC IIi processor, with full utilization of the PMC slots, the Netra CP2160 board has System Management Controller (SMC) capability that suppports hot-swap operations, system managment, and environmental monitoring. The Netra CP2160 board is an ideal platform for NEPs to use for a wide variety of Solaris applications.

An illustration of the board is shown in FIGURE 1-1. A summary of features of the Netra CP2160 board is given in TABLE 1-1.

TABLE 1-1 Feature Summary

Feature	Description
CPU	UltraSPARC IIi 650 MHz processor with internal L2 cache (2:2 mode, 512 Kbyte, 4-way set association)
Memory	• 1 GB on-board memory • 1 GB additional memory module is available
Power requirement	Estimated at 20W (typical) and 26W (maximum) at 650 MHz (excluding PMC power)
PICMG and PCI compliance	• PICMG 2.0 R3.0 CompactPCI bus specification for 33MHz PCI speed • PICMG 2.1 R2.0 Hot-Swap Specification • PICMG 2.9 R1.0 System Management Specification • PICMG 2.10 R1.0 Keying of CPCI boards and backplanes • PICMG 2.15 R1.0 PCI Telecom Mezzanine/Carrier Cards (PTMC) support • 64 bit, 33MHz, 5V bus interface [3.3V supported through alternate board stuffing]
Host-mode support	The board can function as a system host board with the Solaris 8 package
Satellite mode support	The board can function as a satellite board with the with Solaris 8 package
IPMI system management	Uses IPMI communications with Baseboard Management Controller (BMC); performs Advanced System Monitoring (ASM) on local board interface for example temperature sense, FRU ID, and control
Hot-swap support	Basic and Full hot-swap support as both a system and satellite board
Operating system	Solaris 8 operating environment, Release 2/02, or or subsequent compatible version

TABLE 1-1 Feature Summary

Feature	Description
Front I/O and connectors	• Two PMC slots • Two Ethernet ports (can only be used if rear ports are not used) • One serial port (can only be used if rear serial port COM A is not used)
Connectors on rear transition card (optional)*	• Two 10/100 Ethernet ports • Two serial ports • One USB port • One PCI Interface Module (PIM)
PMC I/O	Provision for adding up to two IHV supplied PMC expansion ports on front panel. PMC availability depends on the memory used on the board: • Two PMC slots are available with 1 GB on-board memory only. • One PMC slot is available when a single-size memory module is added to the board. • No PMC slots are available when a double-sized memory module is added to the board.
Backplane PMC I/O	One USB port; also provision for adding two independent hardware venfor (IHV)-supplied PIM I/O ports when used with transition card
Watchdog timer	Two-level watchdog timer
NVRAM	8 Kbyte of nonvolatile memory storage, which functions as SRAM for the battery-less board; no battery backup to TOD or memory
System flash	1 Mbyte on board
User flash	8 Mbyte on board
Building compliance	NEBS Level 3
Flash update	Supported from downloaded file

Note – When used as a system controller, the CP2160 board is Class A for EMI compliance. When used as a satellite card, the CP2160 board is Class B under the following conditions. For Class B EMI compliance of front access ports, use of shielded cables is required on all I/O ports. For Class B compliance of rear access ports, use of shielded cables is required on the serial I/O port and unshielded cables can be used on the Ethernet port. The shields for all shielded cables must be terminated on both ends.

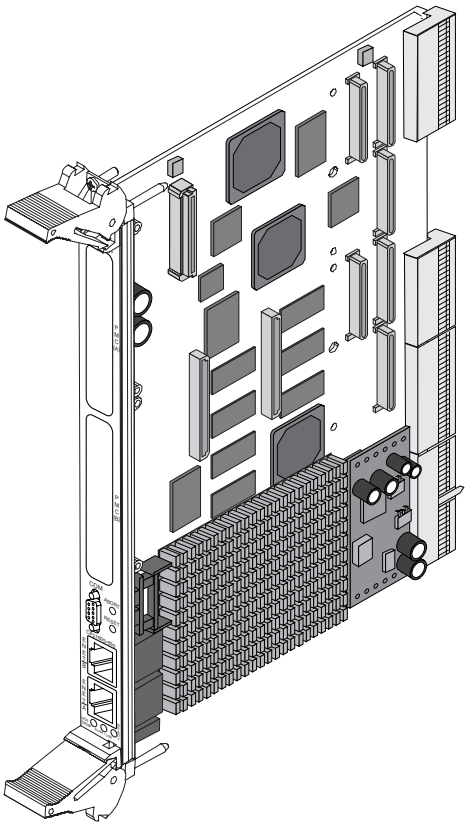

FIGURE 1-1 Netra CP2160 System Host Board or Satellite Board

1.2 Netra CP2160 System Configurations

The Netra CP2160 boards can be mounted in various enclosures, such as shown in FIGURE 1-2. The boards can be deployed in various electrical configurations to suit each end-user requirement. For example, the host board can be configured to boot from a network as a diskless client with either a front or rear network connection. Alternatively, industry-standard PMC and PIM hardware from Independent Hardware Vendors (IHVs) can be installed to provide local disk I/O, which may optionally be used as a boot path. The installation procedure is independent of the type of enclosure, whether a floor-mounting rack or a bench-top cabinet is used. The Netra CP2160 board has fixed on-board memory and additional memory can also be installed.

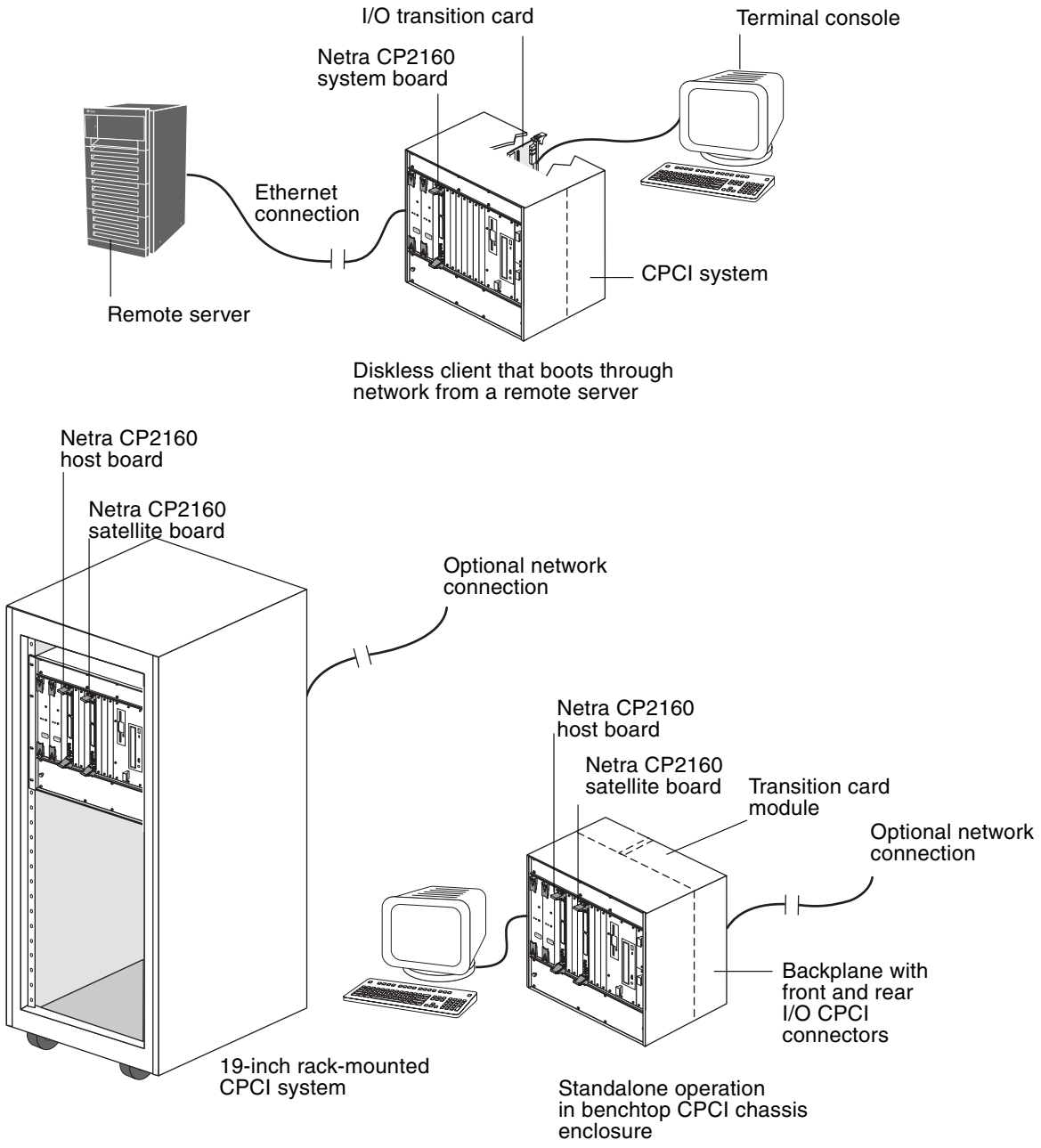

FIGURE 1-2 Examples of Netra CP2160 Board Mounting Configurations

1.2.1 System Host and Satellite Configurations

Systems that conform to CompactPCI specifications require differentiation of chassis board slots, depending upon the function of the board.

To function as a system host board, a Netra CP2160 board has connections that distribute PCI clocks and receive interrupts from peripherals. The board must be installed in a system slot in the CompactPCI segment, because only the system chassis slots have backplane wiring with the full set of connections required to enable the system host board function. The Netra CP2160 board can control CompactPCI peripheral hardware if it is installed as a system controller in a PICMG system slot, because it detects a special enable signal (SYS-EN signal) in this slot. A system host slot is marked with an open triangle legend, as specified in *CompactPCI Specification*, PICMG 2.0 R3.0 (see Appendix C for reference details).

The Netra CP2160 board can be placed in one of the remaining (nonsystem controller) slots if the user wants to use it as a functional satellite board.

For a definition of the system host board and satellite board see the *Glossary* in this book.

1.2.2 PMC and PIM Modules

The Netra CP2160 board has two Ethernet ports and one serial port on the front panel. The addition of IHV-built PMC modules provide additional I/O to the front panels. PMC modules decode their custom I/O from the Netra board's on-board PCI bus B signals. See Section 5.4.4, "PMC and PIM Interface" on page 5-16 for further information.

1.2.3 Transition Card

The optional XCP2060-TRN transition card from Sun Microsystems installs into the rear of the CompactPCI enclosure, opposite the Netra CP2160 board (see FIGURE 1-3). The transition card connects with the host CompactPCI P3 and P5 connectors through the backplane pins and carries two serial ports and a USB port out to its rear-panel flange.

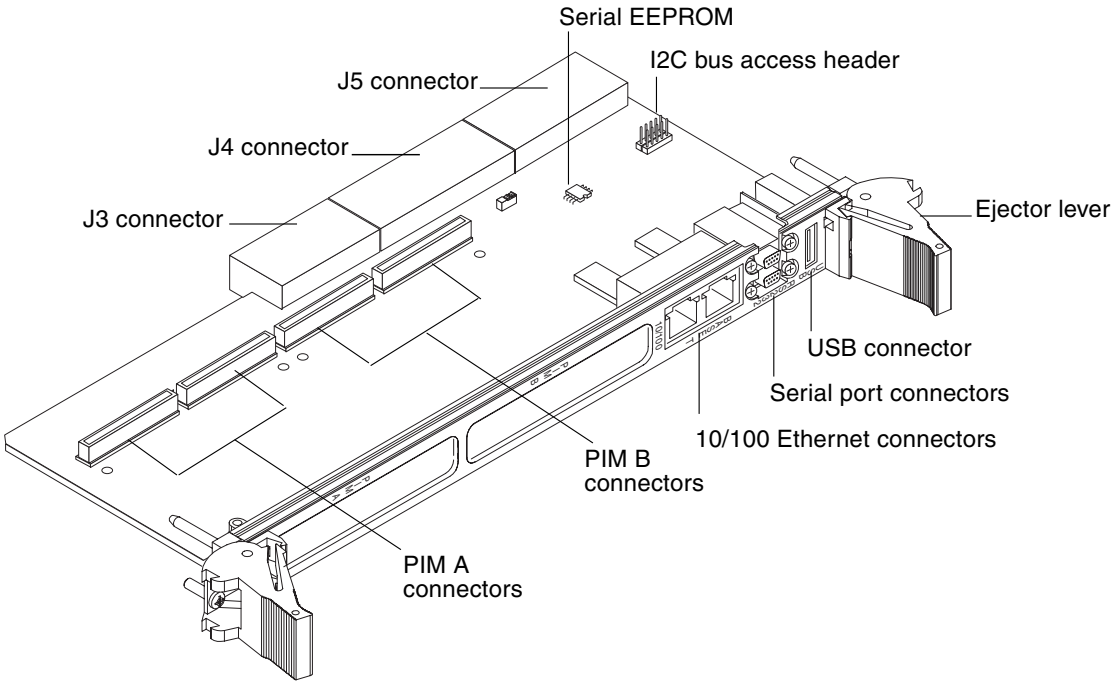

FIGURE 1-3 XCP2060-TRN Transition Card with Location of On-Board Components

FIGURE 1-4 and FIGURE 1-5 show the physical relationship between host boards, transition cards, and the backplane in a typical system.

Note – For Class B EMI compliance: When the transition card is used with the Netra CP2160 board, shielded cables are required for serial and USB I/O ports and unshielded cable can be used on Ethernet ports. The shields for all shielded cables must be terminated on both ends.

The transition card can also be fitted with IHV PCI Interface Modules (PIMs) which are configured to bring I/O channels to the unit rear panel. A PIM hardware kit includes a card for the PMC slot and a card for the PIM slot on the transition card. A PIM is a rear-panel extension added to a PMC module. When the PIM I/O is configured, the front PMC I/O output is not accessible.

The customer can order the XCP2060-TRN transition card, build a custom card, or buy from an Independent Hardware Vendor (IHV). A minimal set of I/O must provide for a boot path for the host board and for a path for console I/O to deliver commands and to read board and system status.

Possible boot and console configurations are described in TABLE 1-2. Sun Microsystems provides the host boards and a compatible XCP2060-TRN transition card for Netra CP2160 boards. This transition card brings out 10/100 Ethernet RJ45 ports from the host to the rear of the system, which can be used to accomplish network boot as a diskless client. The other configurations require IHV hardware.

TABLE 1-2 Netra CP2160 I/O Board Configurations

I/O	Hardware Required	Description
Ethernet*	XCP2060 I/O transition card—supplied as an option for rear access; Ethernet also available on front panel with no extra hardware required	Default boot path uses Ethernet port on transition card; host runs in diskless client configuration.
SCSI	XCP2060-TRN I/O transition card; PMC SCSI I/O	May be used for local boot; requires optional transition card with PMC SCSI I/O.
Serial data	XCP2060-TRN I/O transition card	Serial port A on optional transition card is path of default console I/O (see FIGURE 1-3 for location).
SVGA video	XCP2060-TRN I/O transition card and PMC video graphics controller, or CPCI video controller card	CPCI card video controller takes one CPCI slot and attaches directly to CPCI backplane.
USB	XCP2060-TRN I/O transition card	Can be used for keyboard I/O for use with video graphics.

* For details on the correct plugging and usage of the Ethernet port on the front panel of the CP2160 board or the Ethernet port on the RTM, see "Setting Up an Assembled Netra CP2160 Board Computer" on page 3-12.

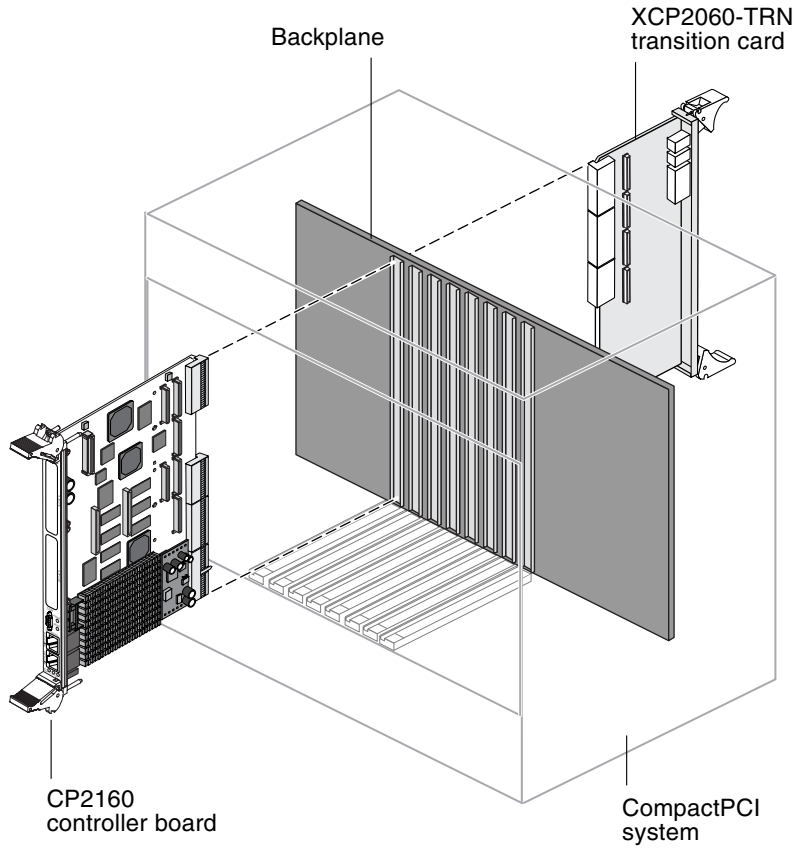

FIGURE 1-4 Typical CPCI System Illustrating the Netra CP2160 Board in System Board Role With XCP2060-TRN Transition Card

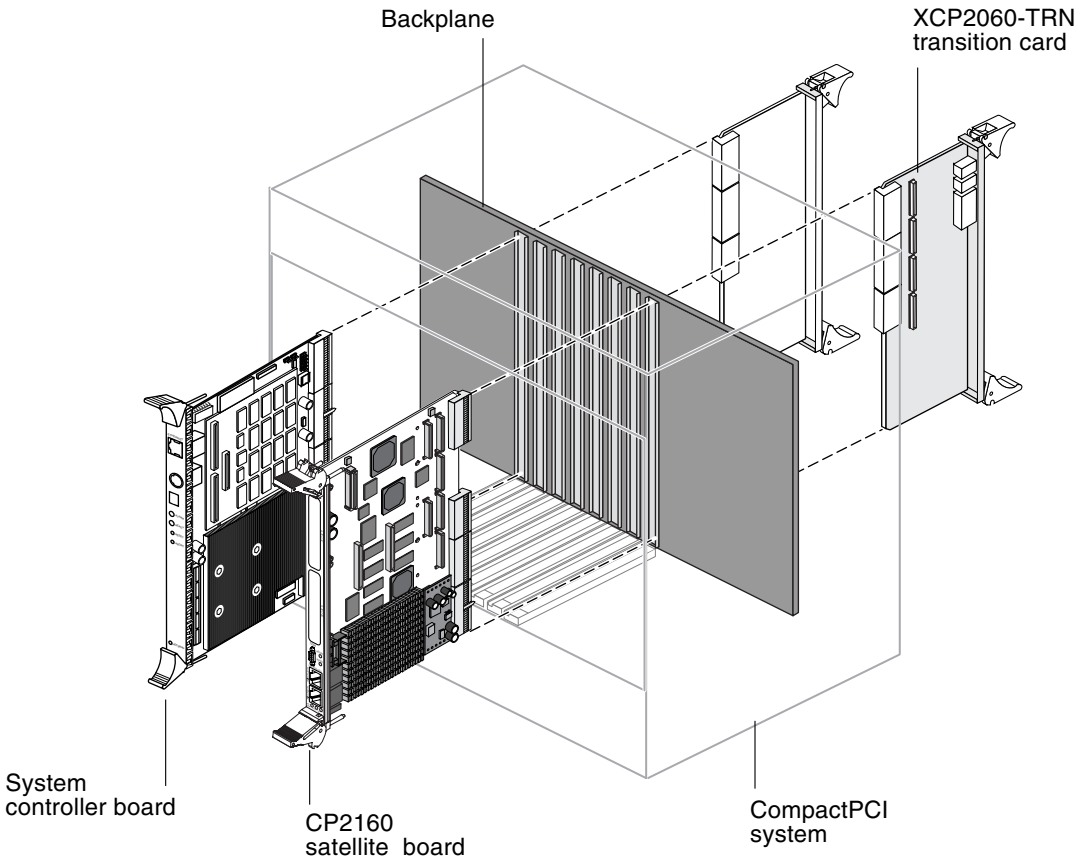

FIGURE 1-5 Typical CPCI System Illustrating the Netra CP2160 Board in Satellite Board Role With XCP2060-TRN Transition Card

1.3 Hot-Swap Support

This section briefly discusses the hot-swap support on the Netra CP2160 boards.

Instructions on hot-swap configurations for the Netra CP2160 satellite board are in Section 2.1, "Hot-Swapping a Netra CP2160 Satellite Board" on page 2-1.

See Appendix C for a reference to the PICMG *CompactPCI Hot Swap Specification* which provides a detailed description of this subject. In general, the hot-swap process includes the orderly connection of the hardware and software. This process uses:

- *Hardware connection control*—to connect the hardware in an orderly sequence; this process includes the use of backplane pins of different lengths to accomplish signal sequencing to protect the hardware and avoid corrupting the backplane bus.
- *Software connection control*—to bind software device drivers to the peripheral hardware once it has been connected or to unbind the drivers from the hardware before disconnection. A failure to achieve this control effectively results in a non-functional peripheral or a system panic.

There are three models of hot swap described in the PICMG *CompactPCI Hot Swap Specification*: basic hot-swap, full hot-swap, and HA hot-swap.

TABLE 1-3 lists the hot-swap support details when a Netra CP2160 board functions as a system host board or as a satellite board.

TABLE 1-3 Netra CP2160 Board Hot-Swap Support

Netra CP2160 Role	Basic Hot-Swap	Full Hot-Swap	HA Hot-Swap
System host board role	Yes	Yes	No
Satellite board role	Yes	Yes	Yes*

* When a board is full hot-swap capable, it implies that the board is also HA hot-swap capable.

Note – The Netra CP2160 host board supports satellite hot-swap insertion/extraction, but the host board itself cannot be inserted or extracted while the server is powered-on. See Section 2.1, "Hot-Swapping a Netra CP2160 Satellite Board" on page 2-1 for more information.

1.4 System Requirements

1.4.1 Hardware Requirements

Sun provides these items to customer order:

- Host board: CP2160S-650-1GB (Netra CP2160 with 1 GB on-board memory)
- Netra CP2160 board memory options: XCP2000-MEM-1GB (1GB memory mezzanine card)

  This memory card is optional must be ordered separately from the Netra CP2160 board. See TABLE A-4 for more information on board memory configurations.

- Rear-access transition card: XCP2060-TRN I/O transition card

  A compatible transition card provides rear I/O access with the Netra CP2160 board. The transition card enables rear system access to the network, to a boot device, and to a console terminal (shown in FIGURE 1-3).

  This transition card is optional and must be ordered separately from the Netra CP2160 board. See the *XCP2060-TRN I/O Transition Card Manual for Netra CP2060/CP2080/CP2160 CompactPCI Boards* (806-6203-*xx*) referenced in Appendix C.

The customer must procure the following components as required:

- Serial terminal or terminal emulation for console output
- Cables for terminal and network connection

  See Section B.2, "Front Panel Connectors" on page B-8 and *XCP2060-TRN I/O Transition Card Manual for Netra CP2060/CP2080/CP2160 CompactPCI Boards* (806-6203-*xx*)for descriptions of I/O connections.

- PIM and PMC hardware

TABLE 1-4 CompactPCI System and Other Minimum Requirements Dependent on Board Function

Requirements	Netra CP2160 as System Host Board	Netra CP2160 as Satellite Board
CompactPCI system box for 6U boards (includes chassis, backplane, power supply*)†	Yes	Yes
Console output device/serial terminal	Yes	Yes
Boot device (such as hard drive or network)	Yes	Yes
Peripheral device for network access	Yes	Yes
System controller	No	Yes

* See Appendix A to ensure that your system enclosure meets the power supply and cooling requirement specifications.

† See FIGURE 1-4 and FIGURE 1-5 for a typical arrangement.

1.4.2 Software Requirements

The Solaris 8 operating environment, release 2/02, or subsequent compatible version, may be used with the Netra CP2160 board system. Refer to Solaris installation manuals for the installation procedure (see Appendix C).

For additional software functionality available through the CP2000 Supplemental CD 4.0 for Solaris 8 contact your field application engineer or refer to the product web site at:

```
http://www.sun.com/products-n-solutions/nep/hardware/boards/cp2160/
```

Note – CP2000 Supplemental CD 3.1 for Solaris 8 can also be used with the Netra CP2160 board, but does not provide all of the features available in the 4.0 version.

1.5 Technical Support and Warranty

Should you have any technical questions or support issues that are not addressed in the Netra CP2160 board documentation set or on the Web site contact your local Sun Enterprise Services. This hardware carries a 1-year return-to-depot warranty. For customers in the US or Canada, please call 1-800-USA-4SUN (1-800-872-4786). For customers in the rest of the world, find the World Wide Solution Center nearest you by visiting our web site:

```
http://www.sun.com/service/contacting/solution.html
```

When you call Sun Enterprise Services, be sure to indicate that the Netra CP2160 board was purchased separately and is not associated with a system. Please have the board identification information ready. For proper identification of the board be prepared to give the representative the board part number, serial number, and date code (see FIGURE 1-6).

1.5.1 Board Part Number, Serial Number, and Revision Number Identification

The Netra CP2160 board part number, serial number, and version can be found on stickers located on the card (see FIGURE 1-6). For proper identification of the board, please see the list below along with FIGURE 1-6.

The Sun barcode label provides the following information (see FIGURE 1-6):

- Board part number (for example, 3753129) which is the first seven digits on the barcode label.
- Board serial number (for example, 000016) which is the next six digits on the barcode label.

The Dash/Revision/Date Code label provides the following information (see FIGURE 1-6):

- Product dash number (for example, -01)
- Revision number (for example REV: 01)
- Board date code (for example, 3702, which represents the thirty-seventh week of year 2002)

The MAC address label contains the MAC address for the board in printed and barcode form. See Section 3.3.4, "Replacing the Serial EEPROM" on page 3-6 for information on installation and removal of the MAC address label.

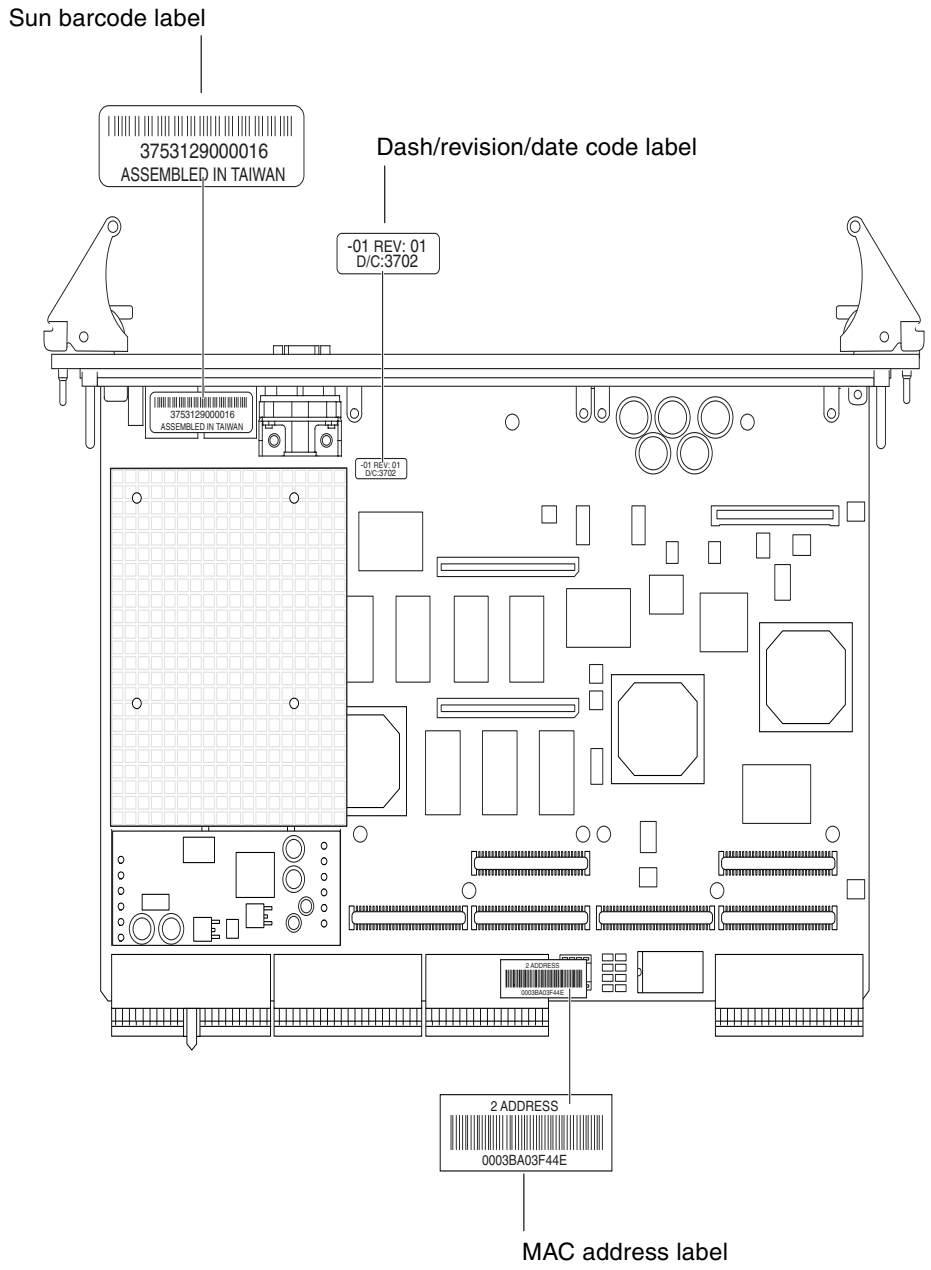

FIGURE 1-6 Labeling on a Typical Netra CP2160 Board

CHAPTER 2

Software Configuration

This chapter contains the following sections:

2.1 Hot-Swapping a Netra CP2160 Satellite Board

Each Netra CP2160 satellite board is capable of working in either basic or full hot-swap modes. If the system is set to work in basic hot-swap mode, then the board has to be manually configured. If the system is set to work in full hot-swap mode, the process of configuration is automatic.

Refer to the READ ME file in the CP2000 Supplemental CD 4.0 for Solaris 8 or CP2000 Supplemental CD 3.1 for Solaris 8 for details on setting the hot-swap mode of the system. Information on obtaining the CD is available from your Field Application Engineer or at the product web site:

`http://www.sun.com/products-n-solutions/nep/hardware/boards/cp2160/`

Note – If the Netra CP2160 board is being used as a system controller board and not functioning as a satellite board, it cannot be hot-swapped at this time.

When it is inserted in a CPCI chassis, a satellite board needs to be configured before it can be used. This process ensures that a board is recognized by the system. (For information on configuring an I/O board, see Section 2.2, "Peripheral I/O Board Configuration" on page 2-7.)

You can check the current status of all the cards in the system by executing the following command in the superuser mode from the system board:

```
# cfgadm
```

This displays a screen showing the current status of the hot-swappable system components. The example below for slot 2 shows a typical display for a satellite board.

```
Ap_Id              Type          Receptacle    Occupant      Condition
c0                 scsi-bus      connected     configured    unknown
c1                 scsi-bus      connected     unconfigured  unknown
pci1:hsc0_slot2    mcd/fhs       connected     configured    ok
pci1:hsc0_slot3    unknown       disconnected  unconfigured  unknown
pci1:hsc0_slot4    unknown       disconnected  unconfigured  unknown
pci1:hsc0_slot5    stpcipci/fhs  connected     configured    ok
pci1:hsc0_slot6    unknown       disconnected  unconfigured  unknown
pci1:hsc0_slot7    unknown       disconnected  unconfigured  unknown
pci1:hsc0_slot8    pci-pci/bhs   connected     configured    ok
```

The hot-swap process for Netra CP2160 satellite boards and I/O boards in basic hot-swap mode and full hot-swap mode are described in the following sections:

- Section 2.1.1, "Hot-Swap Status LED" on page 2-2
- Section 2.1.2, "Basic Hot-Swap Process" on page 2-3
- Section 2.1.3, "Full Hot-Swap Process" on page 2-4

2.1.1 Hot-Swap Status LED

The hot-swap blue LED located on the front panel of the Netra CP2160 board (FIGURE 5-18) lights up when the hot-swap function is enabled by the system software. The hot-swap LED indicates that the board can be extracted from the chassis. When a board is inserted into a CompactPCI system, the LED is lit automatically until the hardware connection process is completed. The LED then remains off until the extraction is once again enabled by the system software.

Note – The user should wait for the blue LED to turn off on the last inserted board before inserting or extracting another board.

2.1.2 Basic Hot-Swap Process

The basic hot-swap process is initiated by executing the `cfgadm` configure command. The `cfgadm` command provides configuration administration operations on dynamically reconfigurable hardware resources. Refer to the man pages (by entering %**man cfgadm**) for additional information on the options associated with this command.

1. **Execute the command to bring down the operating system from the satellite board:**

   ```
   # shutdown -y -g0 -i0
   ```

2. **Execute the unconfiguration command from the system controller board:**

   ```
   # cfgadm -c unconfigure pci1:hsc0_slotx
   ```

   Where *x* is the slot number that the board occupies. See

   This command informs the system to perform the process of extraction of the device.

3. **Wait for the blue LED on the satellite board to turn on.**

4. **Unlock both the ejector handles of the board by pressing the red buttons.**

   Even if you now decide that you do not want to remove the board, you must completely unseat the board and reset the ejection levers again in order to start the software driver attachment process. Simply locking the ejection levers after unlocking them will not start the driver attachment process.

Caution – Do not unconfigure any other boards until the previous board has been unconfigured. Deactivating more than one board at the same time can lead to unpredictable results.

5. **Extract the board and set it aside.**

6. **Slide the new board into the top and bottom mounting rails in the same slot into the backplane while gently keeping the board handles in open position. Once the board is all the way in, lock the ejector handles (see** FIGURE 2-1**).**

   The blue LED is lit once the board makes complete contact with the backplane. The LED goes off shortly after the ejector handles are closed, if the hardware initialization of the board is successful. Otherwise, it will remain lit, indicating that the board has to be replaced.

7. **Once the blue LED of the board is off, install two screws at the top and bottom of the front connector plate to secure the board.**

8. **Execute the configuration command from the system controller board:**

   # **cfgadm -c configure pci1:hsc0_slot***x*

   Where *x* is the slot number that the board occupies.

9. **Take any other step necessary for board-specific configuration.**

2.1.3 Full Hot-Swap Process

Full hot-swap of a board does not require that the system power is turned off. Refer to the chassis manufacturer's documentation for slot assignments and additional information. A full hot-swap board does not require running the `cfgadm` administrative command. The system automatically configures the board for using the system resources. The board-specific configuration steps are still necessary after the completion of host-specific configuration.

Follow these steps to hot-swap a Netra CP2160 board or an I/O board in a chassis that contains the Netra CP2160 board system host board.

1. **Execute the command to bring down the operating system from the satellite board:**

   # shutdown -y -g0 -i0

2. **Unlock both the ejector handles of the satellite I/O board by pressing the red buttons.**

   Wait for the blue light to turn on. Do not unseat the board until the target board LEDs on the system status panel are in the proper state.

   Even if you now decide that you do not want to remove the board, you must completely unseat the board and reset the ejection levers again in order to start the software driver attachment process. Simply locking the ejection levers after unlocking them will not start the driver attachment process.

3. **Extract the satellite board and set it aside.**

4. **Slide the new satellite board into the top and bottom mounting rails in the same slot into the backplane while gently keeping the board handles in open position. Once the board is all the way in, lock the ejector handles (see FIGURE 2-1).**

   The blue LED turns on once the board makes complete contact with the backplane. The LED goes off shortly after the ejector handles are closed, if the hardware initialization of the board is successful. Otherwise, it will remain on, indicating that the board has to be replaced.

5. **Once the blue LED of the board is off, install two screws at the top and bottom of the front connector plate to secure the board.**

Caution – Do not unconfigure any other boards until the first board has been unconfigured. Unconfiguring more than one board at the same time can lead to unpredictable results.

FIGURE 2-1 shows how to release the Netra CP2160 board injector/ejector handles.

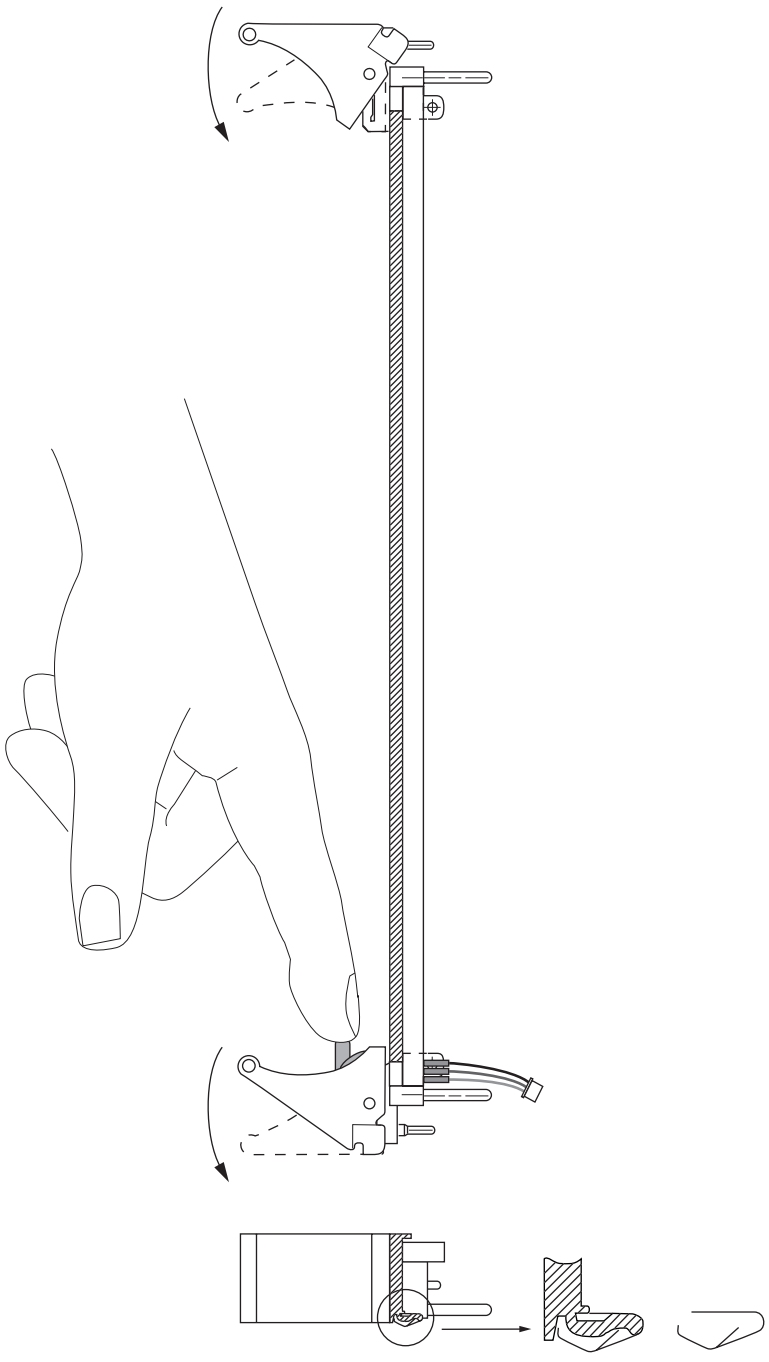

FIGURE 2-1 Releasing the Netra CP2160 Board Injector/Ejector Handles

2.2 Peripheral I/O Board Configuration

Each basic hot-swappable peripheral I/O board, when inserted in a chassis with Netra CP2160, needs to be configured before it can be used. This process ensures that a board is recognized by the system. For information on configuring a satellite board, see Section 2.1, "Hot-Swapping a Netra CP2160 Satellite Board" on page 2-1.

Note – No manual configuration is required to configure an I/O board for full hot-swap mode. It is done automatically upon insertion.

You can check the current status of all the cards in the system by executing the following command in the superuser mode from the system board:

```
# cfgadm
```

This displays a screen showing the current status of the hot-swappable system components like this:

```
Ap_Id              Type          Receptacle     Occupant       Condition
c0                 scsi-bus      connected      configured     unknown
c1                 scsi-bus      connected      unconfigured   unknown
pci1:hsc0_slot2    unknown       disconnected   unconfigured   unknown
pci1:hsc0_slot3    unknown       disconnected   unconfigured   unknown
pci1:hsc0_slot4    unknown       disconnected   unconfigured   unknown
pci1:hsc0_slot5    stpcipci/fhs  connected      configured     ok
pci1:hsc0_slot6    unknown       disconnected   unconfigured   unknown
pci1:hsc0_slot7    unknown       disconnected   unconfigured   unknown
pci1:hsc0_slot8    pci-pci/bhs   connected      configured     ok
```

2.2.1 Configuring a Peripheral I/O Board in Basic Hot-Swap Mode

1. **Enter the following command from the system controller board as superuser to configure a board in slot x:**

```
# cfgadm -c configure pci1:hsc0_slotx
```

Where *x* is the slot number that the board occupies.

The board configuration is complete. You may confirm configuration on the display screen, with the `cfgadm` command. Also see the `cfgadm` (1M) man page for further details.

2. **Execute the following commands from the system board if you are going to activate a networking board with qfe (Quad fast Ethernet) interfaces.**

   # **ifconfig qfe***instance* **plumb**

   # **ifconfig qfe***instance hostname* **up**

   For example, to configure `qfe0`, which is assumed to be assigned to the first physical Ethernet interface of the network board and is the I/O board network interface, you would use `0` in place of the *instance* variable in these following commands.

   See the `ifconfig` (`1M`) man page for further details on configuration options.

2.2.2 Unconfiguring a Peripheral I/O Board in Basic Hot-Swap Mode

1. **Execute the following command from the system controller board:**

   # **ifconfig -a**

   If an interface is running, it shows up on the display screen.

2. **To deactivate the interface, type from the system controller board:**

   # **ifconfig qfe***instance* **down unplumb**

3. **To unconfigure the I/O board type from the system controller board:**

   # **cfgadm -c unconfigure pci0:hsc0_slot***x*

   Where *x* is the slot number that the board occupies.

4. **Wait for the blue LED on the I/O board to turn on before extracting it from the chassis.**

2.3 Setting Up a Diskless Environment

This section provides pointers on how to obtain information on building a remote boot server in a diskless environment. Thus, a Netra CP2160 board acts as a diskless client booted over the network.

For information on how to set up a diskless server, see Section 2.3.1, "How to Set Up a Boot Server" on page 2-9. For information on how to use a tip line connection on a diskless client and boot over the net, see Section 2.3.2, "How to Boot as a Diskless Client" on page 2-9.

2.3.1 How to Set Up a Boot Server

For information on how to boot from a diskless server, refer to the document *Solaris 8 Advanced Installation Guide* (806-0957-*xx*)

The document contains a section on *How to Create a Boot Server on a Subnet* and is available on line, in PDF format or for purchase through the following URL:

`http://docs.sun.com/documentation`

2.3.2 How to Boot as a Diskless Client

For information on working with diskless clients, refer to the document *Solaris 8 System Administration Supplement* (806-6611-*xx*).

The document contains a section on *How to Set Up Your Diskless Client Environment* and *How to Add Diskless Clients* and is available online, in PDF format or for purchase through the following URL:

`http://docs.sun.com/documentation`

2.4 Setting the Time of Day on a Battery-less System

Because the Netra CP2160 board is battery-less, the date and time stored in the TOD chip are not backed up when the system is powered-off. When the system is powered-on, the OpenBoot PROM initializes the date and time fields of the TOD chip. This feature can be configured in different ways in a networked configuration or on a standalone system.

2.4.1 In a Networked Configuration

The Network Time Protocol (NTP) provides the correct timestamp for all systems on a network by synchronizing the clocks of all the systems. A Solaris server, called xntp, is queried by OpenBoot PROM for setting and maintaining the timestamp. At least one system or board in the same subnet as the Netra CP2160 board must be

configured to be an xntp server. Refer to the online man pages for the `xntpd` (`1M`), `ntpq` (`1M`), and `ntpdate` (`1M`) commands for more information about configuring a system to be an xntp server.

The OpenBoot PROM NTP client will be invoked only when system has gone through a hardware power cycle and the configuration variable `ntp-enable?=true` (default value is `false`). The TOD will be programmed with the date and time received from the NTP server.

The configuration variable `ntp-server-addr` can be set with the NTP server's IP address. The default value for `ntp-server-addr` is a broadcast address (`255.255.255.255`). The default value implies that OpenBoot PROM NTP client will broadcast its NTP request in the subnet and update the TOD's date and time as per the response received from an NTP server in the subnet.

TABLE 2-1 Values for `ntp-server-addr` Variable

ntp-server-addr	Action
default value	The OpenBoot PROM NTP client will broadcast its NTP request in the subnet.
NTP server's IP address	The OpenBoot PROM NTP client will send the NTP request to the NTP server

If `ntp-enable?=false`, OpenBoot PROM will not invoke its NTP client and the TOD will be programmed with system manufacture date (`system-board-date`) and the time will be set to start at 00:00:00 hours.

TABLE 2-2 Values for `ntp-enable?` Variable for Networked Configuration

ntp-enable?	Action
`false`	OpenBoot PROM will not invoke its NTP client and programs the TOD with the system manufacture date.
`true`	OpenBoot PROM sends an NTP request and programs the TOD with the response from NTP server. In case of any failure, OpenBoot PROM will program the TOD with the system manufacture date and time (00:00:00 Hrs)

To use the NTP feature at Solaris level, disable NTP at the OpenBoot PROM level (`ntp-enable?=false`) and configure the NTP client at the Solaris level.

For information on setting OpenBoot PROM configuration variables, see the section "OpenBoot PROM Configuration Variables".

2.4.2 On a Standalone System

On a standalone battery-less system which cannot get the time of day from a network, the TOD will be programmed with the system manufacturing date (`system-board-date`) after the system is power-cycled, regardless of the `ntp-enable?` variable setting.

TABLE 2-3 Values for `ntp-enable?` Variable for Standalone Configuration

ntp-enable?	Action
`false`	OpenBoot PROM will not invoke its NTP client and programs the TOD with the system manufacture date.
`true`	The OpenBoot PROM NTP request will timeout after one minute and the OpenBoot PROM will program the TOD with the system manufacture date and time (00:00:00 Hrs).

To manually set the time of day after power is restored:

As root, at the Solaris prompt, enter the date command.

`date` [*mmddHHMMccyy*]

where:

mm is the current month

dd is the current day of the month

HH is the current hour of the day

MM is the current minutes past the hour

cc is the current century minus one

yy is the current year

Refer to the online man page for the `date(1M)` command if you need additional information. After you set the date, you must reboot (but not power cycle) the system for the changes to take full effect. Failing to reboot can cause problems.

CHAPTER 3

Hardware Installation

This chapter describes some of the typical system configurations in which the Netra CP2160 board may be used.

This chapter contains the following sections:

3.1 Equipment and Operator Safety

Refer to the *Important Safety Information for Sun Hardware Systems* (816-7190-*xx*) for general safety information.

Read these safety statements specific to the Netra CP2160 board carefully before you install or remove any part of the system.

Caution – Depending on the particular chassis design, operations with open equipment enclosures can expose the installer to hazardous voltages with a consequent danger of electric shock. Ensure that line power to the equipment is disconnected during operations that make high voltage conductors accessible.

The installer must be familiar with commonly-accepted procedures for integrating electronic systems and with the general practice of Sun systems integration and administration. Although parts of these systems are designed for hot-swap operation, other components must not be subjected to such stresses. Work with power connected to a chassis only when necessary and follow these installation procedures to avoid equipment damage.

This equipment is sensitive to damage from electrostatic discharge (ESD) from clothing and other materials. Use the following antistatic measures during an installation.

- If possible, disconnect line power from the equipment chassis when servicing a system or installing a hardware upgrade. If the chassis cannot be placed upon a grounded antistatic mat, connect a grounding strap between the facility electrical input ground (usually connected to the equipment chassis) and facility electrical service ground.
- Use an antistatic wrist strap when:
  - Removing a board from its antistatic bag
  - Connecting or disconnecting boards or peripherals

  The other end of the strap lead should be connected to one of the following:

  - A ground mat
  - Grounded chassis metalwork
  - A facility electrical service ground
- Keep boards in the antistatic bags until they are needed.
- Place circuit boards that are out of their antistatic bags on an antistatic mat if one is available. The mat must be grounded to a facility electrical service ground. Do not place boards on top of an antistatic bag unless the outside of the bag also has antistatic protective properties.
- Remove a board from its antistatic bag only when wearing a properly-connected ground strap.

3.2 Preparing for Installation

Read the following subsections before starting to install these boards. In addition, do the following:

1. Become familiar with the contents of the referenced documentation.
2. Verify that all listed hardware and software is available (see Section 1.4, “System Requirements” on page 1-11).

3. Check power, thermal, environmental and space requirements (see Section 3.2.1, "Checking Power, Thermal, Environmental, and Space Requirements" on page 3-3).
4. Verify that local area networking (LAN) preparations are completed (see Section 3.2.2, "Determining Local Network IP Addresses and Hostnames" on page 3-4).
5. Ensure that the hostnames and their network IP addresses are allocated and registered at the site.

3.2.1 Checking Power, Thermal, Environmental, and Space Requirements

Ensure that:

- Your enclosure specifications support the sum of the specified maximum board power loads. See Section A.6, "Power Requirements" on page A-6 for board power specifications.
- Facility power loading specifications can support the rack or enclosure requirements.
- Your enclosure specifications support the cooling airflow requirements. See Section A.8, "Environmental Specifications" on page A-8.
- The Netra CP2160 board fits a standard CompactPCI chassis. If your installation requirements are different, contact your field application engineer.

3.2.2 Determining Local Network IP Addresses and Hostnames

Collect the following information to connect hosts to the local area network (LAN). Ask your network administrator for help, if necessary. This information is not needed for a standalone installation You can use TABLE 3-1 to record this information.

TABLE 3-1 Your Local Network Information

Information Needed	Your Information
IP addresses* and hostname for each Netra CP2160 client	
Domain name	
Type of name service and corresponding name server names and IP addresses--for example DNS and NIS (or NIS+)	
Subnet mask	
Gateway router IP address	
NFS server names and IP addresses	
Web server URL	

* Local IP addresses are not needed if they are assigned by a network DHCP server

You may need the MAC (Ethernet) addresses of the local hosts to make nameserver database entries. The MAC address can be seen in the console output while booting to the `ok` prompt. It can also be derived from the Host ID seen on the label of the I^2C EEPROM package.

3.2.3 Installation Procedure Summary

The steps in this section summarize the Netra CP2160 board installation at a high level. Make sure to read the details in Section 3.3, "Configuring the Netra Board Hardware" on page 3-5 through Section 3.7, "Software Installation" on page 3-17 before installing the board.

The procedure to setup and configure a Netra CP2160 board in a system includes the following steps:

1. Configure host board physical hardware. For example, install memory and PMC cards, replace the serial EEPROM, and set switches if necessary.

2. Configure the transition card with PIMs, switch settings, or connector attachments, as necessary.
3. Physically install the transition card (as necessary), host, and any peripheral boards into the chassis.
4. Connect the host(s) to a local network. Alternatively, the host can be run as a standalone system without a network connection.
5. Install the operating system.

3.3 Configuring the Netra Board Hardware

This section lists hardware installation and settings that may or may not apply for your board configuration. Read and perform the procedures, as necessary, before installing the Netra CP2160 board into the chassis.

3.3.1 Installing the Memory Module

The Netra CP2160 board can accommodate modular memory. For directions on the installation process of the memory modules on the Netra CP2160 board, refer to the document *Memory Module Installation and Removal Guide for Netra CP2000/CP2100 Series Boards* (817-0654-*xx*).

3.3.2 Installing the PMC Module

Use the PMC card manufacturer's procedure to install these cards.

3.3.3 Setting Switches

Section B.4, "Switch Settings" on page B-14 details the SW2501 and SW4101 switch settings for the Netra CP2160 board.

3.3.4 Replacing the Serial EEPROM

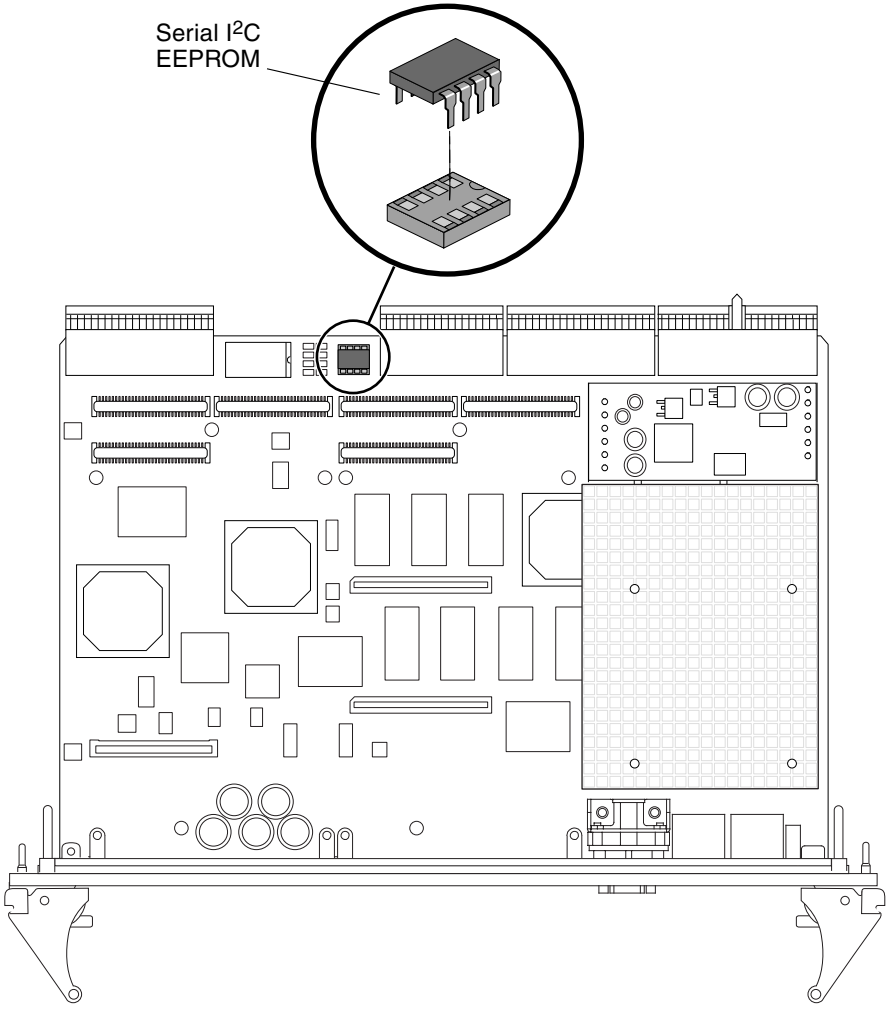

FIGURE 3-1 Replacing the Serial I2C EEPROM

The serial I2C EEPROM stores the backup copy of the board MAC address and host ID information (see Section 5.3.4.4, "Serial I2C EEPROM" on page 5-12 for more information).

If you need to replace the Netra CP2160 board, remove the serial I^2C EEPROM from the original board and install it on the new Netra CP2160 board.FIGURE 3-1 shows the position of the serial I^2C EEPROM on the Netra CP2160 board.The MAC address label is positioned on top of both the serial I^2C EEPROM and the J3 connector. See FIGURE 1-6 for the location of the MAC address label.

3.3.5 Configuring Transition Card Hardware

If you are using the XCP2060-TRN I/O transition card, refer to the *XCP2060-TRN I/O Transition Card Manual for Netra CP2060/CP2080/CP2160 CompactPCI Boards* (P/N 806-6203-xx). You may also refer to the transition card manual for detailed connector pin assignments.

3.3.5.1 Installing PIM Assemblies

Use the PMC card manufacturer's procedure to install these cards. Only the PIM A and PIM B Connector Power Pin Assignments are provided in TABLE 3-2.

Caution – When installing a PIM card on to the transition card, ensure that the PIM card power signals match the corresponding power signals of the PIM connectors that are to be installed on the XCP2060-TRN I/O Transition Card.

TABLE 3-2 PIM A and PIM B Connector J0 Power Pin Assignments (J400 and J500)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1		17		33		49	
2	+12V	18	GND	34	GND	50	GND
3		19		35		51	
4		20		36		52	
5	+5V	21	+5V	37	+5V	53	+5V
6		22		38		54	
7		23		39		55	
8		24		40		56	
9		25		41		57	
10	+3.3V	26	+3.3V	42	+3.3V	58	+3.3V
11		27		43		59	
12		28		44		60	

TABLE 3-2 PIM A and PIM B Connector J0 Power Pin Assignments (J400 and J500)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
13	GND	29	GND	45	GND	61	-12V
14		30		46		62	
15		31		47		63	
16		32		48		64	

3.4 Installing Boards Into the CompactPCI Chassis

This section describes the installation of the transition card, the system host board, the satellite board and the I/O cards into a Netra CP2160 CompactPCI system chassis.

3.4.1 Installing the XCP2060-TRN I/O Transition Card

Use the installation procedure detailed in the *XCP2060-TRN I/O Transition Card Manual for Netra CP2060/CP2080/CP2160 CompactPCI Boards* (806-6203-*xx*) to install the XCP2060-TRN transition card.

Note – If the system power is on when installing the XCP2060-TRN I/O transition card, the transition card *must* be installed before its mating Netra CP2160 board.

A compatible transition card must be used with the Netra CP2160 board for rear I/O access. The transition card enables access to the network, to a boot device and to a console terminal. You may use the XCP2060-TRN I/O transition card, or you may design your own transition card.

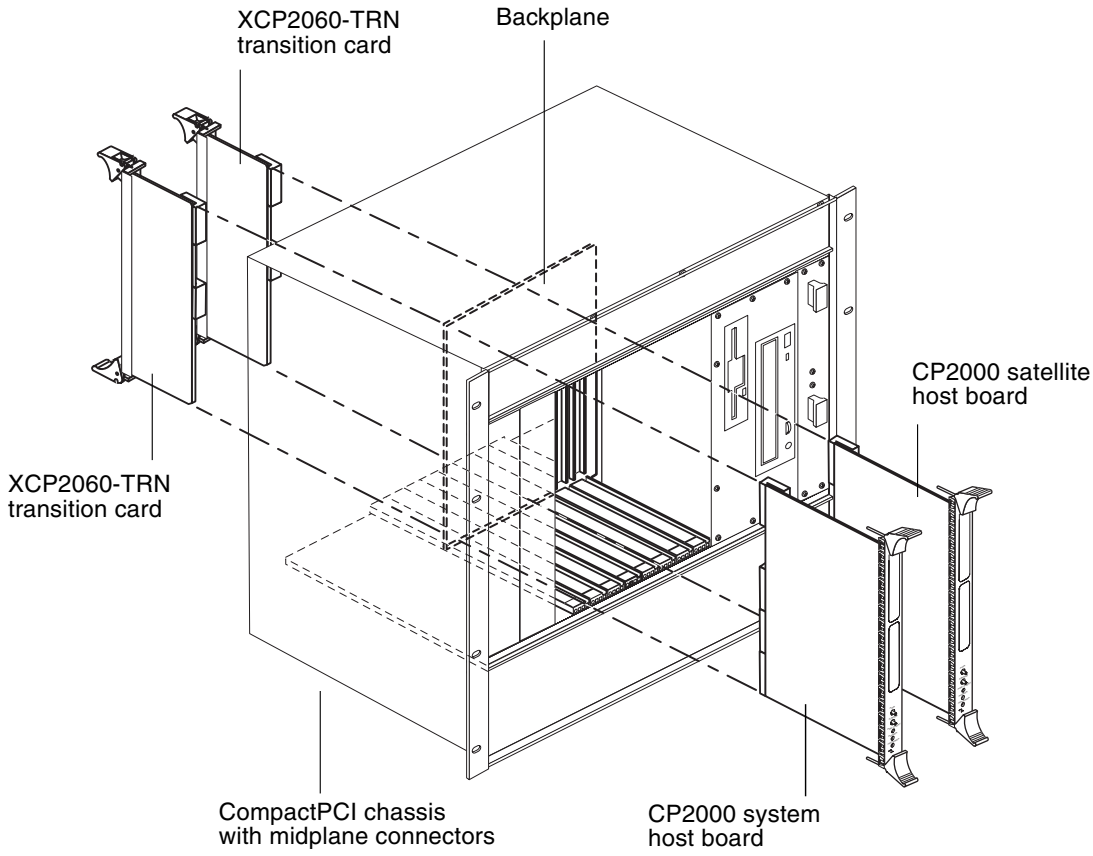

FIGURE 3-2 Installing the XCP2060-TRN CPCI I/O Transition Card

3.4.2 Installing the Netra CP2160 Board

A CompactPCI chassis contains:

- A system slot, usually the leftmost slot (as viewed from the front). The system slot is indicated by a triangle symbol visible on the backplane, if the chassis meets the PICMG 2.0 CompactPCI specification.
- Seven peripheral slots (for a single-segment chassis). Peripheral slots are identified by a circle symbol visible on the backplane.

To use the Netra CP2160 board as a system controller, install the board into the system board slot. To use the Netra CP2160 board as a satellite board, install the board into a peripheral slot. (see Section 5.4.3.1, "Arbitration in System Controller Role" on page 5-15).

1. **Ensure that power is disconnected from the chassis.**

   The Netra CP2160 satellite board can be installed while the chassis is powered—however *only start with a powered chassis if necessary.* See Section 2.1, "Hot-Swapping a Netra CP2160 Satellite Board" on page 2-1 for information on hot-swapping the Netra CP2160 satellite board.

   The Netra CP2160 board cannot be hot-swapped when used as a system controller.

2. **Check that the corresponding XCP2060-TRN I/O transition card is installed.**

   If you need a transition card for I/O for the Netra board, ensure that it is already present in the chassis. This step is essential if the chassis is powered during the installation.

3. **Slide the Netra CP2160 board into the appropriate slot on the corresponding top and bottom mounting rails and toward the backplane while gently pushing the board handles inward.**

   While sliding the board, ensure that the Netra CP2160 board extraction levers are aligned perpendicular to the card flange in the unlocked position and that the board connectors are aligned with the transition card connectors.

4. **Install two screws through the top and bottom of the front connector plate to secure the board.**

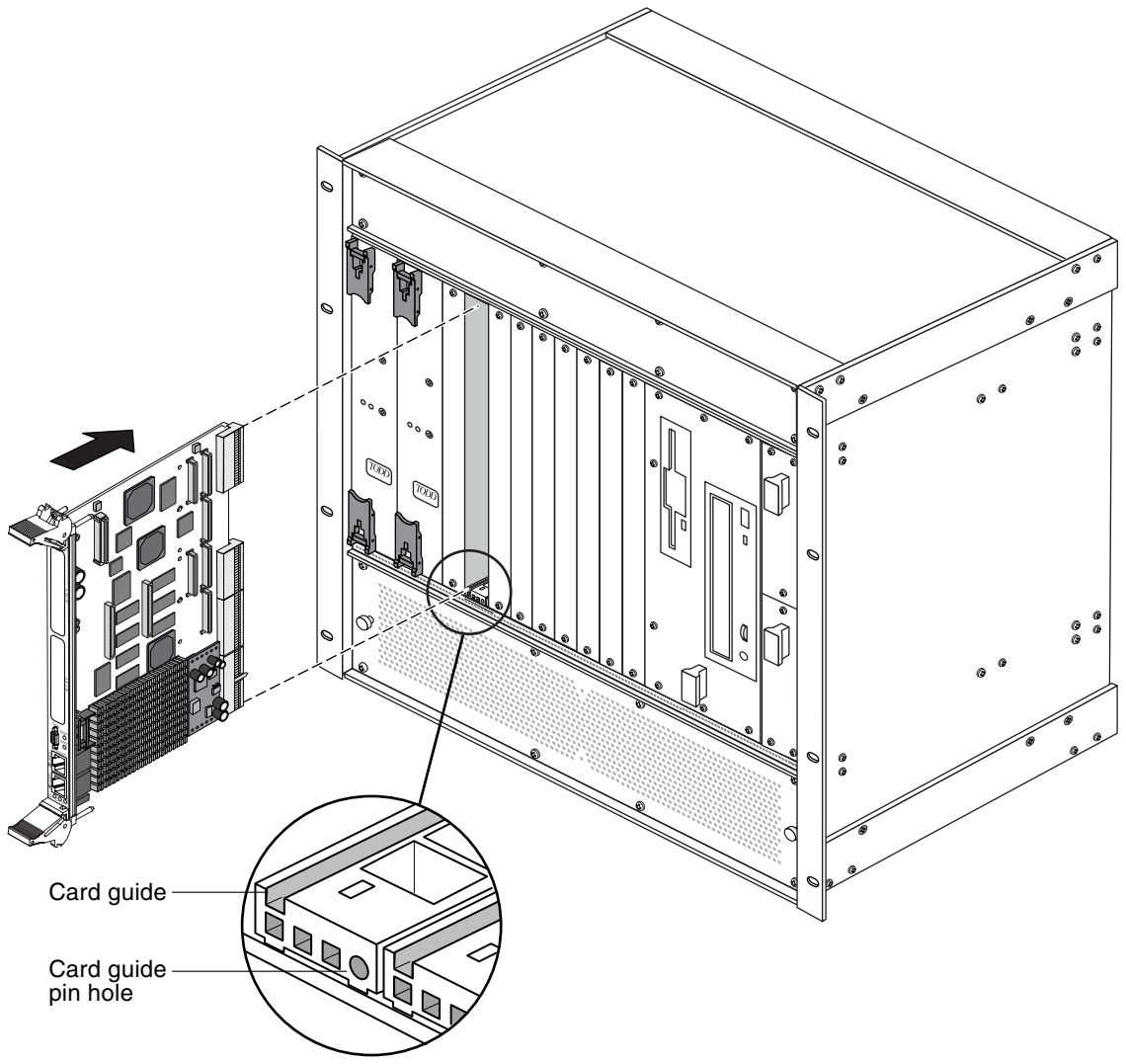

FIGURE 3-3 Installing a Typical Netra CP2160 Board Into a CompactPCI Chassis in a System Host Slot

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Note – Follow the CompactPCI chassis manufacturer's instructions to make sure the Netra CP2160 board is installed into the system controller slot.

3.4.3 Installing an I/O Board

Various I/O boards (I/O cards) can be installed in the chassis that contain the Netra board. If these boards meet hot-swap requirements, these can be hot-inserted and do not require that the system is powered down. These I/O cards need to be installed in their respective slots. Refer to the chassis manufacturer's documentation for slot assignments and for special installation instructions.

The basic I/O card installation procedure is the same as described in Section 3.4.2, "Installing the Netra CP2160 Board" on page 3-9. The ejector handles on the I/O cards may not be the same style as Netra board ejector handles. Some boards have retracting ejector handles. Refer to the I/O card manufacturer's instructions on how to engage or disengage ejector handles that secure that board to the chassis.

Refer to Section 2.2, "Peripheral I/O Board Configuration" on page 2-7 for information on configuring and I/O card to work with a Netra CP2160 host board.

3.5 Setting Up an Assembled Netra CP2160 Board Computer

This section describes how to set up a computer that contains the Netra CP2160 board.

1. **Using a category 5 grade network cable, connect one RJ45 connector into the receptacle on the front panel of the Netra CP2160 board or on the rear flange of the transition card (RTM).**

   The other end must be connected to a suitable 10/100 Mb Ethernet hub on the local subnet. To use the front ethernet ports, set the NVRAM variable to true (this is the default setting). To use the RTM ethernet port, set the NVRAM variable "front-phy?" to false. The command syntax at the `ok` prompt is:

   ```
   ok setenv front-phy? false
   ok reset-all
   ```

   Plug the ethernet cables only on one set of ports; plug the cables on the front panel ports when using front ports and plug them on the RTM when using the the rear ethernet ports. They should not be plugged on both sides at the same time.

Note – When used as a system controller, the CP2160 board is Class A for EMI compliance. When used as a satellite card, the CP2160 board is Class B under the following conditions. For Class B EMI compliance of front access ports, use of shielded cables is required on all I/O ports. For Class B compliance of rear access ports, use of shielded cables is required on the serial I/O port and unshielded cables can be used on the Ethernet port. The shields for all shielded cables must be terminated on both ends.

2. **Connect I/O cabling to the host board and to the serial port of the host system.**
3. **Connect a serial cable to the ttya port on the front panel of the Netra CP2160 board or the the XCP2060-TRN CPCI I/O transition card of the target machine and to the serial port of the host machine.**
4. **Use the `tip` utility on the host system to establish a full-duplex terminal connection with the Netra CP2160 board.**
5. **At the UNIX prompt in a command tool or shell tool, type:**

   ```
   tip -9600 /dev/ttya
   ```

6. **Connect any other peripheral devices (such as a printer) to the appropriate connector.**

3.6 Initial Power On and Firmware Upgrade

3.6.1 Powering on the System

1. **Power on the system that contains the Netra CP2160 board to run the power-on self-tests (POST). For details on POST, see Chapter 4, Firmware.**
2. **After running POST, install the Solaris operating environment package on the system that contains the Netra CP2160 board (see Section 3.7.1, "Installing the Operating System" on page 3-17).**

3.6.2 Determining the Firmware Version

If the installed version is not current, update the OpenBoot PROM before continuing (see Section 3.6.3, "Upgrading the OpenBoot PROM Firmware" on page 3-14). The third character group (`x`) in OpenBoot PROM is the revision number.

3.6.2.1 Determining the Firmware Version From OpenBoot PROM

To determine the installed OpenBoot PROM version, use the `.version` command at the `ok` prompt. An example of the screen print-out is shown below.

```
Firmware version 1.0.1
SMC Firmware Release 4.0.6 TEST Platform ID 21
*** SMC FIRMWARE NOT FOR PRODUCTION ***
FPGA Version 1.2
PLD Version 4.2
Firmware CORE Release 0.0.7 created 2002/9/23 17:2
Release 4.0 Version 11 created 2002/09/30 12:27
cPOST version 0.0.1 created 2002/6/28
CORE 0.0.7 2002/09/23 17:02
```

Note – In the above printout example, the OBP release version is 4.0.11, as specified in the seventh line of the printout.

3.6.2.2 Determining the Firmware Version From the Solaris Prompt

Use the **`prtconf`** command at the *machine_name***`%`** prompt.

*machine_name***`% /usr/bin/prtconf -V`**
`OBP 4.0.xx` *creation date*

3.6.3 Upgrading the OpenBoot PROM Firmware

This firmware can only be upgraded when operating at the OpenBoot PROM level, that is, at the `ok` prompt.

Note – See information for sequencing of SMC and board upgrade information provided on the product web site at:
`http://www.sun.com/products-n-solutions/nep/hardware/boards/CP2160`

---

1. **Download the latest Netra CP2160 host firmware binaries.**

2. **Bring the system down to OpenBoot PROM level.**

   If your Netra CP2160 board is currently running Solaris software, become superuser and issue the command:

```
# sync; sync; halt
```

3. **Check the present firmware revision.**

   Check the current firmware revision on the target system by typing:

```
ok .version
```

   A *typical* output is:

```
ok .version
Firmware version 1.0.1
SMC Firmware Release 4.0.6 TEST Platform ID 21
*** SMC FIRMWARE NOT FOR PRODUCTION ***
FPGA Version 1.2
PLD Version 4.2
Firmware CORE Release 0.0.7 created 2002/9/23 17:2
Release 4.0 Version 11 created 2002/09/30 12:27
cPOST version 0.0.1 created 2002/6/28
CORE 0.0.7 2002/09/23 17:02
```

Note – In the above printout example, the OBP release version is 4.0.11, as specified in the seventh line of the printout.

---

4. **Disable autoboot, then reset the system.**

   Disable autoboot and reset the system by means of the commands:

```
ok setenv auto-boot? false
ok reset-all
```

5. **Flash update your firmware.**

```
ok flash-update device; obp-file-path/obp-latest-binary
ok smc-flash-update device; smc-file-path/smc-latest-binary
```

Note – The `flash-update` command will execute both the SMC and SPARC flash updates if they are both included in the file path. You can still use the `smc-flash-update` if you want to update the SMC flash only.

The system should automatically reset. If it does not, power cycle it.

6. **Check the firmware revision.**

   Check the firmware revision by typing:

```
ok .version
```

   The form of the output appears as in Step 3. Ensure that the version information shows up as expected. If not, please attempt the OpenBoot PROM upgrade once more.

7. **Enable auto booting and reset the system.**

   a. **Enable auto booting by typing:**

```
ok setenv auto-boot? true
```

   b. **Reset the system to boot Solaris software:**

```
ok reset-all
```

   Please contact your service personnel if you face any problems.

Note – Solaris scripts are also available to upgrade core OpenBoot PROM firmware.

3.7 Software Installation

3.7.1 Installing the Operating System

The Solaris 8 operating environment, Release 2/02 or subsequent compatible version, may be used with the Netra CP2160 board system. Refer to Solaris installation manuals for the installation procedure (see Appendix D).

For additional software functionality available through the CP2000 Supplemental CD 4.0 for Solaris 8, contact your field application engineer or refer to the product web site at:

`http://www.sun.com/products-n-solutions/nep/hardware/boards/cp2160/`

Note – CP2000 Supplemental CD 3.1 for Solaris 8 can also be used with the Netra CP2160 board, but does not provide all of the features available in the CD 4.0 version.

3.7.2 Downloading and Installing SunVTS

Sun Validation Test Suite (SunVTS™) is a comprehensive software package that tests and validates the Netra CP2160 board by verifying the configuration and function of most hardware controllers and devices on the board. SunVTS is used to validate a system during development, production, inspection, troubleshooting, periodic maintenance and system or subsystem stressing. SunVTS can be tailored to run on various types of machines ranging from desktops to servers with modifiable test instances and processor affinity features.

You can perform high-level system testing by using the appropriate version of SunVTS. For detailed information on SunVTS support and downloads, refer to the following web site:

`http://www.sun.com/oem/products/vts/index.html`

The SunVTS packages are also located on the Solaris 8 Supplemental Software CD for Sun Computer Systems that ships with the Solaris operating environment release.

Ensure that the SunVTS software version is compatible with the Solaris operating environment version being used. Solaris 8 2/02 operating environment is compatible with SunVTS 4.6 package.

Information on the version of the SunVTS software installed can be found in the file:

```
/opt/SUNWvts/bin/.version
```

To obtain SunVTS documentation, contact your local customer service representative or field application engineer.

Note – For security reasons only a superuser is permitted to run SunVTS. Installation and starting instructions are included with the software when it is downloaded.

CHAPTER 4

Firmware

The Netra CP2160 board platform comprises a modular firmware architecture that gives the user latitude in controlling boot initialization. The user can customize initialization and test firmware, even enabling installation of a custom operating system.

This platform also employs the System Management Controller (SMC)—described in Section 5.6, "System Management Controller" on page 5-24—which controls the CompactPCI interface, System Management and Hot Swap control, and some board hardware. The SMC configuration is controlled by separate firmware.

This chapter contains the following sections:

4.1 Initialization Firmware

Control flow at board startup is shown in FIGURE 4-1. Execution begins in Firmware Common Operations andReset Environment (CORE)—which includes Basic POST (BPOST). It passes to Comprehensive POST (CPOST) and Extended POST (EPOST), if these are present, before returning to firmware CORE and on to OpenBoot PROM.

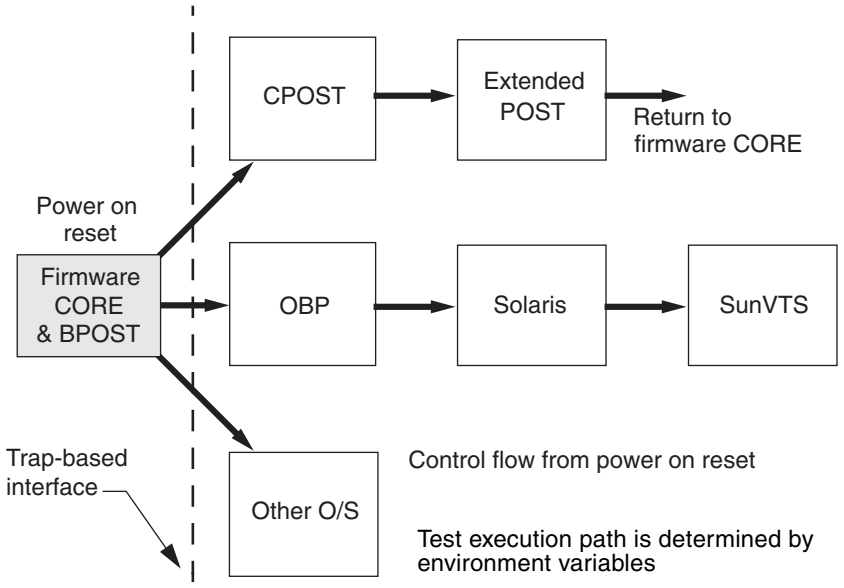


FIGURE 4-1 Control Flow from Power On for Firmware CORE and Client Modules—Solaris Case

4.1.1 Firmware CORE and BPOST

Firmware CORE:

- Unifies system initialization and I/O Operations for a higher level client, for example, OpenBoot PROM for Solaris software
- Avoids any duplication of effort for the same type of functions among various clients
- Provides a unified interface to higher level software using a soft-trap mechanism. Trap services (software interrupts) are used to abstract hardware-dependent features behind a uniform service interface. Sun SPARC processors are designed with a common software trap structure that is useful for this common programming interface, so that clients may not need to carry another copy of those drivers and may use those services provided by Firmware CORE until their driver takes over.
- Provides access, early in the boot sequence, to the hardware-dependent services needed for client initialization; examples are I/O devices including serial port and net.
- Provides basic system tests that can replace existing POST in `min mode`
- Enables extensive system testing to be done using the POST dropin in `max mode`

- Provides error recovery from exceptions which currently does not exist in OpenBoot PROM.
- Enables use of popular languages with efficient compilation and easier debugging for development

BPOST is integrated into Firmware CORE. BPOST tests are interleaved with the initialization activities of Firmware CORE to present a foundation of validated and initialized hardware to run subsequent code such as that in CPOST or OpenBoot PROM. The tests listed in TABLE 4-1 are examples of CORE and BPOST flow of execution.

Note – Not all of the hardware listed in this table is present on this platform. When a hardware item is not detected by the firmware, this firmware makes no attempt to test or initialize it.

Because BPOST runs from PROM, its extent of testing is limited to that needed by modules that are loaded later. Such a module, for example CPOST, can perform comprehensive testing more quickly because it executes from DRAM.

TABLE 4-1 Firmware CORE and BPOST Flow of Execution

Firmware CORE Service	Detail
Initialize Processor	Sets processor in stable state
Initialize NVRAM	Sets up state variables
Initialize EBus and bridges	Initializes EBus and UPA/PCI and PCI/PCI bridges in path between CPU and EBus devices
InitializeTTY	For message display
Set memory timings	
Verify NVRAM	Check magic number. Set defaults if bad
Check keyboard	Probe & initialize keyboard, set TTYA otherwise
Check I/P device for key pressed	Set state variables in NVRAM accordingly
Cache, MMU test	Perform basic diagnostics on caches & MMUs*
Initialize caches, MMUs	Setup I and D caches and MMUs
Memory test	Perform partial memory test†
Memory probe	Probe memory and clear top memory region
MMU and cache setup	Setup I/D MMUs with valid mappings; enable MMUs and I/D caches
Copy Firmware CORE	Copy Firmware CORE into memory and transfer control to the RAM copy
Setup trap table	Set up trap table in memory
Initialize interrupts	Set up hardware interrupts
Initialize TOD	
Set up CPU counter	Calibrate CPU counter to determine module speed
Probe PCI bus	Probe for Primary PCI system bus
Execute POST dropin†	
Locate the client	Locate the client in PROM. If found, copy into memory and transfer control to it
Enter user interface	OpenBoot PROM for Solaris software, else RTOS or custom OS

* Execute if hardware power-on, run-post set to true, post-level set to min/max and key to skip post not pressed

† Execute if h/w power-on, run-post set to true, post-level set to max and key to skip post not pressed

4.1.2 CPOST and EPOST

CPOST contains tests for higher-level board functions. By placing these tests in a separate module, the user has the option of performing them and the developer can substitute them with other tests. Examples of CPOST tests are:

- PCI configuration register test for PCIO-2
- DMA tests

4.1.3 EPOST

EPOST is used for additional POST code dropins that are provided by the user.

4.1.4 OpenBoot PROM

Rather than executing the initialization code that formerly existed in OpenBoot PROM for prior Sun board platforms, OpenBoot PROM now makes calls to the traps laid down by Firmware CORE. OpenBoot PROM exists in the form of a dropin in the System Flash memory area.

OpenBoot PROM probes for devices and builds the device tree, which is a table that contains entries for how drivers communicate with connected hardware. Each line, or entry, of the device tree is a reference for the node entry for the peripheral in the `/dev` directory. The device tree is inherited by Solaris software as it is booted. An example of a device tree is shown below. The device tree can be seen by directory in the `/` directory. The device tree is inherited by Solaris software as it is booted. An example of a device tree is shown below. The device tree can be seen by typing **`show-devs`** at the `ok` prompt. An example of a device tree appears below.

CODE EXAMPLE 4-1 Example of a show-devs Device Tree

```
ok show-devs
/SUNW,UltraSPARC-IIe@0,0
/pci@1f,0
/virtual-memory
/memory@0,0
/aliases
/options
/openprom
/chosen
/packages
/pci@1f,0/pci@1
/pci@1f,0/pci@1,1
/pci@1f,0/pci@1/pci@1
/pci@1f,0/pci@1,1/usb@3,3
/pci@1f,0/pci@1,1/network@3,1
/pci@1f,0/pci@1,1/usb@1,3
/pci@1f,0/pci@1,1/network@1,1
/pci@1f,0/pci@1,1/ebus@3
/pci@1f,0/pci@1,1/ebus@1
/pci@1f,0/pci@1,1/usb@3,3/device@3
/pci@1f,0/pci@1,1/ebus@3/sysmgmt@14,600000
/pci@1f,0/pci@1,1/ebus@1/flashprom@10,400000
/pci@1f,0/pci@1,1/ebus@1/su@14,300000
/pci@1f,0/pci@1,1/ebus@1/su@14,320010
/pci@1f,0/pci@1,1/ebus@1/idprom
/pci@1f,0/pci@1,1/ebus@1/eeprom@14,0
/pci@1f,0/pci@1,1/ebus@1/flashprom@10,0
/openprom/client-services
/packages/kbd-translator
/packages/dropins
/packages/SUNW,builtin-drivers
/packages/disk-label
/packages/obp-tftp
/packages/deblocker
/packages/terminal-emulator
ok
```

OpenBoot PROM also contains aliases for some of the devices shown in the device tree, These aliases can simplify hardware access at the ok prompt, for example:

CODE EXAMPLE 4-2 Aliases for Devices in the Device Tree

```
ok boot disk1
ok devalias

userprom1
/pci@1f,0/pci@1,1/ebus@1/flashprom@10,400000
hsc                    /pci@1f,0/pci@1,1/ebus@3/sysmgmt@14,600000
dload                     /pci@1f,0/pci@1,1/network@1,1:,
systemprom                /pci@1f,0/pci@1,1/ebus@1/flashprom@10,0
pcic                      /pci@1f,0/pci@1/pci@1
pcib                      /pci@1f,0/pci@1,1
pcia                      /pci@1f,0/pci@1
ebus2                     /pci@1f,0/pci@1,1/ebus@3
ebus                      /pci@1f,0/pci@1,1/ebus@1
net2                      /pci@1f,0/pci@1,1/network@3,1
net                       /pci@1f,0/pci@1,1/network@1,1
ttya                      /pci@1f,0/pci@1,1/ebus@1/su@14,320010
ttyb                      /pci@1f,0/pci@1,1/ebus@1/su@14,300000
ok

hsc                    /pci@1f,0/pci@1,1/ebus@3/sysmgmt@14,600000
dload                     /pci@1f,0/pci@1,1/network@1,1:,
userprom1
/pci@1f,0/pci@1,1/ebus@1/flashprom@10,400000
systemprom                /pci@1f,0/pci@1,1/ebus@1/flashprom@10,0
pcic                      /pci@1f,0/pci@1/pci@1
pcib                      /pci@1f,0/pci@1,1
pcia                      /pci@1f,0/pci@1
ebus2                     /pci@1f,0/pci@1,1/ebus@3
ebus                      /pci@1f,0/pci@1,1/ebus@1
net2                      /pci@1f,0/pci@1,1/network@3,1
net                       /pci@1f,0/pci@1,1/network@1,1
ttya                      /pci@1f,0/pci@1,1/ebus@1/su@14,320010
ttyb                      /pci@1f,0/pci@1,1/ebus@1/su@14,300000
name                      aliases
```

4.2 Firmware Configuration Variables

This section provides some information on the CORE SRAM variables and the configuration variables. For a battery-less system, such as the Netra CP2160 board, the NVRAM functions as an SRAM. That is, the SRAM stores configuration variables while the system is powered-on, but when the system goes through a power cycle, the system flash retains the variable information and reloads the SRAM at boot-up.

4.2.1 Firmware CORE SRAM Variables

At start up, Firmware CORE defines a set of variables in the SRAM. These provide for controlling initialization and selecting the amount of testing required. These variables determine the following functions. At the CORE interface, type `print-nvram` and the fixed offset SRAM variables *similar* to the following will be displayed on the screen (see TABLE 4-3):

```
user-interface = 0
run-post       = ff
post-level     = 40
kernel         = FVM
trap-state     = 60
msg-verbosity  = 3
```

4.2.2 Firmware CORE Execution Control

The key combinations listed in TABLE 4-2 can be used to control the flow of execution at system boot. These key combinations must be pressed at Power-on.

TABLE 4-2 Key Sequences

Key combination	Result
Control-P	Skip POST
Control-U	Enter CORE user interface
Control-N	Set default SRAM configuration variables
Control-M	Turn on power on messages

The Netra CP2160 board supports the USB keyboard.

4.2.3 OpenBoot PROM Configuration Variables

Configuration variables are used by the OpenBoot PROM code and are stored in the system flash. The following is a sample of the output when the `printenv` command is entered at the `ok` prompt. The `setenv` command is used to modify the environment variables. The boot process is controlled by several variables. See TABLE 4-4. For values of each variable, refer to the *OpenBoot 4.x Command Reference Manual* (see Appendix D).

TABLE 4-3 SRAM Configuration Variables

Parameter	Value	Default Value	Description
`env-monitor`	disabled	disabled	Environment monitoring at OpenBoot PROM (enabled or disabled).
`warning-temperature`	70	70	Sets the CPU warning temperature
`shutdown-temperature`	80	80	Sets the CPU shutdown temperature
`critical-temperature`	75	75	Sets the CPU critical temperature
`diag-passes`	1	1	
`diag-continue?`	0	0	
`diag-targets`	4	0	
`diag-verbosity`	3	0	
`keyboard-click?`	false	false	If true, enable keyboard click
`keymap`			Key map for custom keyboard
`scsi-initiator-id`	7	7	
`#power-cycles`	1431655901	no default	Initialized in manufacture
`system-board-serial#`		no default	Initialized in manufacture
`system-board-date`		no default	Initialized in manufacture
`ttyb-rts-dtr-off`	false	false	If true, OS does not assert DTR and runs on TTYB
`ttyb-ignore-cd`	true	true	If true, OS ignores TTYB carrier-detect
`ttya-rts-dtr-off`	false	false	If true, OS does not assert DTR and runs on TTYA
`ttya-ignore-cd`	true	true	If true, OS ignores TTYA carrier-detect

TABLE 4-3 SRAM Configuration Variables *(Continued)*

Parameter	Value	Default Value	Description
ttyb-mode	9600,8,n,1,-	9600,8,n,1,-	TTYB (baud, #bits, parity, #stop, handshake)
ttya-mode	9600,8,n,1,-	9600,8,n,1,-	TTYA (baud, #bits, parity, #stop, handshake)
cpci-probe-list	0,1,2,3,4,5,6,7,8,9,a,b,..	0,1,2,3,4,5,6,7,8,9,a,b,..	Probe list for devices present on cPCI bus
pcia-probe-list	1	1	Probe list for devices present on internal PCI bus A
pcib-probe-list	1,2,3,4	1,2,3,4	Probe list for devices present on internal PCI bus B
mfg-mode	off	off	manufacturing test mode (leave off)
diag-level	max	max	Level of diagnostics to run (min or max)
watchdog-timeout	65535	65535	
watchdog-enable?	false	false	
fcode-debug?	false	false	
output-device	screen	screen	Console output device (usually screen, ttya or ttyb)
input-device	keyboard	keyboard	Console input device (usually screen, ttya or ttyb)
load-base	16384	16384	Base address where client image is loaded by OpenBoot PROM
auto-boot-retry?	false	false	
boot-command	boot	boot	Command that is executed if auto-boot? is true
auto-boot?	false	true	If true, boot automatically after power-on reset
watchdog-reboot?	false	false	If true, reboot after watchdog reset
diag-file			File from which to boot in diagnostic mode
diag-device	net	net	Device from which to boot
boot-file			File to boot (an empty string lets secondary boot choose default)
boot-device	disk net	disk net	Device from which to boot

TABLE 4-3 SRAM Configuration Variables *(Continued)*

Parameter	Value	Default Value	Description
local-mac-address?	false	false	If true, local-mac-address is used; else, whwtem-wide mac-address is used when booting over any network interface in this system
net-timeout	0	0	
ansi-terminal?	true	true	Not applicable
screen-#columns	80	80	Screen width in columns
screen-#rows	34	34	Screen height in rows
silent-mode?	false	false	If true, suppress messages related to clearing memory
use-nvramrc?	false	false	If true, execute commands in NVRAMRC during system start-up
nvramrc	″ebus2″ select-dev 000...		Contents of NVRAMRC
security-mode	none	no default	Firmware security level (none, command or full) none: no password required (default) command: all commands except for boot and go require password full: all commands except for go require password
security-password		no default	Firmware security password (never displayed)
security-#badlogins	0	no default	OpenBoot PROM internal use
oem-logo		no default	Byte array custom OEM logo (enabled by oem logo? true); displayed in hex
oem-logo?	false	false	If true, use custom OEM logo, else use Sun logo
oem-banner		no default	Custom OEM banner (enabled by oem-logo? true)
oem-banner?	false	false	If true, use custom OEM banner
hardware-revision	UUUUUUUU..	no default	Initialized in manufacture
last-hardware-update	UUUUUUUU..	no default	Initialized in manufacture

TABLE 4-3 SRAM Configuration Variables *(Continued)*

Parameter	Value	Default Value	Description
`diag-switch?`	true	false	If true, POST is executed when system is next powered
`auto-config-save?`	true	true	If true, NVRAM configuration variables are saved in flash
`post-on-sir?`	false	false	If true, execute post on softreset
`probe-delay?`	30	30	Defines number of seconds for which the host board waits before probing CPCI bus
`front-phy?`	true	true	If true, the board is recognized as a front-access system. If false, the board is recognized as a rear access system.

Note – *All numbers are HEX numbers.*

The `diag-switch?` and `diag-level` *variables listed in* TABLE 4-3 affect the path through the various embedded tests. TABLE 4-4 shows the effect of setting these variables.

BPOST is embedded within Firmware CORE and is executed when the OpenBoot PROM environment variable, `diag-switch?` is set to `true` and `diag-level` set to `min`. Similarly CPOST (and EPOST if it is present) is executed when `diag-level` is set to `max`. The permutations are shown in TABLE 4-4.

TABLE 4-4 OpenBoot PROM Environment Variable Settings for Executing the POST Modules

Module	diag-switch?* set:	diag-level* set:	Description
BPOST	false	X	NO messages are output to TTY
	true	min (0x20)	
	true	off (0x0)	Messages are output to TTY
CPOST	false	X	No messages are output to TTY
	true	max (0x40)	Runs after BPOST
	true	off (0x0)	Messages are output to TTY

TABLE 4-4 OpenBoot PROM Environment Variable Settings for Executing the POST Modules *(Continued)*

Module	diag-switch?* set:	diag-level* set:	Description
EPOST	false	X	No messages are output to TTY
	true	max (0x40)	Runs automatically after CPOST (if EPOST module is present)
	true	off (0x0)	Messages are output to TTY

* Firmware CORE variables *run-post* and *post-level* are equivalent to env. variables diag-switch? and diag-level respectively.

4.3 Firmware Memory Map

The satellite host board boots from the 1MB system flash PROM device which contains the Firmware CORE, Basic POST code, Comprehensive POST, and OpenBoot PROM. The contents map of this PROM is shown in FIGURE 4-2. User-developed code can also be programmed into the user flash memory space in the form of *dropins*. The system flash may be upgraded by running a program out of OpenBoot PROM—see Section 4.7, "SMC Firmware" on page 4-18. It is not otherwise accessible by the user.

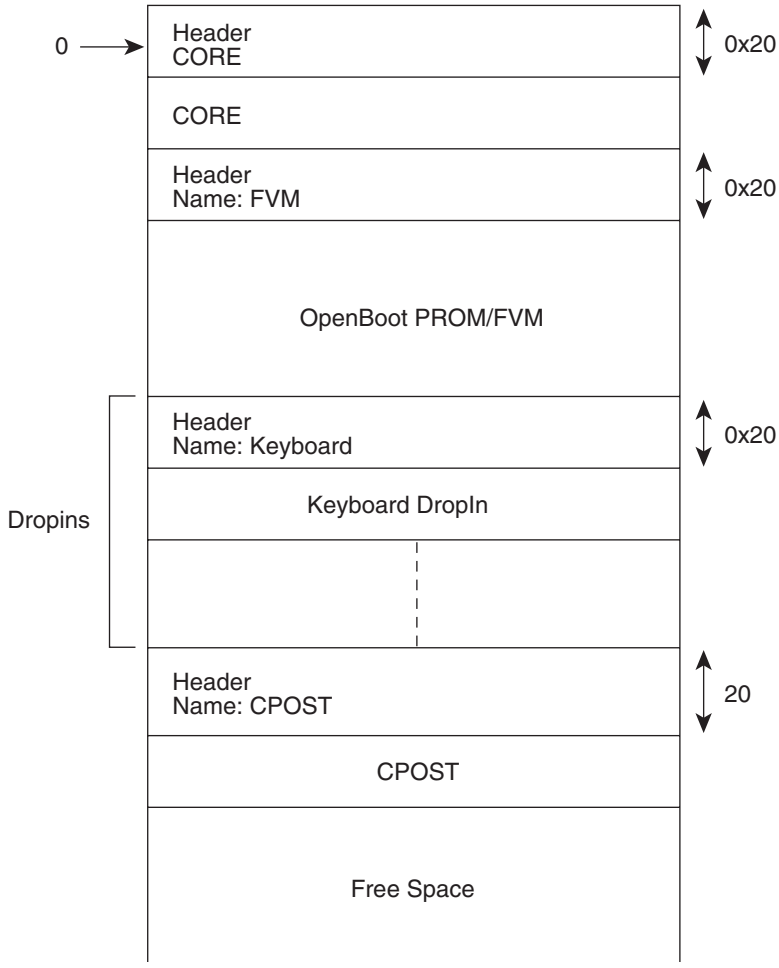


FIGURE 4-2 System Flash PROM Map

4.4 Firmware CORE Features

TABLE 4-5 lists the firmware CORE Commands that are run from the monitor. At the key sequence Control-U mode (see TABLE 4-2), you may type help to get all the supported commands such as in the example shown below.

TABLE 4-5 Monitor Commands CORE

Description of Task	CORE Monitor Command
To get this help	`help`
To allocate memory buffer	`malloc <size>`
To free memory buffer	`free <addr>`
To block copy memory	`bcopy <src> <dest> <#bytes>`
To dump memory	`dump <addr> <#bytes> [asi]`
To read an address	`[safe-]peek <addr> <1|2|4|8> [asi]`
To write to an address	`poke <addr> <1|2|4|8> <data> [asi]`
To update Flash PROM	`flash-update <dev> <file-path>`
To load a file	`load <device> <file-path> <addr>`
Jump to an address	`go <addr>`
Execute client	`execute [client-name]`
Print NVRAM data	`print-nvram`
Write to NVRAM variable	`set-nvram <variable-name|ID> <data>`
Read an NVRAM variable	`get-nvram <variable-name|ID>`
Delete an NVRAM variable	`delete-nvram <ID>`
Set NVRAM vars to default	`set-defaults`
Call a trap function	`trap <trap#> <par0> ... <par5>`
Soft Reset	`reset`
To change input device	`input-device <tty|kbd>`
To initialize PCI	`init-pci`
To show all pci devices	`show-pci-devs`
To show pci config space	`show-pci-space <bus#> <device#> <function#> <offset>`
To show pci nexus nodes	`show-nexus-nodes`

TABLE 4-5 Monitor Commands CORE *(Continued)*

Description of Task	CORE Monitor Command
To remove a pci device	`rm-pci-dev <device#>`
To add a pci device	`add-pci-dev <device#>`
To remove all pci devices	`rm-pci-devs`
To add all pci devices	`add-pci-devs`
To execute UI cmd in loop	`loop <count> <command>`

Note – All numbers are HEX numbers

4.5 USB Keyboard Support

The Netra CP2160 board supports USB keyboard only.

4.6 ASM Support at OpenBoot PROM

Advanced System Monitoring (ASM) is an intelligent fault detection system to increase uptime and manageability at OpenBoot PROM. The SMC module on the Netra CP2160 board, supports the temperature monitoring functions of ASM. ASM monitors the following at regular intervals at the `ok` prompt:

- CPU heat sink thermal sensor
- ENUM signal on the system host board
- PCI_RESET# polling on the satellite board

4.6.1 CPU Heat Sink Thermal Sensor

At the OpenBoot PROM level, when an over-temperature condition occurs, corresponding messages are displayed on the console. OpenBoot PROM displays the warning messages as soon as the board temperature reaches the warning temperature and is still below the shutdown temperature. The shutdown messages are displayed as soon as the board temperature reaches the shutdown temperature. The `warning-temperature` and `shutdown-temperature` are maintained in the

SRAM for the Netra CP2160 board (for warning and shutdown temperature values, see TABLE 4-3). Also, the `show-sensor` command at OpenBoot PROM displays the readings of all the temperature sensors on the board.

When the CPU temperature reaches the set warning temperature limit, the following message is displayed at the `ok` prompt at regular intervals

```
<<< !!! ALERT!!! Upper Non-critical - going high >>>
     The current threshold setting is:  < >
     The current temperature is      : < >
```

When the CPU temperature reaches the set shutdown temperature limit, the following message is displayed at the `ok` prompt at regular intervals::

```
<<< !!! ALERT!!! Upper Critical - going high >>>
     The current threshold setting is:  < >
     The current temperature is      : < >
```

The warning and shutdown temperature values provided are the OpenBoot PROM default values. A user can change these values by changing the corresponding SRAM variable values and resetting the system hardware or software.

```
ok setenv warning-temperature  <new_value>
ok setenv shutdown-temperature <new_value>
ok setenv critical-temperature <new_value>
ok reset-all
```

The `<new_value>` is a decimal value for a new temperature limit. The OpenBoot PROM then uses the new temperature limits after the system reset.

Caution – Be careful when setting the temperature parameters. Setting the `warning-temperature` and `shutdown-temperature` values too high will leave the system unprotected against overheating. Setting the temperature too low may cause the Netra CP2160 board to send error messages continuously.

4.6.2 PCI_RESET# Polling on the Satellite Board

The ASM also provides PCI-RESET# polling. ASM checks the status of the PCI_RESET# on the system board and enables the satellite board to respond accordingly. For example, a hot-swap cPCI chassis containing a system host board and a few Netra CP2160 satellite boards that are all at the `ok` prompt: If the

PCI_RESET# is reasserted by the system board, then the assertion is polled by the SMC on the satellite boards. The satellite board then does an automatic `reset-all` on itself.

4.7 SMC Firmware

The field upgradeable SMC firmware supports features such as Netra CP2160 board resources, temperature monitoring, control of the power module, IPMI communication with other boards, PCI reset modes of operation, hot-swap capability and watchdog timer heartbeat mechanism. The SMC firmware also has its own built-in self test at power up. The SMC consists of DS80CH11, which is an 8051 compatible chip and the WS833, the memory chip. Inside WS833, there are the main flash and the boot flash and SRAM for data storage. The host CPU sends commands and data to SMC via the EBus. For more details on the SMC subsystem please see Section 5.6, "System Management Controller" on page 5-24.

The SMC architecture allows the update of the SMC firmware. SMC firmware is only updated from the OpenBoot PROM. This feature is used to modify SMC firmware during a field upgrade, for fixing bugs, adding enhancements/new features, or providing special code for a specific OEM customer.

The SMC is capable of performing a flash update on both, main and boot flash. The main flash can flash update the boot flash, and the boot flash can flash update the main flash. The boot code contains the bare minimum code to be able to let the system boot to `ok` prompt in the event of the main flash failure, and be able to switch from boot flash to main flash for execution. Therefore any attempt to perform flash update to the boot flash is considered risky and should not be done too often.

The CORE/OpenBoot PROM code has support for recovery in case of SMC flash update failure. When it detects that SMC is running from boot code, it automatically goes to the `ok` prompt, and the user can do a flash update. Any other commands sent to SMC will not be allowed at this time.

For full details on SMC firmware and detailed commands, please refer to the Netra CP2160 board web site:

`http://www.sun.com/products-n-solutions/nep/hardware/boards/cp2160/`

Note – Due to interdependency between OpenBoot PROM CORE, SMC and hardware, the user must take into account compatibility between various parts of the system among different version numbers when performing flash update. Please refer to the release note at the product web site for the latest information and compatibility between firmware and hardware components.

4.7.1 SMC Firmware Reset Modes for System Slot and Peripheral Slot Operations

This section provides information on the various modes of reset available on the Netra CP2160 board when used in the different roles and CompactPCI slots. TABLE 4-6 describes the available modes of operation in response to a reset request on the CompactPCI backplane. Determination of system or peripheral/satellite operation is made from the state of the cPCI backplane SYSEN# signal as per the *PICMG 2.0 R3.0 Specification*. The RESET# signal affects only the PCI component of the cPCI bus. Please refer to the Netra CP2160 board web site for detailed information on reset modes:

`http://www.sun.com/products-n-solutions/nep/hardware/boards/cp2160/`

TABLE 4-6 Reset Operating Modes

Reset Mode	System Slot	Peripheral / Satellite Slot
11	Standard system slot operation -- the board generates normal RESET# and PCI signalling for the backplane in its role as system controller	Backplane reset is propagated to the UltraSPARC-IIi 21555 NTB and other reset table components on the board. This results in a complete reset of the UltraSPARC section of the board.
22	Standalone mode - The board asserts a constant RESET# but no PCI clocking for the cPCI bus, and does not respond to any PCI signalling on the backplane	Standalone mode - The local cPCI bridge is held in reset, isolated from the cPCI bus. the board does not respond to any PCI signalling on the cPCI bus.
66*	Standard system slot operation -- the board generates normal RESET# and PCI signalling for the backplane in its role as system controller	Standalone mode - The local cPCI bridge is held in reset, isolated from the cPCI bus. The board does not respond to any PCI signalling on the cPCI bus.

* Reset Mode 66 is the default setting for the Netra CP2160 boards.

Users may reprogram the operating mode from the OpenBoot PROM prompt, then reboot (power cycle) the entire system in order for the new reset modes to take effect.

Caution – Some of these modes may be incompatible with various PICMG specifications, and customers may use these modes at their own risk.

4.7.2 SMC Configuration Block

The SMC power-on behavior and other attributes are stored in an 16-byte configuration block. This configuration block is stored in an accessible Serial I^2C EEPROM. In the absence of this configuration block, SMC boots up in a default mode. For this purpose, at the OpenBoot PROM level there are two commands: `setsmcenv` and `printsmcenv` in the SMC node. The `setsmcenv` command is used to set paramters in the configuration block of SMC. The `printsmcenv` command prints the value of the parameters in the SMC configuration block.

4.7.2.1 Command Usage Detail

To change the settings on the configuration block, read the block using the `printsmcenv` command. If you want to change the settings, use the setsmcenv command to change the SEEPROM configuration block. Some examples are given below:

Example:

```
ok printsmcenv
config-version      : 4
backplane-type      : 1
reset-mode          : 66
sir-xir-enable      : 2
byte5               : 0
chassis-type        : 0
flash-device        : 0
byte8               : 0
ha-signal-handler   : 0
poweron-vector      : 0
ipmi-checksum-ctlr  : 0
byteC               : 0
byteD               : 0
byteE               : 0
byteF               : 0
byte10              : 0
ok setsmcenv reset-mode 66
ok setsmcenv backplane-type 1
```

Note – Each setting on the configuration block can change the behavior of the board significantly. For further information on how to change the settings, contact your local Sun support team. Please refer to Netra CP2160 CompactPCI Board Product (P/N 816-5761).

During OpenBoot PROM start up sequence, and before the PCI probe, OpenBoot PROM checks for a valid SMC configuration block. If it does not find a valid configuration block (i.e configuration version is not equal to 1), then OpenBoot PROM instructs the SMC to program the configuration block with the following default settings:

```
Config version:   1
Backplane info:   0
Reset mode:       66
SIR & XIR:        2
Health control:   0
Health status:    0
byte 7:           0
byte 8:           0
```

4.8 Firmware Diagnostics

The firmware contains a comprehensive set of hardware diagnostic modules that provide tests for most situations. FIGURE 4-1 shows the control-flow relationship of the diagnostic modules with the system firmware. SunVTS can be executed from within the Solaris software if more tests are required. For more information, see Section 3.7.2, “Downloading and Installing SunVTS” on page 3-17.

The firmware diagnostic modules are:

- Basic POST (BPOST)
- Comprehensive POST (CPOST) -- optional
- Extended POST (EPOST) -- OEM supplied dropin
- OBDiag

The firmware diagnostics cover address and data bits on all system buses and exercise the function of the major hardware resources on the board.

Diagnostics can be performed at OpenBoot PROM level by using the `obdiag` command, or by typing individual test commands at the `ok` prompt. These test suites are similar to those in earlier OpenBoot PROM versions but they are comprised of dropins that can be placed by the user. See the reference to the *OpenBoot 4.x Command Reference Manual* listed in Appendix D.

4.8.1 Setting Diagnostic Levels

The user interface in terms of running POST at minimum or maximum remains the same. BPOST is embedded within Firmware CORE and is executed when the OpenBoot PROM environment variable, `diag-switch` is set to `true` and `diag-level` set to `min`. Similarly, CPOST (and EPOST if it is present) is executed when diag-level is set to `max`. The permutations are shown in TABLE 4-4.

CPOST and Extended POST are clients of Firmware CORE.

4.8.2 Basic POST (BPOST)

BPOST is integrated into Firmware CORE. It can provide on-demand diagnostic services in response to IPMI requests from the System Management Bus.

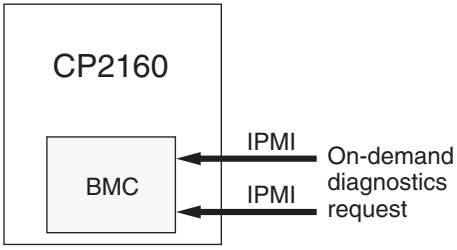


FIGURE 4-3 Basic POST Services

BPOST consists of two parts:

The first part of BPOST executes from flash memory. It is designed to validate enough of the system resources to be able to run Firmware CORE in main memory (System RAM). If this test phase is passed, BPOST is also copied into system RAM. BPOST runs when the `diag-switch?` is set to `true` (see TABLE 4-4).

The part of BPOST executed from flash includes basic tests for the following:

- SRAM
- I-cache and D-cache
- MMU
- FPU
- L2-cache tag and RAM
- Data lines
- CORE memory

The second part of BPOST is performed after Firmware CORE is copied into main RAM. This part of BASIC POST executed from RAM includes:

- Memory address line test; this test assumes that the CPU, MMU, and FPU are functional.
- ECC block memory test; verifies main memory with block write and ECC checking. This test assumes that the CPU, MMU, and FPU are functional.

4.8.3 Comprehensive POST (CPOST)

Comprehensive POST (CPOST) is a client of Firmware CORE. It is a dropin module invoked by Firmware CORE and contains enhanced diagnostics for the CPU and on-board devices.

The execution of CPOST is optional and can be selectively controlled by an environment variable—see TABLE 4-4. CPOST runs after BPOST. To run CPOST, set the environment variables `diag-switch?` to `true` and diag-level set to `max`

CPOST tests comprise:

- Memory stress test; advanced main memory test
- Basic PBM, IOMMU test
- Basic Advanced PCI Bridge APB test
- PCI/EBus/Ethernet/SuperI/O tests
- System Management Controller test

After CPOST it undergoes a software reset which sends it back to Firmware CORE. From this point, execution enters OpenBoot PROM (since diagnostics are only executed at power on reset).

4.8.4 OpenBoot PROM On-Board Diagnostics

The OpenBoot PROM on-board diagnostics reside in the OpenBoot PROM dropin. These diagnostics are described fully in the *OpenBoot 3.x Command Reference Manual*—see Appendix D.

To execute the OpenBoot PROM on-board diagnostics, the system must be at the ok prompt. The OpenBoot PROM on-board diagnostics comprise:

- watch-clock
- watch-net and watch-net-all
- probe-scsi
- test *device path*
- test-all

4.8.5 OpenBoot Diagnostics

The OpenBoot Diagnostics are an enhancement of the traditional system tests. They reside in Forth script in a dropin and are invoked with an interactive tool that is started from the ok prompt by typing **obdiag**.

When OpenBoot Diagnostics is started, the following menu is displayed:

```
ok obdiag

1 ebus@1                2 ebus@3                3 flashprom@10,0
4                       5 network@1,1           6 network@3,1
flashprom@10,400000     8 usb@3,3
7 usb@1,3

Commands: test test-all except help what printenvs setenv versions
exit
```

When at the obdiag prompt, typing test-all would display a printout similar to the following:

```
obdiag> test-all
Hit the spacebar to interrupt testing
Testing /pci@1f,0/pci@1,1/ebus@1..................................... passed
Testing /pci@1f,0/pci@1,1/ebus@3 ..................................... passed
Testing /pci@1f,0/pci@1,1/ebus@1/flashprom@10,0 ...................... passed
Testing /pci@1f,0/pci@1,1/ebus@1/flashprom@10,400000 ................. passed
Testing /pci@1f,0/pci@1,1/network@1,1 ................................ passed
Testing /pci@1f,0/pci@1,1/network@3,1 ................................ passed
Testing /pci@1f,0/pci@1,1/usb@1,3 .................................... passed
Testing /pci@1f,0/pci@1,1/usb@3,3
```

CHAPTER 5

Hardware and Functional Description

This chapter contains the following sections:

5.1 Summarized Physical Description

The Netra CP2160 board is a 6U-sized CompactPCI circuit card with CompactPCI connectors J1 and J2 for PCI, and J3 and J5 for I/O. J4 is not fitted to the board. See FIGURE 5-1 and FIGURE 5-2 for top and solder-side views of the board.

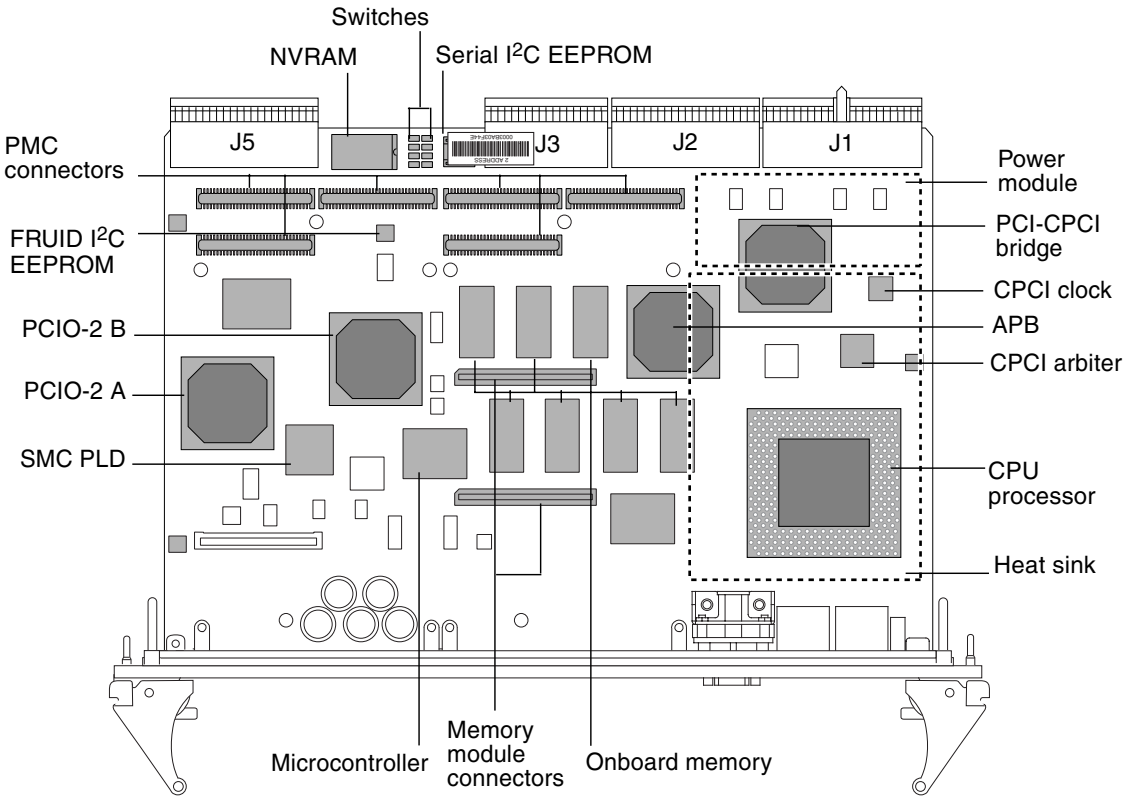


FIGURE 5-1 Netra CP2160 Board Layout

Note – The heat sink and the power module are shown as dotted lines in this diagram to illustrate the components on the board that lie beneath these devices.

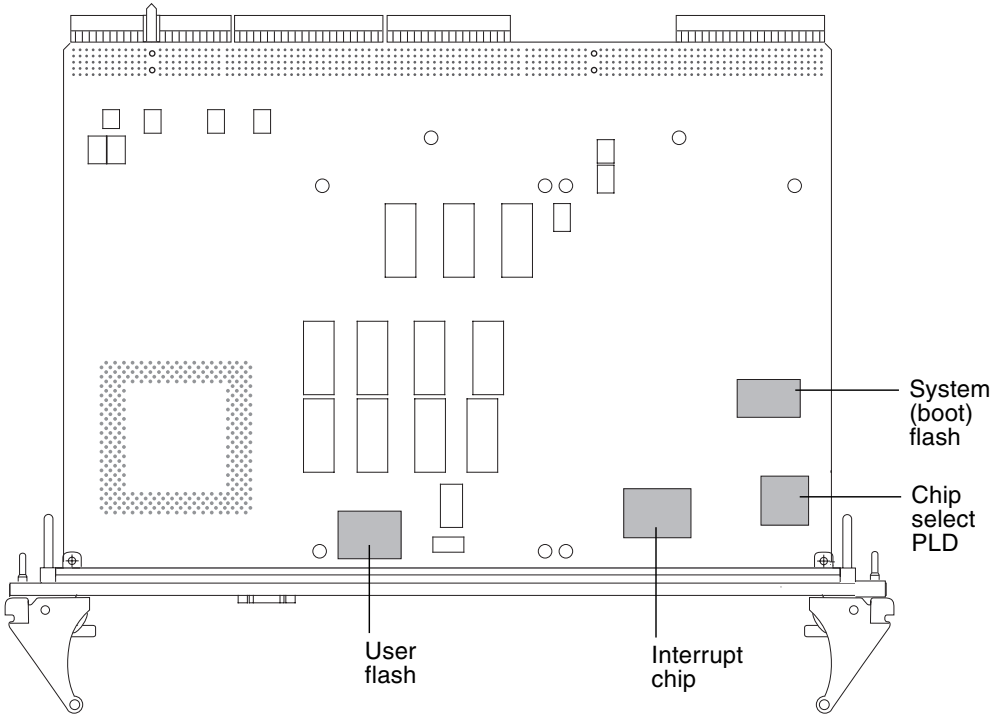


FIGURE 5-2 Typical Netra CP2160 Board – Solder Side

A Netra CP2160 board functions as a satellite board or as a system host board. The board has the following I/O access:

- Through the two Ethernet ports and one serial port on the front panel.
- Through the CompactPCI backplane: a transition card must be connected to provide rear connector access for two serial ports, two Ethernet ports and a USB port. Sun Microsystems offers a compatible XCP2160-TRN transition card (375-0120-*xx*). This card is recommended for use, but OEM customers may design their own transition cards for use instead.
- Through one or two PMC card interfaces provided to accept up to two IHV-supplied PMC I/O cards.
- Through one or two IHV-supplied PIM modules that can duplicate front-panel PMC I/O ports. The PIMs attach to interfaces on a transition card and bring the ports out to its panel at the rear of the enclosure. See Section 5.4.4, "PMC and PIM Interface" on page 5-16 for further details.

The front panel of the Netra CP2160 board has two PMC module slots, two Ethernet ports, a serial port and the following reset pushbuttons and status LEDs:

- ABORT – pushbutton (XIR)

- RESET – pushbutton (POR)
- USER – orange/green
- READY – green
- Blue LED for hot-swap

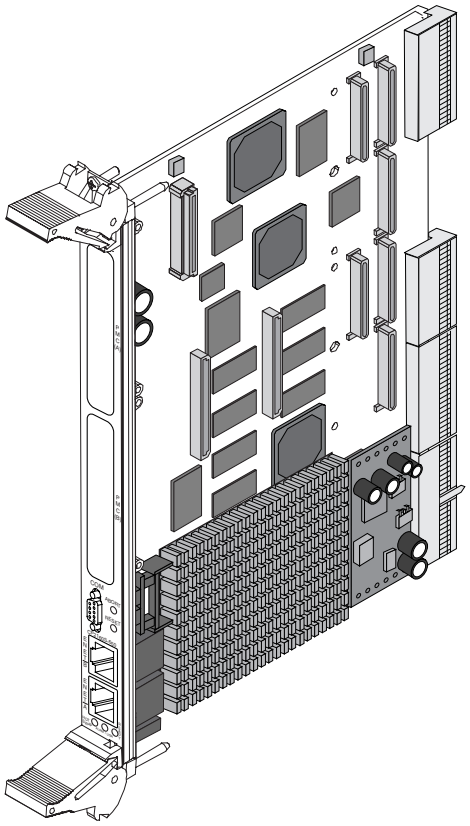


FIGURE 5-3 Typical Netra CP2160 Board Assembly With Heat Sink

5.2 Detailed Description

A simplified schematic diagram is shown in FIGURE 5-4.

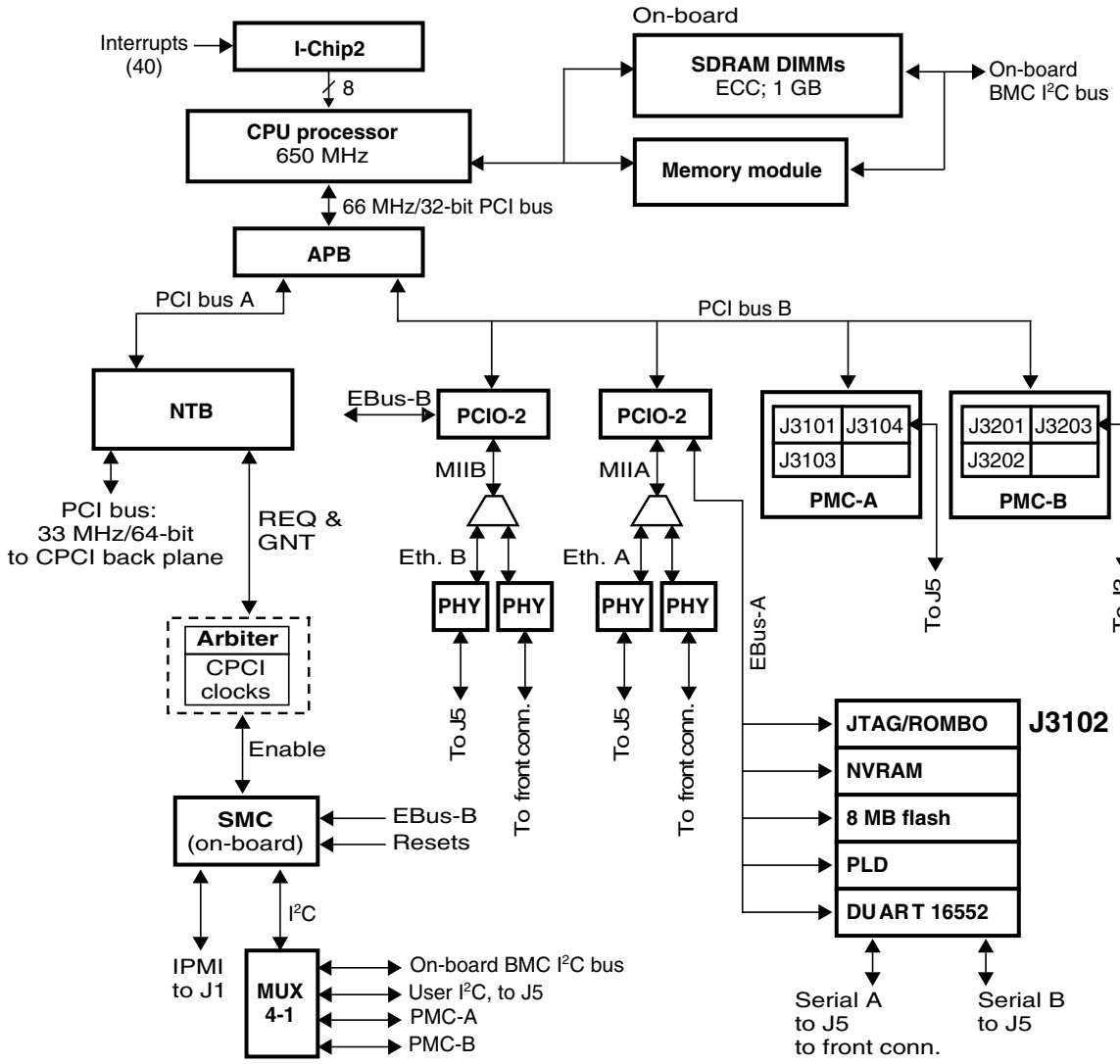


FIGURE 5-4 Netra CP2160 Board Functional Block Diagram

The L2-cache is integrated into the UltraSPARC IIi processor package. This processor is supported by SDRAM memory that is soldered onto the board and is also available in plug-in module form.

Apart from incoming interrupts, the processor handles all I/O through its built-in 66 MHz, 32-bit PCI bus interface. This interface is used to connect to a Sun Advanced PCI Bridge (APB) that services two 33 MHz 32-bit downstream interfaces, PCI bus A and PCI bus B.

PCI bus A connects to a nontransparent PCI bridge (21555 NTB), which services the principal PCI bus connection to the CompactPCI backplane through its connectors J1 and J2. In a system host role, a PCI bus arbiter provides CompactPCI bus arbitration signals for the CPCI backplane bus. It also supplies clocks for the CPCI bus. The arbiter is only active if the system host board is installed into the system slot and functions in a system host role. When the board functions as a satellite board, the CPCI bus arbiter is disabled by the system management controller (SMC). (See Section 5.4.3.1, "Arbitration in System Controller Role" on page 5-15 for details).

PCI Bus B connects the APB to each of two PCIO-2 South Bridge packages, PCIO-2 A and PCIO-2 B. See Section 5.4.2, "PCIO-2 Devices and EBus Paths" on page 5-13 for more details.

In addition, The PCI bus B from the APB connects to each of two 33 MHz, 32-bit PMC interfaces on the host board. See Section 5.4.4, "PMC and PIM Interface" on page 5-16 for more detail.

The SMC connects to:

- The bus arbiter and clock generator, enabling it to control CompactPCI bus arbitration, clock, and reset functions.
- The on-board I^2C bus, enabling it to communicate with sensors and controls.
- The User IPMI bus, enabling user management of other entities in the system. Peripheral hot-swap control is also enabled through this path.
- The power module.

The SMC controls the startup of the board, because it activates the power module and can control the system reset signals. In addition, it handles hot-swap signals from the CompactPCI backplane, for example: ENUM, HEALTHY, BD_SEL, and PCI_RST (the PCI reset signal). See Section 1.3, "Hot-Swap Support" on page 1-10 for more information on hot-swap.

The block schematic diagram of FIGURE 5-5 shows a more detailed block diagram of the Netra CP2160 board.

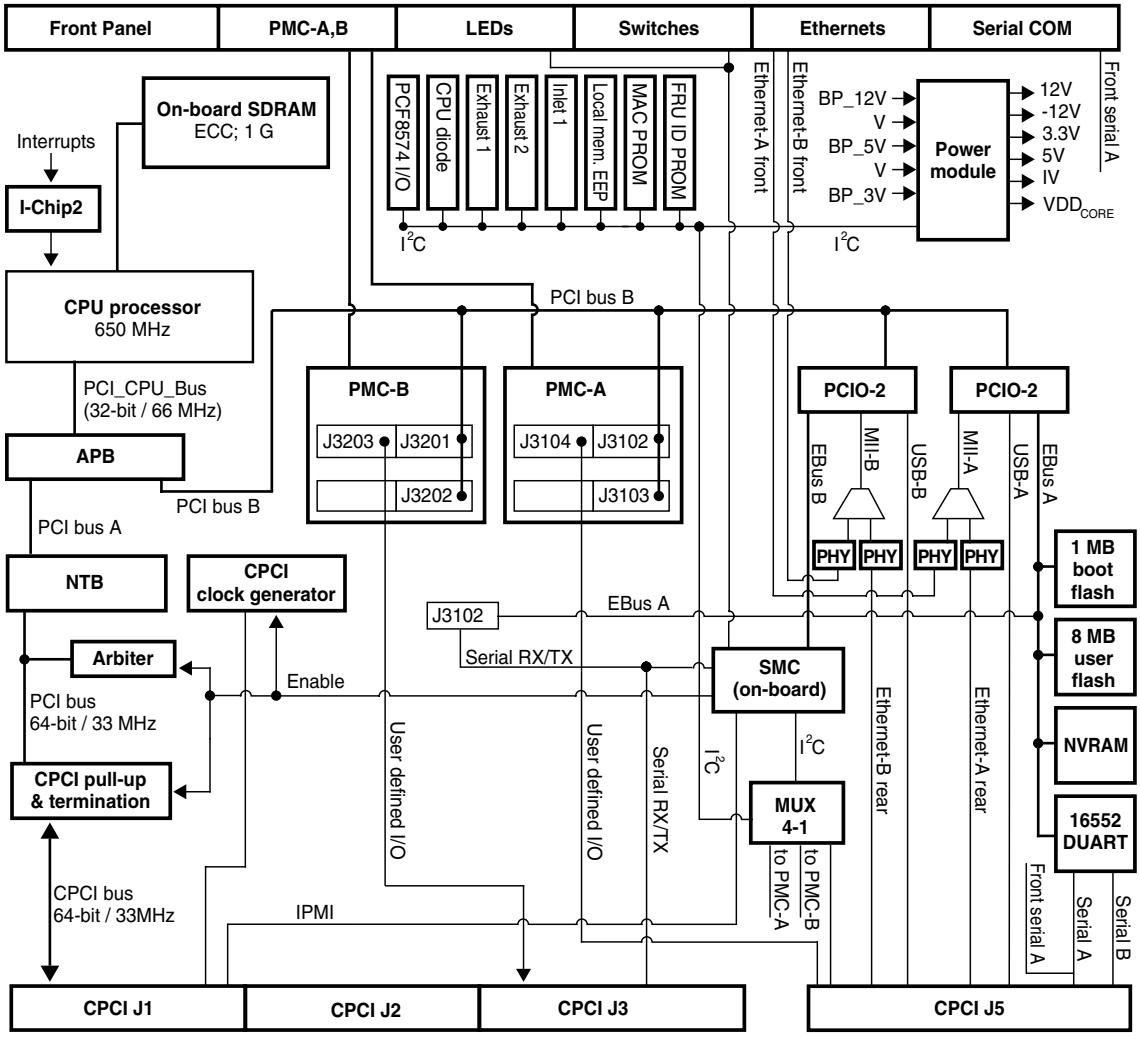


FIGURE 5-5 Netra CP2160 Board Detailed Block Diagram

5.3 CPU and Main Memory Subsystems

This section describes the UltraSPARC-IIi processor and additional memory on the Netra CP2160 boards. FIGURE 5-6 shows the UltraSPARC IIi interfaces.

5.3.1 UltraSPARC IIi Processor

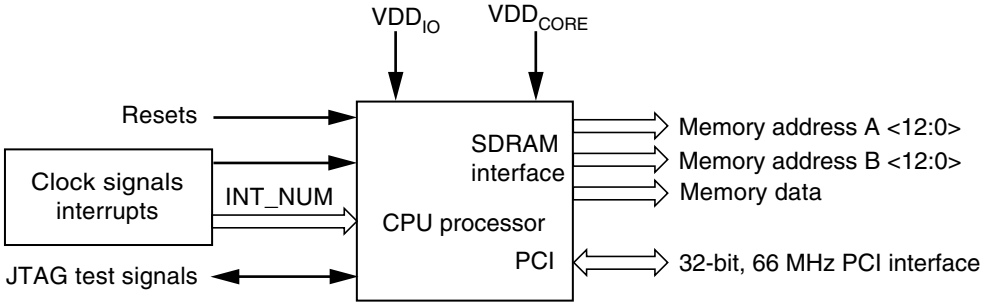


FIGURE 5-6 UltraSPARC IIi Interface

The Netra CP2160 board uses the UltraSPARC IIi 650 MHz processor. The processor is housed in a 370-pin ceramic pin grid array (PGA) package. It typically dissipates no more than 25 W at 650 Mhz.

The UltraSPARC IIi processor is directly connected to the board SDRAM through a 72-bit ECC path. Dual address buses reduce capacitive loading and increase the memory density beyond that of unbuffered devices.

The CPU connects to the APB by means of a 32-bit, 66 MHz PCI interface which the APB in turn translates to two downstream 33 MHz PCI buses.

The UltraSPARC processor begins execution from a fixed image in a PROM that lies on EBus A. The processor accesses this EBus in a boot path that automatically includes the APB, PCIO-2 A (a South Bridge), and EBus A.

Processor resets are received from the system management controller (SMC). See Section 5.7, “Resets” on page 5-28 and FIGURE 5-20 for more detail.

The various interrupts on the board are prioritized and encoded by the I-chip2 to appear at the UltraSPARC IIi processor as 6-bit parallel data. See Section 5.7, “Resets” on page 5-28 for more information.

The processor I/O is run at a fixed VDDIO of 3.3V but the core voltage, VDDCORE, is adjustable and configured according to CPU speed, typically in the range of 1.3 V to 1.9 V.

JTAG/Test signals are available for use in boundary scan diagnostics.

5.3.2 Memory Address Mapping

The UltraSPARC IIi L2 cache megacell reserves a 2 GB region for cacheable main memory. The memory databus width and the module databus width are of equal size (64-bit data plus 8 bit ECC) so memory modules can be installed in mixed sizes.

The UltraSPARC IIi Address Data Generation Logic (ADGL) logically maps modules according to their size, rather than their physical location. The largest sizes are mapped to the lowest address ranges. Where modules of identical size are present, the lower slot number is mapped to the lower address range.

FIGURE 5-7 shows a memory mapping example.

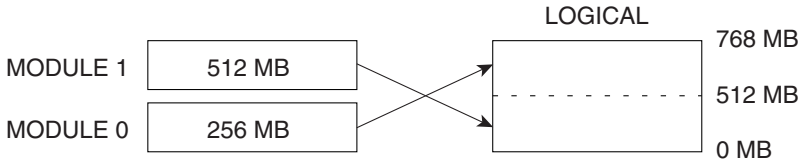


FIGURE 5-7 Memory Mapping Example

5.3.3 SDRAM Memory

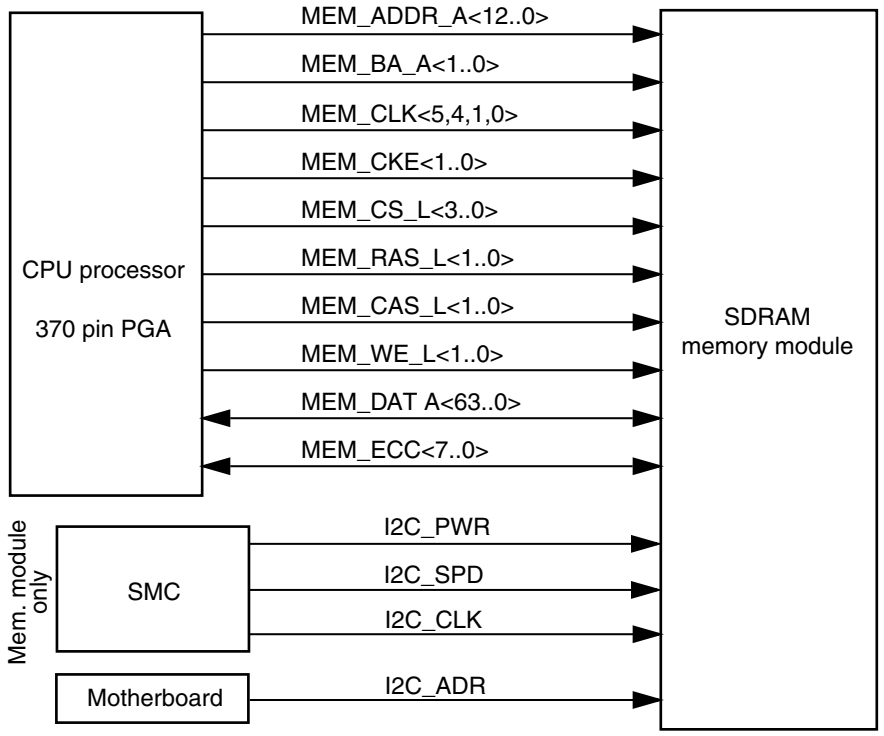


FIGURE 5-8 SDRAM Memory Interface

The UltraSPARC IIi 650 MHz processor connects directly to the memory with a 72-bit ECC data bus. The memory can be either on-board SDRAM only or composed of an additional mezzanine memory module.

Each mezzanine memory module has two 100-pin male connectors on its bottom surface—these plug into corresponding female connectors on the system board. No more than one additonal memory modules may be added to the 1 Gbyte on-board memory.

Each module is equipped with a temperature sensor and a serial EEPROM device containing 256 bytes of presence detect data. The double size module (if used) also contains a PLL, which generates eight clock signals. Both the temperature sensor and the serial EEPROM are accessed using the two pin I^2C protocol.

The memory block, whether on-board or a module, provides non-volatile serial memory to enable the Serial Presence Detect function. This memory can be interrogated by the SMC through the I^2C interface.

5.3.4 Memory Components

This section describes additional memory available on the Netra CP2160 boards.

5.3.4.1 System (Boot) Flash Memory

The system flash resides in 1 Mbyte of space. It contains Common Operations and Reset Environment (CORE) firmware, Comprehensive POST, and OpenBoot PROM boot code. The system flash may be upgraded by running a program out of OpenBoot PROM or executing a Solaris software script. If the system flash becomes corrupted, contact your nearest Field Application Engineer.

5.3.4.2 User Flash Memory

The board is equipped with 8 Mbyte of user flash memory. You may use the flash memory for various purposes such as storage for RTOS, user data storage, OpenBoot PROM information, or to house dropins. Dropins simplify customizing a system for the user.

A userflash switch SW2501 determines whether the userflash is detected during OpenBoot PROM boot and whether it is write enabled (see Section B.4, “Switch Settings” on page B-14).

5.3.4.3 NVRAM

The Netra CP2160 board does not have a battery back-up for the NVRAM. The NVRAM on this board functions as SRAM.

These boards use an 8K-bit X 8 timekeeper SRAM (NVRAM) package. This component provides:

- A time-of-day (TOD) real-time clock.
- 8 Kbyte storage for environment variables, user modifiable. The Ethernet address and Host ID are stored in the system flash. These values are copied to the SRAM when the system is powered-on.
- On firmware boot up, the Ethernet address stored in the SRAM is compared against the backup copy stored in the serial I^2C EEPROM on the Netra CP2160 board and the SRAM is updated if it differs from the backup copy.

5.3.4.4 Serial I^2C EEPROM

This device stores the backup copy of the board MAC address and Host ID in a removable serial EEPROM that is accessible through the I^2C bus. This data is downloaded to the SRAM at the OpenBoot PROM level.

5.3.4.5 FRU ID I^2C EEPROM

The FRU ID I^2C EEPROM chip stores manufacturing-related information of the Netra CP2160 board This information is useful only when the Netra board is being serviced.

See Appendix C for details on accessing the FRU ID information for the board.

5.4 Bus Subsystems

There are four PCI buses on the board: three internal buses and the external CompactPCI bus that is driven to and from the backplane. One of the internal PCI buses, PCI bus B, is bridged to two lower-speed buses EBus A and EBus B. PCI bus A communicates with the CompactPCI backplane through the nontransparent PCI-to-PCI bridge (21555 NTB). This arrangement is shown in FIGURE 5-9.

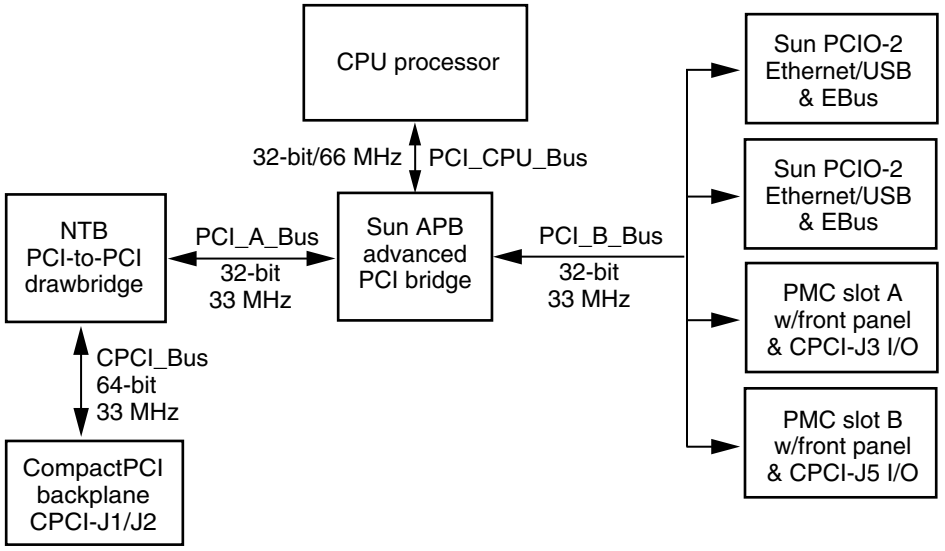


FIGURE 5-9 Netra CP2160 Board PCI Bus Interface, 33MHz CompactPCI Bridge

5.4.1 APB PCI Bus Interfaces

The UltraSPARC IIi CPU has an integrated 32-bit/66 MHz PCI bus interface. The Advanced PCI Bridge—acting as a North Bridge—splits this bus into two 32-bit/33 MHz PCI buses. Of these, the PCI A bus connects to the PCI non-transparent bridge which forms the interface to the CompactPCI backplane. The PCI B bus connects to two PCIO-2 bridges. Each of these bridges carry an EBus and peripheral interfaces at their other end.

5.4.2 PCIO-2 Devices and EBus Paths

The two PCIO-2 bridges connect between the APB PCI Bus B and their EBus and peripheral interfaces at their other end. Each of these bridges carry one EBus interface. The EBus interfaces are used to interface slower internal peripherals.

EBus A coming from PCIO-2 A :

- System Flash EEPROM. The UltraSPARC IIi processor accesses system flash EPROM through the APB and PCIO-2 A to boot from location 0xF0000.0000.
- User flash EPROM
- NVRAM

- Main PLD, which provides EBus decodes for chip select and CompactPCI arbiter control logic.
- Serial I/O through a dual universal asynchronous receiver/transmitter (DUART) device which uses an RS232 transceiver device to support two independent RS232 style serial ports. The RS232 level signals feed to the XCP2160-TRN transition module through the CPCI J5 connector.

EBus B coming from PCIO-2 B :

- System management controller (SMC). This path is the primary means of communication between the UltraSPARC IIi host and the SMC.

In addition, PCIO-2 A supports the MII Ethernet A port and USB A port. PCIO-2 B supports the MII Ethernet B port and USB B port.

5.4.3 CompactPCI Bus

The nontransparent bridge (NTB), in this case the Intel 21555 device, connects the 32-bit/33 MHz internal PCI bus A to the 64-bit/33 MHz CompactPCI backplane bus through CompactPCI connectors J1 and J2. This interface conforms to the PICMG 2.0 R3.0 CompactPCI Specification. FIGURE 5-10 shows the CompactPCI bus interface.

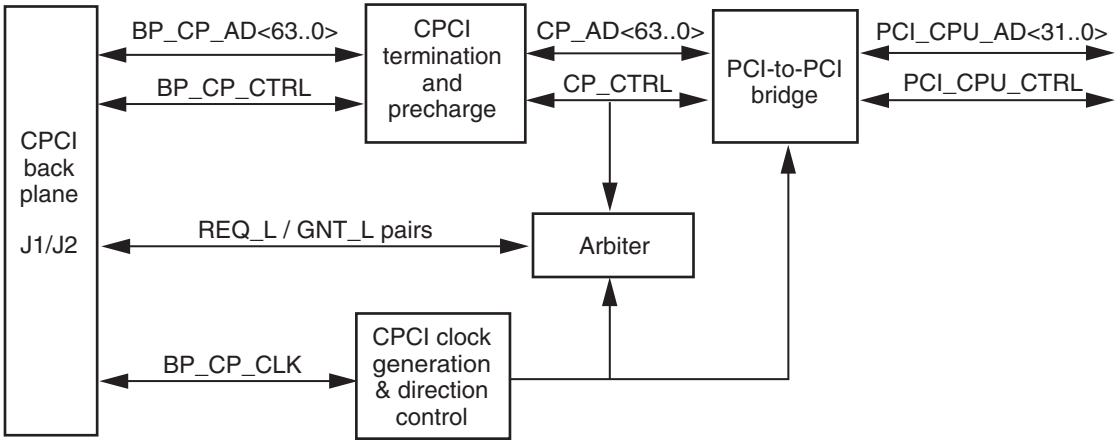


FIGURE 5-10 CompactPCI Bus Interface

The arbiter—only used when the board functions in a system host board role—provides for orderly sharing of the CompactPCI bus among potential bus masters, or *initiators*. When the board performs in a system host board role, PCI clocks sourced from a clock generator on the board are driven to a CompactPCI CLK bus signal to all slots on the CompactPCI backplane.

5.4.3.1 Arbitration in System Controller Role

The Netra CP2160 board can be used as a system controller board or as a satellite board. When the Netra board is a system controller board, the arbiter is enabled by the SMC. When the Netra board is a satellite board, the arbiter is disabled by the SMC through a control signal (signal SYS-EN on J2/C2).

FIGURE 5-11 and FIGURE 5-12 illustrate the signal flows for the two board operations.

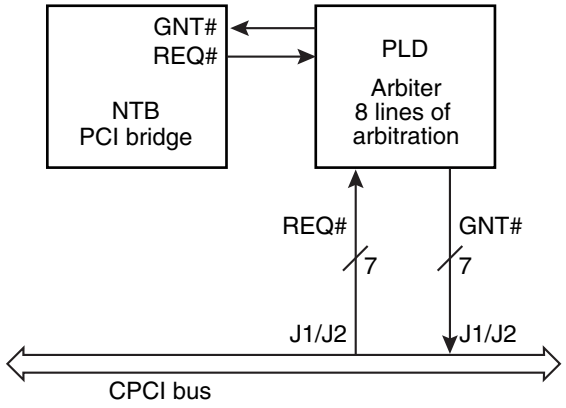


FIGURE 5-11 Netra CP2160 Board System Controller Board: REQ#/GNT# Signal Flow

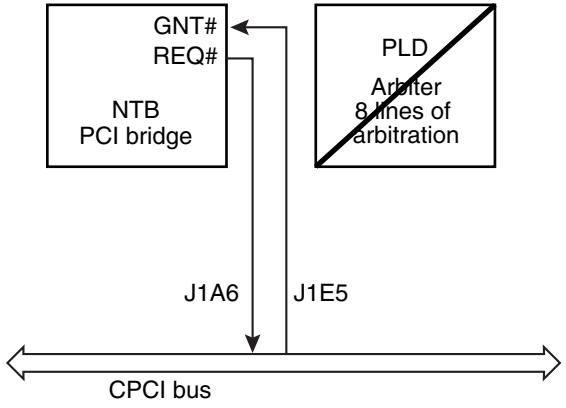


FIGURE 5-12 Netra CP2160 Board Satellite Board: REQ#/GNT# Signal Flow

When the Netra CP2160 board is operating as a satellite board, the arbiter is disabled (through a control signal from the SMC module). When disabled, the arbiter tristates REQ1# through REQ6# and GNT1# through GNT6# and pulls them to a known state.

The multiplexing, switching, or logic used to control the flow of the arbiter signals comply with all requirements of the CPCI specification, notably the requirements for single loads and stub length.

5.4.4 PMC and PIM Interface

The PCI mezzanine card (PMC) interface is defined by IEEE and PICMG standards:

- IEEE P1386, presently in draft form, defines the Common Mezzanine Card (CMC) mechanical profile (*common* because this definition, for example, can also apply to a VME rendering)
- P1386.1 defines the PCI electrical interface through its connectors Pn1/Jn1 through Pn4/Jn4
- PICMG 2.3 R1.0, *PMC on CompactPCI Specification* maps the PMC signals from the Jn1 through Jn4 connectors on the CompactPCI board through the CompactPCI backplane connections. In the case of the 6U products discussed here, these connections are routed to CompactPCI J3 and J5 connectors.

The PMC interface enables you to use Independent Hardware Vendor (IHV) PMC to implement additional I/O from the host at the system integration level.

The number of PMCs that can be used with the Netra CP2160 board varies according to the size of modular memory installed on the board. Refer to TABLE 5-1 for details.

TABLE 5-1 PMC Slots Available

Memory Modules Installed	Number of PMC Slots Available
No modular memory installed	Two
Single-wide module installed	One
Double-wide module installed	Zero

A Sun XCP2060-TRN I/O transition card fitted to the rear of the backplane provides slots for PIM cards. A PIM card enables rear I/O functions when paired with a PMC card installed on the front panel of the board.

A PIM must have a corresponding PMC in the front slot because the PMC board performs an adapter function between the PCI bus B and the user I/O signals passed through J5 to the PIM slot on the transition card. When a PMC that has a front-panel connector is used with a PIM, jumpers are typically set to disable its front I/O operation.

FIGURE 5-13 illustrates the interconnection between PMC and PIM slots for installed PIMs.

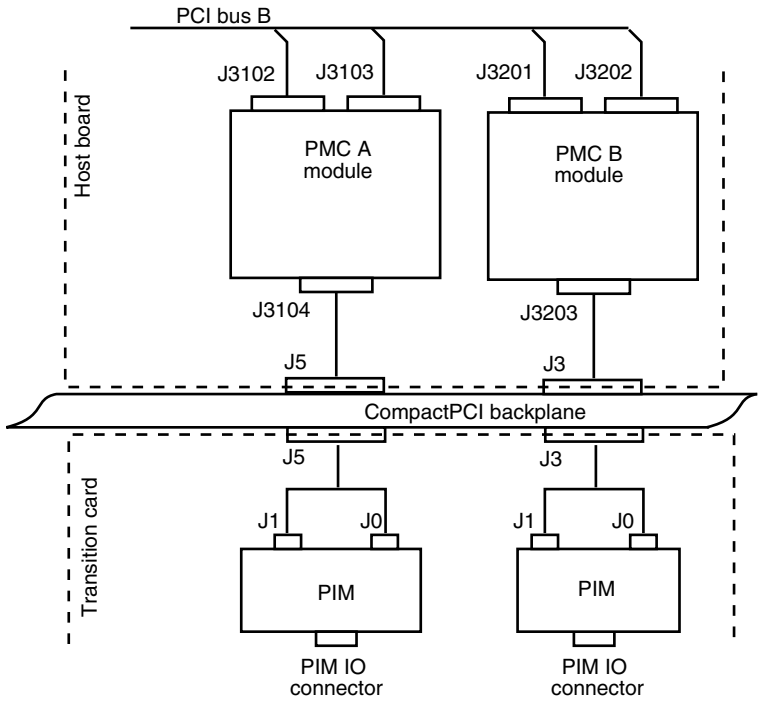


FIGURE 5-13 PIM Installation Configuration

FIGURE 5-14 shows the PMC A and card attachment to a Netra CP2160 board. There is a second PMC connector, PMC B, adjacent to the first (see FIGURE 5-15).

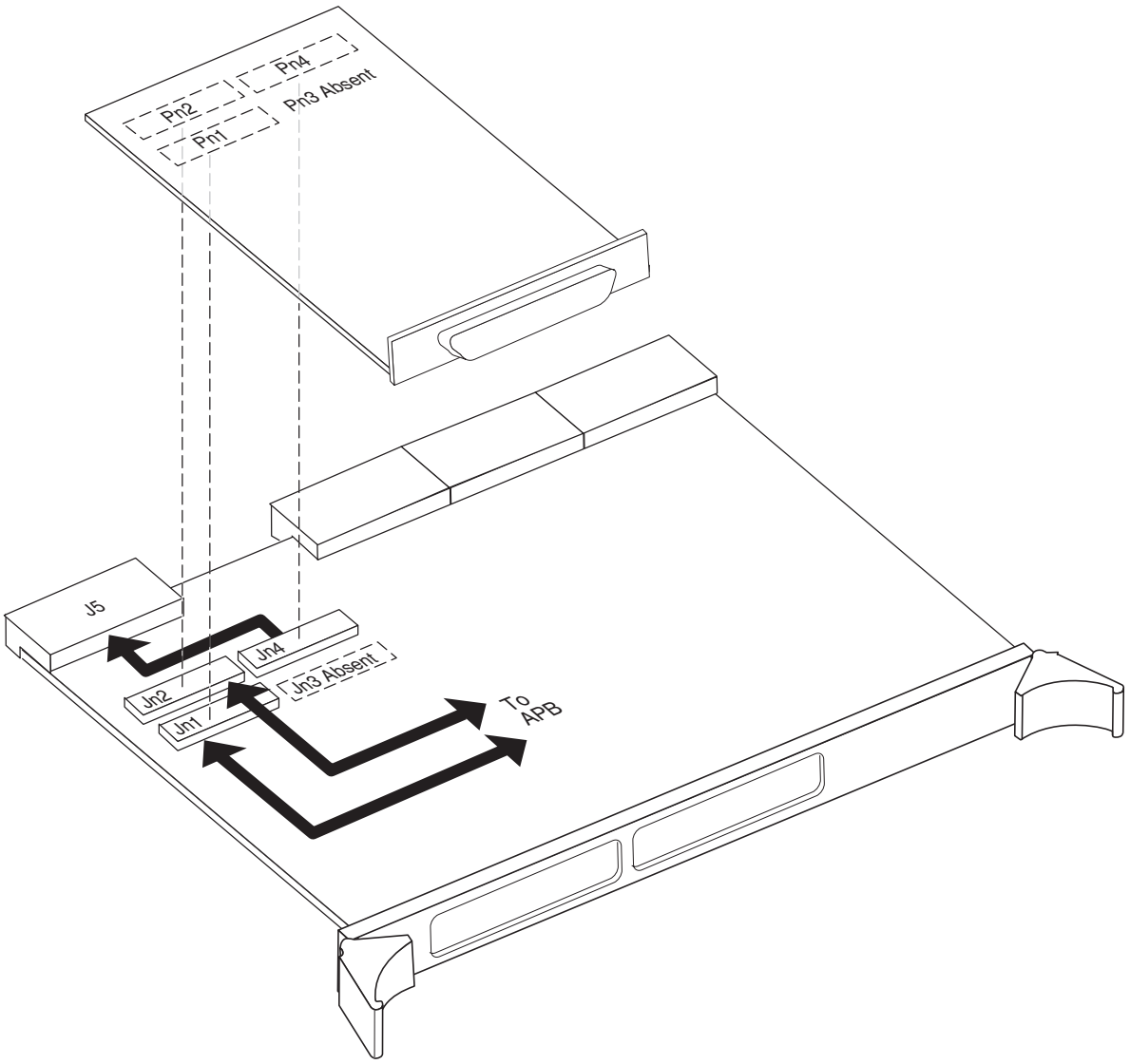


FIGURE 5-14 Data Paths in PCI Mezzanine Module Interface on Host Board

The APB on the Netra CP2160 board supplies PCI bus signals to PMC connectors J21 and J22. The PMC card logic decodes its specific I/O interface, which it makes available at the front panel.

64-pin PMC connectors J23 and J13 are not fitted to these Netra boards. These connectors are specified for expansion for 64-bit PCI (it carries the upper 32 bits), which is not provided. A 64-bit capable PMC card can function in these slots but its bus interface is constrained to 32 bits.

J24 is specified for user I/O and carries PMC signals to CompactPCI backplane connector J3. If a transition card is installed, this J5 I/O is conditioned by an IHV-supplied PIM to provide matching I/O on the enclosure back panel. Its backplane I/O is routed to CompactPCI/J5 connector.

In the case of the PMC B card for the Netra CP2160 board, J11 and J12 are similarly connected to the APB but the user I/O from J14 is routed out of CompactPCI connector J3.

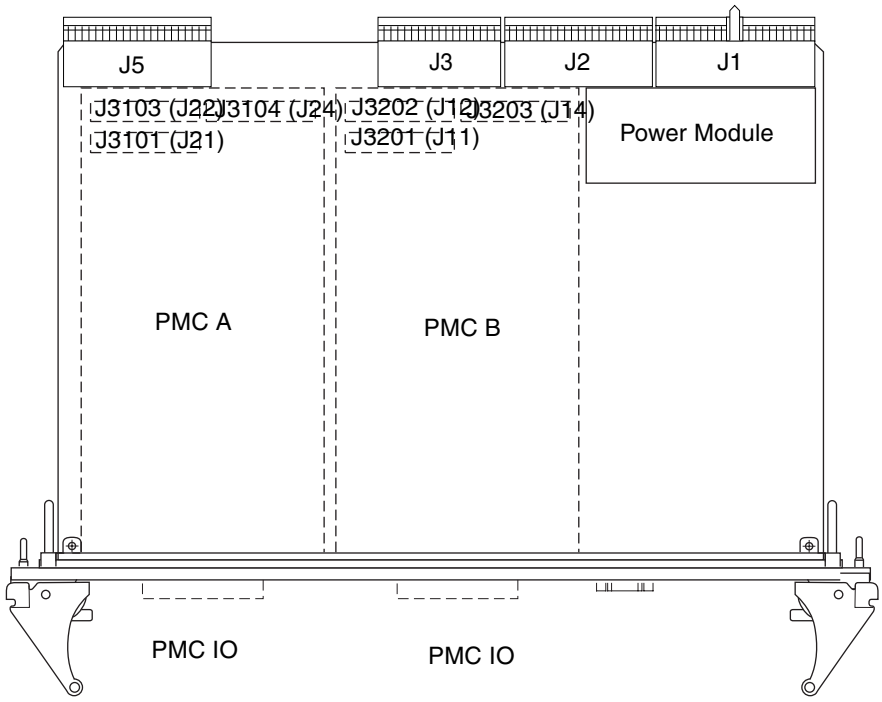


FIGURE 5-15 PMC Connector Interfaces on Netra CP2160 Board.

5.4.5 I²C and IPMI Channels

The I²C paths are shown in FIGURE 5-16. I²C communication is used:

- To implement the IPMI interface for system management.
- To provide a means of performing Local Advanced System Monitoring (ASM) which monitors—and controls where appropriate—local board or chassis "housekeeping" functions. These functions include: monitoring of temperature, FRU ID, MAC address, and memory type and size.
- To provide an interface for user monitoring and control, for example chassis temperature or fan operation.

Each I^2C device on the board uses common address pins. The devices are distinguished by the internal device ID. All I^2C devices are supplied from early power before backend power is established (see Section 5.8, "Power Subsystem" on page 5-30 for further details).

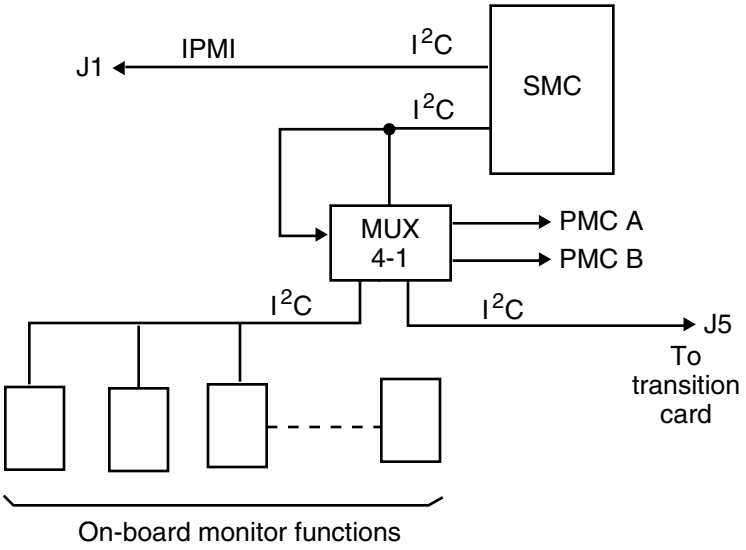


FIGURE 5-16 Netra CP2160 Board and CP2160 I^2C Paths

5.5 System Input/Output

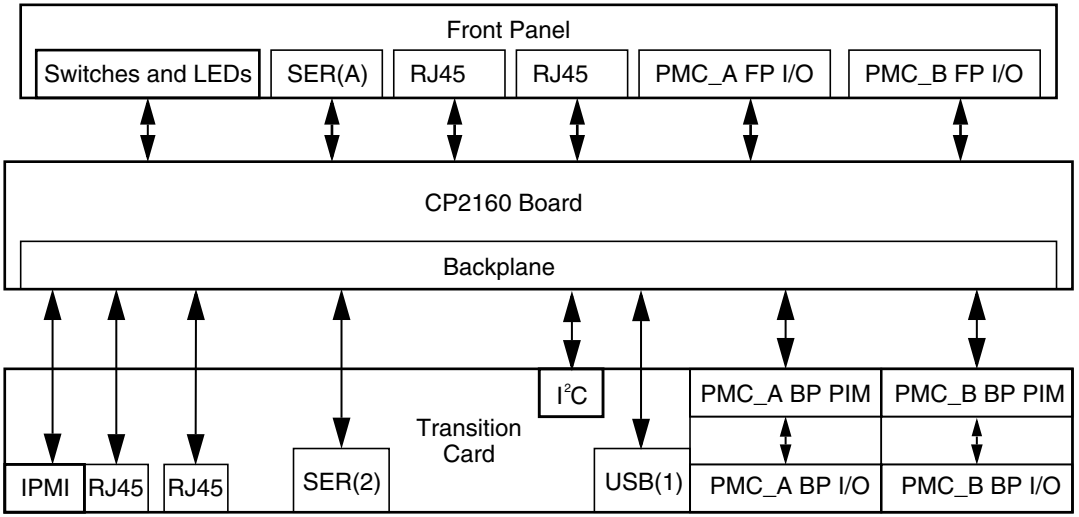


FIGURE 5-17 I/O Interfaces

FIGURE 5-17 shows the I/O for the Netra board. The I/O functions can be categorized into four groups which are described in the following sections.

5.5.1 Front-Panel I/O

FIGURE 5-18 illustrates the indicators and I/O connectors on the Netra CP2160 board front panel. The Netra CP2160 board front panel connectors, buttons and LEDs are described below:

- Two peripheral mezzanine card (PMC) I/O bezels
- Two RJ45 Ethernet connectors (with built-in transformer) connected to two separate PHYs, which are muxed with the other two PHYs of CPCI connector J5
- A serial connector (mini-D9) which is also connected to serial port A of the 16552 UART on the board
- ABORT – An abort pushbutton; passes an XIR signal to the SMC
- RESET – A reset pushbutton; passes an Power-on-Reset (POR) signal to the SMC
- USER – An orange and green (two color) LED that is defined by the user. The default function for the green LED signals that the board is at OK status. The colors are controlled by SPARC via SMC. See the *Netra CP2000 and CP2100 Series*

CompactPCI Boards Programming Guide for Solaris Operating Environment, (816-2485-*xx*) for information on programming the user LED. You can access this document at:

```
http://www.sun.com/products-n-
solutions/hardware/docs/CPU_Boards/
```

- READY – A green power LED, sourced from the power module.
- A blue LED for hot-swap status, sourced from the SMC.

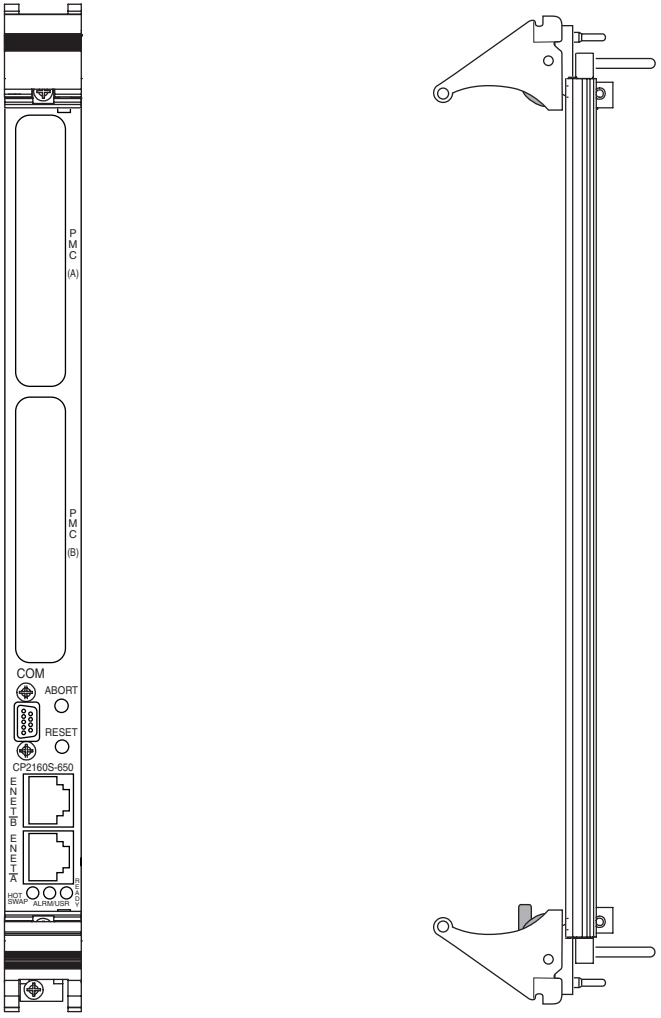


FIGURE 5-18 Netra CP2160 Board Front Panel

5.5.2 PMC Interface

The host board includes two PMC front-panel I/O cutouts to enable attachment of up to two PMC expansion cards. When installed, these cards access a PCI bus through compatible connectors provided on the host board. See Section 5.4.4, "PMC and PIM Interface" on page 5-16.

5.5.3 Backplane I/O

Most of the I/O channels to or from the board are passed to CompactPCI connectors J3 and J5; these channels are accessible from external connections on a transition card connected at the rear of the CompactPCI backplane. Connector J4 is not populated on these host boards to prevent contention with H110-compliant backplane signals. Contact assignments for these connectors are shown in Section B.3, "CompactPCI Backplane Connectors" on page B-9. For location of the connectors, see FIGURE 5-1.

5.5.3.1 J3 Signals

The user-defined PMC I/O signals from the two PMC Jn3 connectors pass to their external interface through the J3 CompactPCI backplane connector (see Section B.3, "CompactPCI Backplane Connectors" on page B-9).

5.5.3.2 J5 Signals

The following signal sets pass through the J5 CompactPCI backplane connector to connect to an external interface connector on the transition card:

- Two TP Ethernet channels from the PHYs
- Two serial channels
- Two USB channels
- An I^2C channel
- PMC I/O

5.6 System Management Controller

The System Management Controller (SMC) subsystem is one of the most important components of the system board. This subsystem provides a variety of service functions related to assuring availability of the system. These functions contrast with the board functions that execute applications.

The SMC consists of a small microcontroller with an SRAM for a software stack and nonvolatile memory for program storage and data logging. The SMC is modular in character, but is physically embedded into the circuitry of the Netra CP2160 board. FIGURE 5-19 shows its functional relationship with the system.

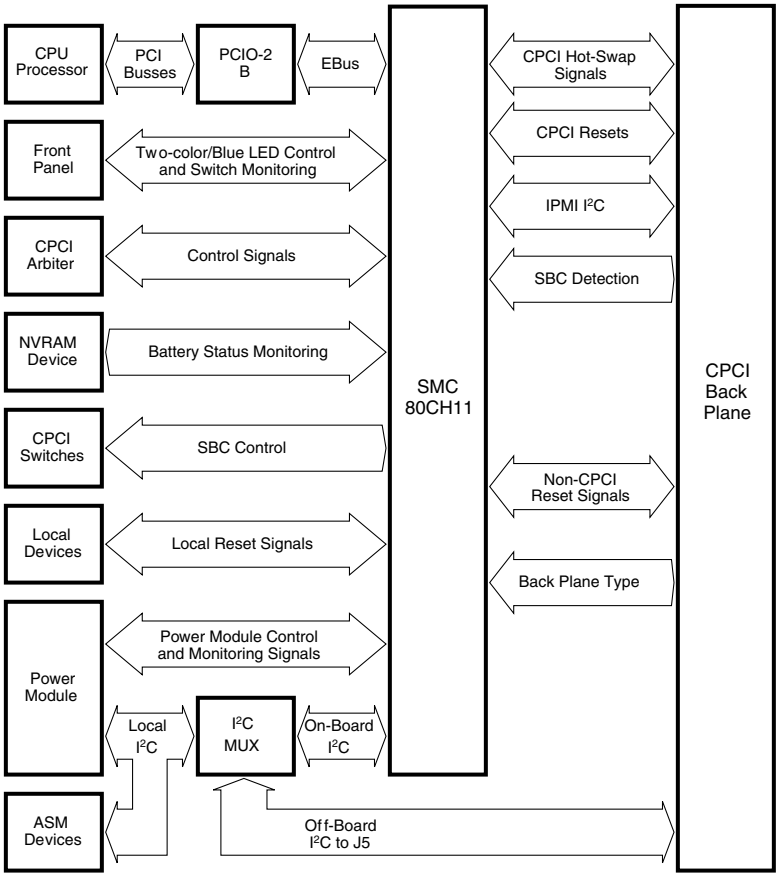


FIGURE 5-19 System Management Controller Interface

The SMC hardware and firmware implements the functions of system management and hot-swap control.

Note – Although the hardware and firmware functions are architecturally separate, reference to the SMC subsystem in this document—whose description is hardware oriented—refers to both functions.

The SMC controls the on-board CompactPCI interface components for the hot-swap process. It coordinates the state of the 21555 PCI bridge, the arbiter functions, and the switched connection of critical CompactPCI signals to the bus.

In performing these functions, the design maintains conformance with the PICMG CompactPCI core specification and the PICMG CompactPCI hot-swap specification: See Appendix D for references to these documents. The main features that are supported by the SMC subsystem are:

- Coordinates and controls local resets on the system board during power-on reset, watchdog timeout, software initiated reset, and as a result of user intervention such as pushbutton reset or backplane reset.
- Enables operation as either a system host board or as a satellite board in standard CompactPCI backplanes.
- Supports a command and communications interface between the UltraSPARC IIi host processor and the SMC microcontroller by means of an interconnecting EBus. This interface accommodates a command suite from the UltraSPARC processor to the SMC and supports bidirectional interrupt between the UltraSPARC processor and the SMC.
- Supports signals that are critical to system configuration or hot-swap reconfiguration. These signals accomplish CompactPCI reset control, bus enumeration, and configuration of CompactPCI bus arbitration. These signals apply differently depending upon whether the board acts as a system host board or a satellite board.
  - A satellite board responds to the CompactPCI RST, ENUM, HEALTHY, and BD_SEL signals from the active system host board (provided that this host provides HA hot-swap functions through the CompactPCI bus. See also Section 4.6.2, “PCI_RESET# Polling on the Satellite Board” on page 4-17). The satellite board also sets a REQ signal to the arbiter on the system host board and awaits a corresponding GNT from it.

Note – This board does not provide HA hot-swap control for peripherals.

  - A system board provides the CompactPCI peripheral reset signal PCI_RST and reads the CompactPCI bus enumeration signal ENUM. Its CompactPCI arbiter is configured to issue GNT signals to peripherals in response to their REQ requests.

- Implements a two-level watchdog timer for the SMC processor and for the host processor.
- Supports two I^2C ports. One of the I^2C ports carries an IPMI bus that is routed through CompactPCI backplane connector J1 to enable communication with other SMCs in the system. The other I^2C port serves a multiplexer that splits its input into two channels: one channel provides communication with on-board devices, (for example for temperature or FRU information); the other channel is for user functions and is passed out of J5 connector.
- Uses an EEPROM for storing non-volatile data such as the host board ID MAC address.
- Supports two system controller models of CompactPCI Hot Swap system architecture. See Section 1.3, "Hot-Swap Support" on page 1-10; also see Appendix D for a reference to the PICMG CompactPCI hot-swap specification.
- Communicates with other SMCs in the CPCI system using the IPMI protocol over a backplane link, in accordance with the PICMG CompactPCI hot-swap specification. The SMC:
  - Assumes a Baseboard Management Controller (BMC) role when the host board is installed in a system host slot.
  - Responds to commands from the active BMC when the host board is installed in a peripheral slot.
- Enables Local Advanced System Monitoring (ASM); ASM is a management scheme that monitors—and controls where appropriate—local board or chassis "housekeeping" functions through the on-board I^2C interface. Such functions include (see also Section 4.6, "ASM Support at OpenBoot PROM" on page 4-16):
  - Temperature sensing
  - Power supply voltage sensing
  - Power supply module on/off control
  - Memory module and board ID detection
- Supports flash update – The SMC firmware supports external update of its flash RAM (see Chapter 4).
- Acts as a peripheral management interface, which includes:
  - IPMI communications with Baseboard Management Controller
  - Handling of hot-swap (HEALTHY/ENUM/PRESENT) related signals
  - Receiving system and CompactPCI reset events to generate local board reset

For full details on SMC and reset information, refer to Chapter 4 and the Netra CP2160 board web site:

```
http://www.sun.com/products-n-
solutions/nep/hardware/boards/cp2160/
```

5.6.1 Watchdog Timer

In the Netra CP2160 board, the SMC implements a two-level watchdog timer. The host-SMC command interface defines communication between host and SMC. The host and the SMC constantly communicate with each other when the watchdog timer is enabled. The SMC monitors the heartbeat of the CPU processor host. The heartbeat is sent in the form of a reset watchdog timer that is sent from the CPU to the SMC. The watchdog timer must be programmed to ensure that it does not get too close to the expiration. There should be some time accounted for the latency overhead or any unexpected event that may delay transmission of the heartbeat. For full details on programming the watchdog timer, refer to the *Netra CP2000 and CP2100 Series CompactPCI Boards Programming Guide* (816-2485-*xx*).

The two levels of the watchdog timer are as follows:

- Countdown register timer (16 bits, 100 msec. resolution)
- Pre-timeout timer (1 sec. resolution)

The two watchdog timers are enabled by messages sent over the host-SMC command interface using the set watchdog timer command. The commands enabled in the host-SMC command interface for watchdog timer functionality are:

- `smc-reset-wdt`
- `smc-set-wdt`
- `smc-get-wdt`

The uses of these functions are shown in TABLE 5-2.

TABLE 5-2 Host-SMC Commands for Watchdog Timer

Host-SMC Command	Uses
`smc-reset-wdt`	Starts and restarts watchdog timer from the initial countdown value
`smc-set-wdt`	Initializes, configures and stops the watchdog timer
`smc-set-wdt`	Retrieves current settings and present timer value of watchdog timer

5.7 Resets

This section provides details on resets for the Netra CP2160 board.

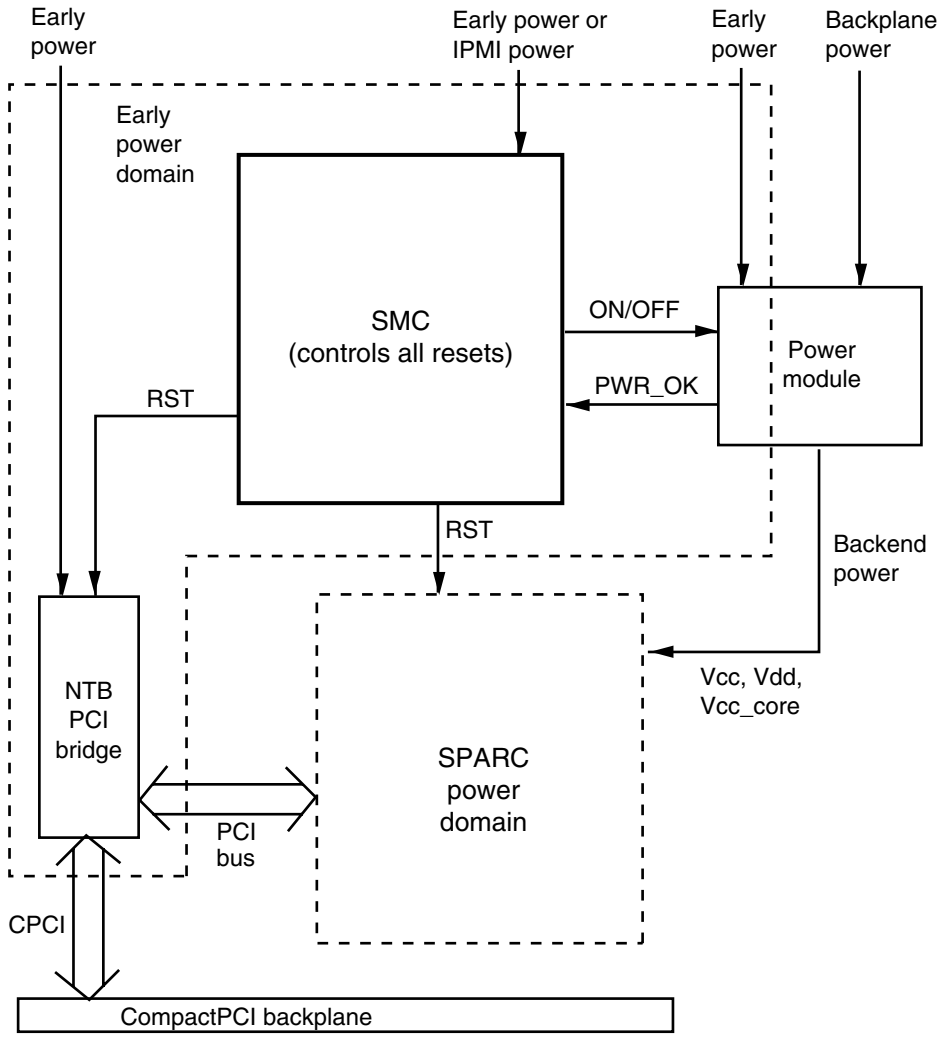


FIGURE 5-20 Simplified Reset Paths

Parts of the system are powered by *early power* before the SPARC domain receives power (backend power). See Section 5.8, "Power Subsystem" on page 5-30. At the onset of early power, the SMC is reset by its component microcontroller. When backend power rails are at their specified voltages and if the SMC has the power module turned on, the SMC receives the PWR_OK signal and in turn resets the backend members of the system. Note that:

- When the SMC is reset, the whole system is reset.
- When the CPU is reset, the CPU I/O and the 21555 NTB is reset.
- The SMC can reset the 21555 NTB without resetting the CPU.

For detailed information on configurable reset implementation by SMC firmware, see Section 4.7.1, “SMC Firmware Reset Modes for System Slot and Peripheral Slot Operations” on page 4-19.

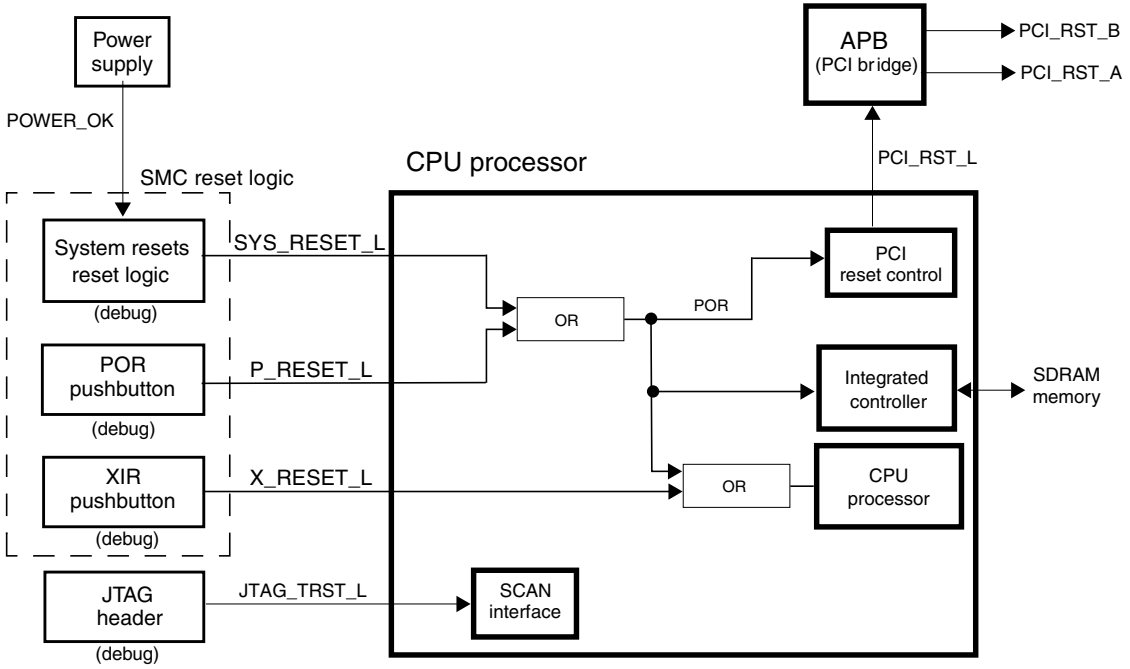


FIGURE 5-21 Simplified CPU Subsystem Reset Architecture

5.8 Power Subsystem

FIGURE 5-22 shows a simplified schematic diagram of the power subsystem. This subsystem can power the board to support a hot-swap environment.

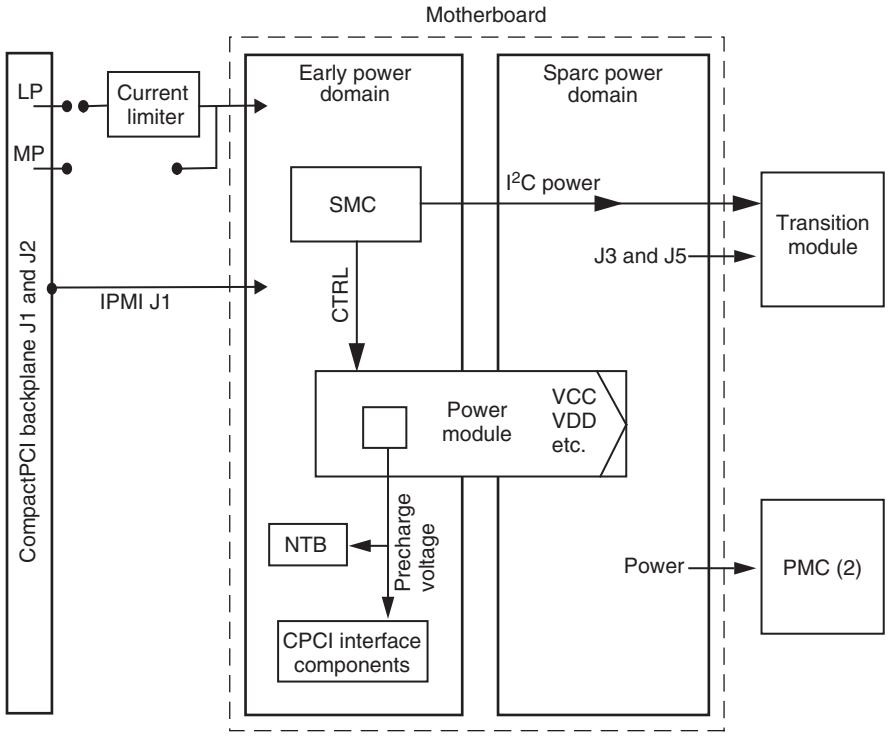


FIGURE 5-22 Power Distribution Block Diagram

Note – In FIGURE 5-22 I^2C power is derived from early power.

The Netra CP2160 board sequences power in two time-separated domains:

- Early Power domain
- SPARC Power domain—this is the *Backend Power* in the PICMG hot-swap specification.

Early power is applied to the board from backplane long pins (LP in the figure) as the board is inserted. Early power current flows to board subsystems:

- Power Module – supplies precharge current to the CompactPCI bus interface component.s
- SMC – needed to control logical state of the CompactPCI interface circuits as they are connected.
- IPMI/I^2C subsystems – needed for management/monitoring functions at this stage; I^2C power also extends to the transition card.
- The 21555 NTB and CompactPCI Interface component – must be placed in a known state during attachment to the CompactPCI bus.

5.8.1 Power Module

FIGURE 5-23 shows a schematic diagram of the power module. This subassembly is integrated with the Netra CP2160 board.

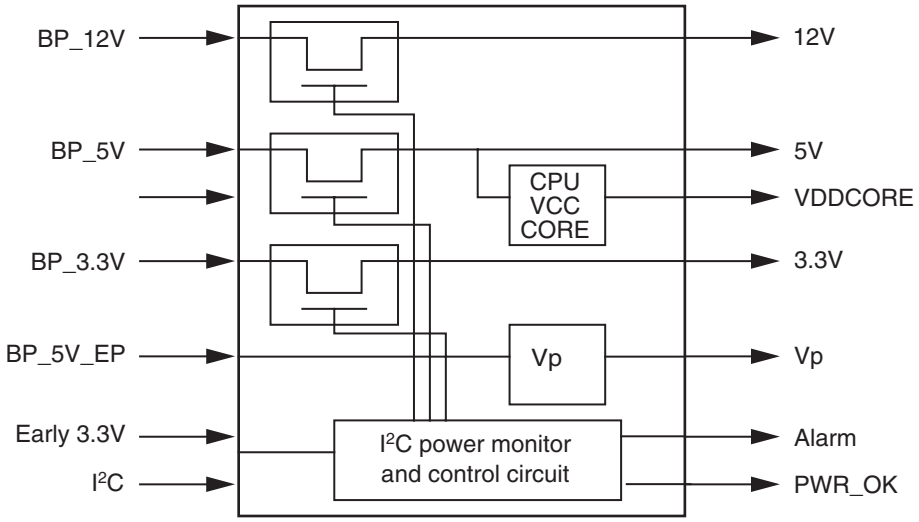


FIGURE 5-23 Power Module Interface

This subsystem performs the following functions:

- Generates Vp, the CompactPCI hot-swap precharge bias voltage using early power
- Generates V_{DDCORE} , the UltraSPARC processor core voltage supply.
- Controls and gates 5V, 12V, 3.3V and -12V
- Automatically shuts down in case of overcurrent or overvoltage
- Asserts the PWR_MOD_OK signal

The power module is controlled by the SMC and the power on/off signal. Functions controlled include core voltage, output level, and module on or off state. There are also automatic controls within the power module, for example, overcurrent shutdown, and voltage regulation.

The power module has a DIP switch with six preset default settings. These switches are for factory use only (see FIGURE 5-24 for location). The user must not change DIP switch settings.

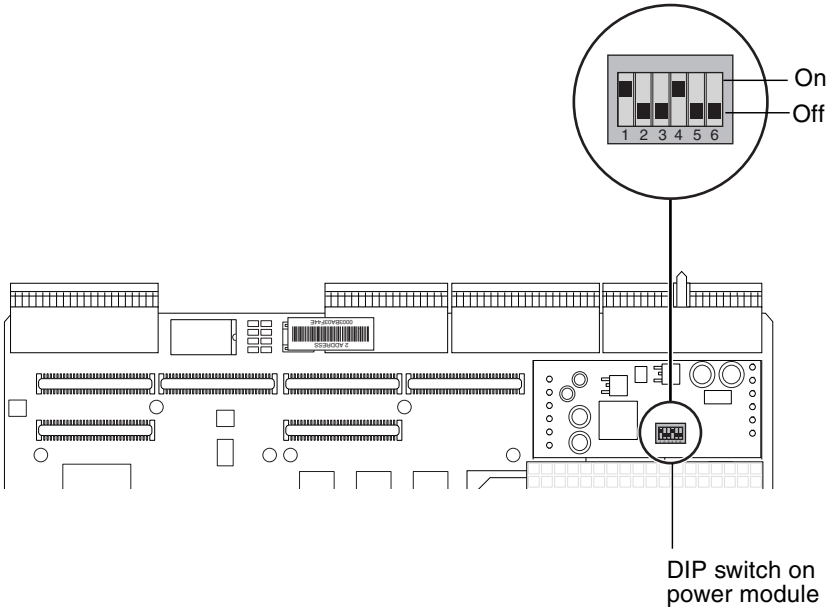


FIGURE 5-24 DIP Switch Settings on Power Module

Note – The preceding figure is only an example of the types of settings you might find on the board youn receive. The DIP switch settings on your board might have been set differently in the factory.

5.8.2 Early Power and IPMI Power

If the system power for the backplane fails, the SMC can use IPMI power, typically supplied from an uninterruptible power supply (UPS), instead of early power from the CompactPCI backplane. The backplane is provided with IPMI power pins for this purpose. FIGURE 5-25 shows the circuit arrangement that selects between these power sources.

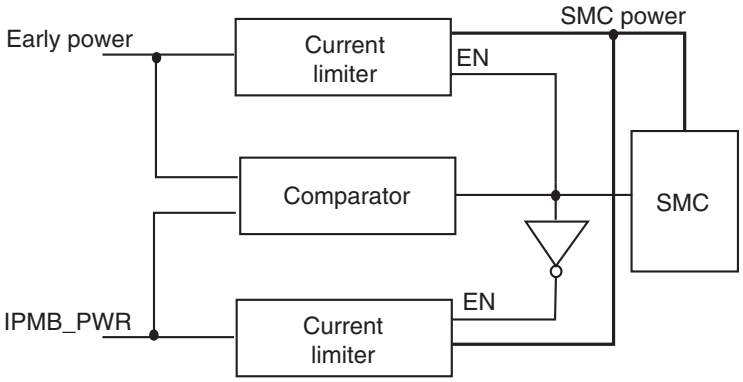


FIGURE 5-25 Selection Between Early Power and IPMI Power

5.8.3 Transition Card Power Distribution

FIGURE 5-26 shows the power rail routing to the transition card. The XCP2160-TRN I/O transition card is powered from the Netra CP2160 board rather than directly from the backplane. The transition card must always be connected to the backplane before the chassis is powered. Always install the transition card before the Netra CP2160 board in the chassis. For details on using a transition card, see Chapter 3.

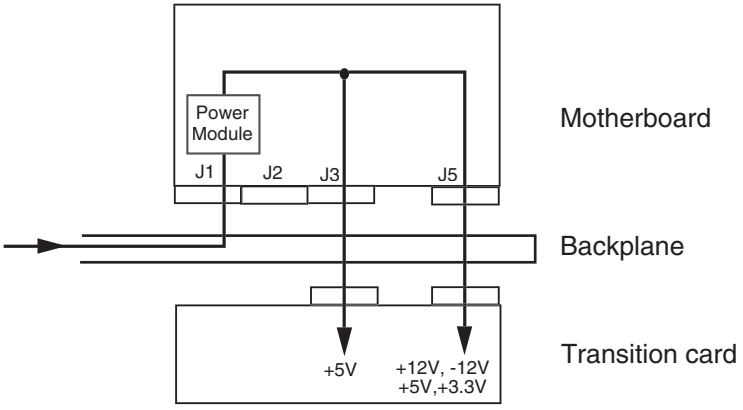


FIGURE 5-26 Transition Card Power Supply Routing

Note – Some V(I/O) power lines are routed into J2 of the motherboard; this is not shown in the figure for clarity.

5.9 CompactPCI Interface

This section provides information on CompactPCI and the Netra CP2160 board interface requirements specifications and CompactPCI signal interface.

5.9.1 CompactPCI Interface Requirements

TABLE 5-3 lists the requirements for Netra CP2160 boards as defined by the PICMG 3.0 CompactPCI and Netra CP2160 board design requirements specifications:

TABLE 5-3 Compact PCI Interface Requirements

Requirement	Description
Bus termination	10 ohm CPCI series termination resistor shall be located 0.600 max. from J1/J2 pin on all required signals.
Stub length	CPCI pull-up stub length 0.500 inches max.
5V VIO	Provides 1.0K ohm +/-1% pull-up for all required CompactPCI bus signals for use in 5V CompactPCI signaling environment.
System and peripheral slot operation	Provide control to disable both pull-ups (In a CompactPCI system, only the board in the system slot can provide the bus pull-ups).
Hot swap	Provide 1V +/-20% precharge bias voltage (Vp) for all required CompactPCI bus signals.
Max capacitive load per pin and system and satellite slot operation	Provide an auxiliary output for selected CompactPCI bus signals (those that are shared between the bridge and external arbiter)

5.9.2 CompactPCI Signal Interface

The tables in this section list the CPCI signal interface description and the CPCI connector power signal interface. The primary side of the bridge is attached to the 64-bit CompactPCI bus.

TABLE 5-4 Compact PCI Signal Interface

Signal	Description	Type	Notes
P_AD<63..0>	Addr/Data Bus	I/O	
P_CBE<7..0>	Command/ Byte Enable#	I/O	
P_CLK	Clock Input	I	33 MHz Compact PCI Bus Clock.
P_IDSEL	ID Select	I	
P_INTA_L	Primary Bus Interrupt	OD	Needs external pullup. Assert when: • Primary doorbell register bit set. • I20 outbound queue not empty. • Subsystem event bit set.
P_GNT_L	Bus Grant	I/O	Shared with arbiter.
P_REQ_L	Bus Request	I/O	Shared with arbiter.
P_PAR	Parity for lower 32 bits	I/O	
P_PAR64	Parity for upper 32 bits	I/O	Requires external pullup.
P_PERR_L	Parity Error	I/O	Requires external pullup.
P_SERR_L	System Error	I/O	Requires external pullup.
P_RST_L	Bus Reset	I	
P_VIO	Signaling Environment 3.3V or 5V	I	
P_DEVSEL_L	Device Select	I	Requires external pullup.
P_FRAME_L	Frame	I	Requires external pullup. Shared with arbiter.
P_STOP_L	Stop	I	Requires external pullup.
P_IRDY_L	Initiator Ready	I/O	Requires external pullup. Shared with arbiter.

TABLE 5-4 Compact PCI Signal Interface *(Continued)*

Signal	Description	Type	Notes
P_TRDY_L	Target Ready	I/O	Requires external pullup. Shared with arbiter.
P_REQ64_L	64 -bit transfer request	I/O	Requires external pullup.
P_ACK64_L	64 -bit transfer ack	I/O	Requires external pullup.

TABLE 5-5 CPCI Connector Power Signal Interface

Voltage	CPCI Pin(s)	Net Name	Notes
3.3V	J1-C6 & C22	BP_EP_3.3V	Long pin
3.3V	J1-A15, A17, A19, A21, A23, C10, C18, & D25	EP_3.3V	Medium pin
5V	J1-D3 & D23	BP_EP_5V	Long pin
5V	J1-A1, A25, B2, B24, E1, & E25	EP_5V	Medium pin
+12V	J1-D1	BP_12V_POS	Medium pin
-12V	J1-B1	BP_12V_NEG	Medium pin
3.3V or 5V	J1-C4	BP_EP_VIO	Long pin
3.3V or 5V	J1-C8, J1-C16, J1-C24, J2-A4, J2-C5, J2-C7, J2-C9, J2-C11, J2-C13	EP_VIO	Medium pin

Note – The early power voltages supply critical circuits such as SMC, CPCI interface circuits, and power module control circuit.

5.10 Interrupts

The Netra CP2160 board interrupts are listed in TABLE 5-6. These are processed and encoded by the I-Chip2 ASIC. This device assigns equal priority to all interrupting devices. When two devices need servicing at the same time, the I-Chip prioritizes using its internal round-robin scheduling scheme. The resultant vector is passed to the processor as a 6-bit parallel word. The ultimate interrupt priority is resolved in the UltraSPARC IIi processor.

TABLE 5-6 Interrupt Assignments

Offset	Interrupt	INT#	Priority
0	CPCI_INTA*	7	7
1	CPCI_INTB	5	5
2	CPCI_INTC	15	5
3	CPCI_INTD	2	2
4	SPARC_H_INT†	F	7
5		D	5
6		LD	5
7		A	2
8	PCIO-2_A_ENET	17	6
9		38	5
A	PMC1_INT_A	10	2
B	PMC1_INT_B	12	1
C	PMC1_INT_C	18	6
D	Not on IChip2	39	4
E		0	2
F	DOORBELL	1A	1
10	DUART_SER_A	6	6
11	MCA_INT_L	4	4
12		3	3
13		1	1
14	DUART_SER_B	E	6
15	PMC1_INT_D	C	4
16	PMC2_INT_A	B	3
17		9	1
18		16	6
19	PCIO-2_B_EBUS	14	4
1A		13	3
1B		11	1
1C	PCIO-2_B_ENET	1E	6
1D	PCIO-2_A_EBUS	1C	4

TABLE 5-6 Interrupt Assignments *(Continued)*

Offset	Interrupt	INT#	Priority
1E	SPARC_L_INT†	1B	3
1F		19	1
20	PMC2_INT_B	20	3
21		21	3
22	PMC2_INT_C	22	2
23		24	8
24	PCIO-2_A_USB	1F	7
25		25	8
26	PCIO-2_B_USB	28	7
27	PMC2_INT_D	29	8
28	I2C_GLOBAL_INT	2A	2
29		2B	4
2A		2C	4
2B	SYNC_SER_L1	2D	7
2C			RES
2D			RES
2E			RES
2F			RES
graphic 1 23 from INR	CPCI_SERR_L‡	23	5
graphic 2 26 from INR		26	5

* CPCI_INT_A is shared with the Bridge Secondary side interrupt.

† SPARC_L_INT and SPARC_H_INT are driven by the SMC module.

‡ CPCI_SERR_L is masked at the PLD.

5.11 Chip-Select PLD Registers

The TABLE 5-7 lists the chip-select PLD registers.

TABLE 5-7 Chip-Select PLD Registers

EBus Address	R/W	Name	Description
0x20.000	W	DUART_RESET	Any write operation to this register toggles the DUART reset line.
0x20.0001	R/W	PMC_BUSMODE	Bit 4: PMC_BUSMODE4_L. R/W; boot default = 0 Bit 3: PMC_BUSMODE3_L. R/W; boot default = 0 Bit 2: PMC_BUSMODE2_L. R/W; boot default = 1 Bit 1: PMC_BUSMODE1_L. Read only; writes are ignored. Bit 0: PMC_BUSMODE0_L. Read only; writes are ignored.
0x20.0002	R/W	WRITE_PROTECT	Bit 1 : I^2C write protect • 1 = protected • 0 = unprotected • Boot default is 0 Bit 0: User flash write protect • 1 = protected • 0 = unprotected • Boot default is 0
0x20.0003	R	PLD_REV	Read returns the PLD firmware revision, for example, 0xB3.
0x20.0004	R/W	SPARC_INT	SMC_SPARC_L_INT_L mask bit. SMC_SPARC_L_INT_L enters the PLD. PLD_SMC_SPARC_L_INT_L is the masked output. • 0 = masked HIGH • 1 = not masked • Boot default is 1.

TABLE 5-7 Chip-Select PLD Registers *(Continued)*

EBus Address	R/W	Name	Description
0x20.0005	R/W	INTx	CPCI interrupts mask register. CPCI interrupts enter PLD as SW_CP_INTx_L. Masked outputs are PLD_CP_INTx_L. Mask behavior: • 0 = masked HIGH • 1 & CP2160 is SBC = unmasked • 1 & CP2160 is not SBC = TRISTATE • Boot default = 1 Bit assignments: • Bit 3 = INTA_L • Bit 2 = INTB_L • Bit 1 = INTC_L • Bit 0 = INTD_L
0x20.0006	R/W	DOORBELL	BRG_S_INTA_L mask bit BRG_S_INTA_L is the input to the PLD PLD_BRG_S_INTA_L is the masked output • 0 = masked HIGH • 1 = unmasked • Boot default = 1
0x20.0007	R/W	TEST	For development use. May be written with any value and read.
0x20.0009	R/W	USERFLASH_SELECT	Bit 7: PLD_FLASH1_SEL (Read only) Bit 6: PLD_FLASH0_SEL (Read only)

Note – The registers in the chip-select PLD are mirrored in the EBus address space.

5.12 SMC PLD Registers

TABLE 5-8 shows the SMC PLD registers.

TABLE 5-8 SMC PLD Registers

EBus Address	R/W	Name	Description
0x1FF.F320.FF00		SMC_INT0 Register No. 1	Bit 7: PWR_MOD_OK signal Bit 6: Latched cPCI RST# • 0 = cPCI RST# was asserted • 1 = cPCI RST# has not been asserted Bit 5: PB_RST_L signal Bit 4: PB_ABORT_L signal Bit 3: SPARC_RST_21554_L signal Bit 2: BKRST_IN_L signal Bit 1: BP_DEG_L signal Bit 0: BP_FAL_L signal Any of the bits asserting LOW initiates an assertion of SMC_INT0_L.
0x1FF.F320.FF01	R	SMC_INT_0 Register No. 2	Bit 7: SERR_L signal INVERTED Bit 6: Non-latched PCI RST# signal Bit 5: IPMI power status • 0 = no ipmi_pwr in • 1 = ipmi_pwr in Bit 4: Option switch #2 status Bit 3: Option switch #1 status Bit 2: Reserved Bit 1: Reserved Bit 0: Reserved
0x1FF.F329.FF02	R/W	General purpose I/O	Bit 7: bp_GPIO_j4e1 GPIO Bit 6: bp_pwroff_j4c10 power Bit 5: sys_rst_set Bit 4: bkrstout_set Bit 3: 21554_rst_set Bit 2: xir_out_set Bit 1: pb_rst_set Bit 0: rst_j1c5_set All bits default HIGH.

TABLE 5-8 SMC PLD Registers *(Continued)*

EBus Address	R/W	Name	Description
0x1FF.F320.FF03	R/W R/W	FIFO/Address register	Bits 7-5: Address FIFO Bits 4-0: ADDR3 Register Bit 4: block PRST, default LOW Bit 3: block cPCI RST#, default HIGH Bit 2: enable NVRAM, default LOW Bit 1: PWR_MOD_ON, default HIGH Bit : SYSEN_ON_L, default LOW
0x1FF.F320.FFFF	R	Revision	SMC PLD Revision Level

APPENDIX **A**

Specifications

Specifications for the Netra CP2160 board are provided in the following sections:

A.1 System Compatibility Specifications

TABLE A-1 System Compatibility Attributes

Property	Specification
Satellite board capability	Yes
System host capability	Yes
H110 chassis compatible	CompactPCI J4 is unconnected at the board; which enables this board to be used in H110 chassis
NEBS compliance	NEBS Level 3 specification compliance
CompactPCI compliance	• PICMG 2.0 R3.0 CompactPCI bus specification for 33MHz PCI speed • PICMG 2.1 R1.0 Hot Swap specification • PICMG 2.9 System Management specification

A.1.1 CPCI Specification Notes

The CPCI standard, PICMG 2.0 Rev 3, calls out the maximum component heights of 13.71 +/- 0.03 mm. Due to variations in parts, board flatness, board thickness, and manufacturing tolerances, the memory turrets installed on a Netra CP2160 board may exceed this limit.

PICMG 2.0 Rev 3 and IEEE 1101.10-1996 requires 2.54mm between the top of components and the separation plane, and there is at least approximately 0.5mm to 2mm of clearance to solder-side components or leads of an adjacent board from that same separation plane. Therefore, there is very little chance that a small specification violation will impact an adjacent card in a PICMG 2.0 Rev 3 compliant chassis.

Care should be taken when installing the boards in systems that have extreme solder-side component heights or in system chassis that don't allow clearances specified in the PICMG or IEEE standards.

The Netra CP2160 board also has a solder side cover installed. The components on the solder side cover meet the limits of the CPCI specification for maximum height. The solder side cover is nominally 1mm thick. When this cover rests upon components greater than 1mm in height, the cover itself may violate the CPCI specification where it rests on these components.

A.2 CPU Specifications

TABLE A-2 CPU Specification

Property	Specification
CPU	650 MHz UltraSPARC IIi
Mounting	370-pin ceramic PGA package soldered to board
Architecture	Sun 4U; 64-bit SPARC V9 architecture with the VIS instruction set
Cache	Integrated, 512 Kbyte, 4-way, set-associative internal L2 cache operating in 2:2 mode
PCI bus local interface	PCI Bus 2.1 compatible, 33/66 MHz, 32-bit, 3.3V (internal to board only, does not come on connector)

A.3 Main Memory Specifications

TABLE A-3 Memory Specification

Property	Specification
Memory size—min	1 GB
Memory size—max.	Up to 2 GB
Onboard memory	1 GB on-board memory, with an additional 1 GB double-wide memory available for order
Memory combinations	One custom 198-pin stackable module; see TABLE A-4 for allowable combinations
Memory type	3.3V, synchronous DRAM with ECC LVTTL-compatible CMOS; configured on bus width of 64-bit + 8-ECC bits
Identification to system	Serial EEPROM provides serial presence detect (SPD) to IPMI interface
ECC	8-bit; single bit error correction; double-bit error detection

A.4 Memory Configuration Specifications

The default memory configuration on the Netra CP2160 board is 1 GB. The possible memory configurations are shown on TABLE A-4.

TABLE A-4 Memory Module Configurations Available on CP2160

Onboard memory	Top SDRAM Module P/N and Specification	Total Memory Available on Board
1 GB	none	1 GB
1 GB	375-3026-*xx* 1GB	2 GB

For directions on the installation process of the stackable memory modules on the Netra CP2160 board, refer to the document *Memory Module Installation and Removal Guide for Netra CP2000/CP2100 Series CompactPCI Boards* (817-0654-*xx*).

A.5 PMC Interface Specifications

TABLE A-5 PMC Interface Specification

Property	Specification
PMC module interfaces on system board	Two: PMC A and PMC B
Interface IEEE P1386.1 compliance	With draft 2.1
Connector configuration, PMC A (P1386 designations)	J21, J22 carry PCI signals; J24 module I/O is connected to CPCI backplane J5; J23*
Connector configuration, PMC B (P1386 designations)	J11, J12 carry PCI signals; J14 module I/O is connected to CPCI backplane J3
PMC connections to CPCI backplane	PMC A on J5; PMC B on J3
PCI clock	33 MHz
PCI bus width	32-bit
Max power load -- per module, combined power rails (5V, 3.3V, 12V, -12V)	7.5 W[2]

* J23 is for internal Sun Microsystems use only and is not installed

A.5.1 PMC Specification Notes

The PMC standard, IEEE 1386, calls out the maximum component height of 4.70 mm below a PMC card. This allows for a 0.6 mm gap separating components on the motherboard from components on the PMC card. The Netra CP2160 board utilizes a standard memory connector that is nominally 5.2mm tall. This means that there would be only 0.1 mm of clearance in two areas below the PMC slot closest to the CPU (PMC B)in the area of two motherboard memory sockets of 4.93 mm by 43.40 mm.

The PMC A slot is not affected by the memory socket height. When at all possible, install any PMC cards that barely meet or exceed PMC component height restrictions in the PMC A slot. PMC disk drive cards in particular may impact the memory connectors on PMC B, as some commercially available PMC disk cards meet or exceed component height restrictions.

A.6 Power Requirements

This section provides information on power sequencing and power requirements by connection phase.

TABLE A-6 shows the power drawn from the backplane connector by phase.

TABLE A-6 Netra CP2160 Backplane Connector Power Requirements by Connection Phase

Power Rail	Early power on long pins† Typ. (A)	Main power on medium pins:‡ Typical (with 1 GB total memory)	Main power on medium pins: Typical (with 2GB total memory)§	Description
+5V*	0.35	3.0A	3.0A	at connector J1/J2
+3.3V	0.02	3.0A	3.4A	at connector J1/J2
+12V	0.00	15mA	15mA	at connector J1/J2
–12V	0.00	15mA	15mA	at connector J1/J2
IPMB_PWR	--	--	--	at J1/A4

* The V I/O on the backplane is connected to 5V.

† The typical figures provided for early power are only provided as examples

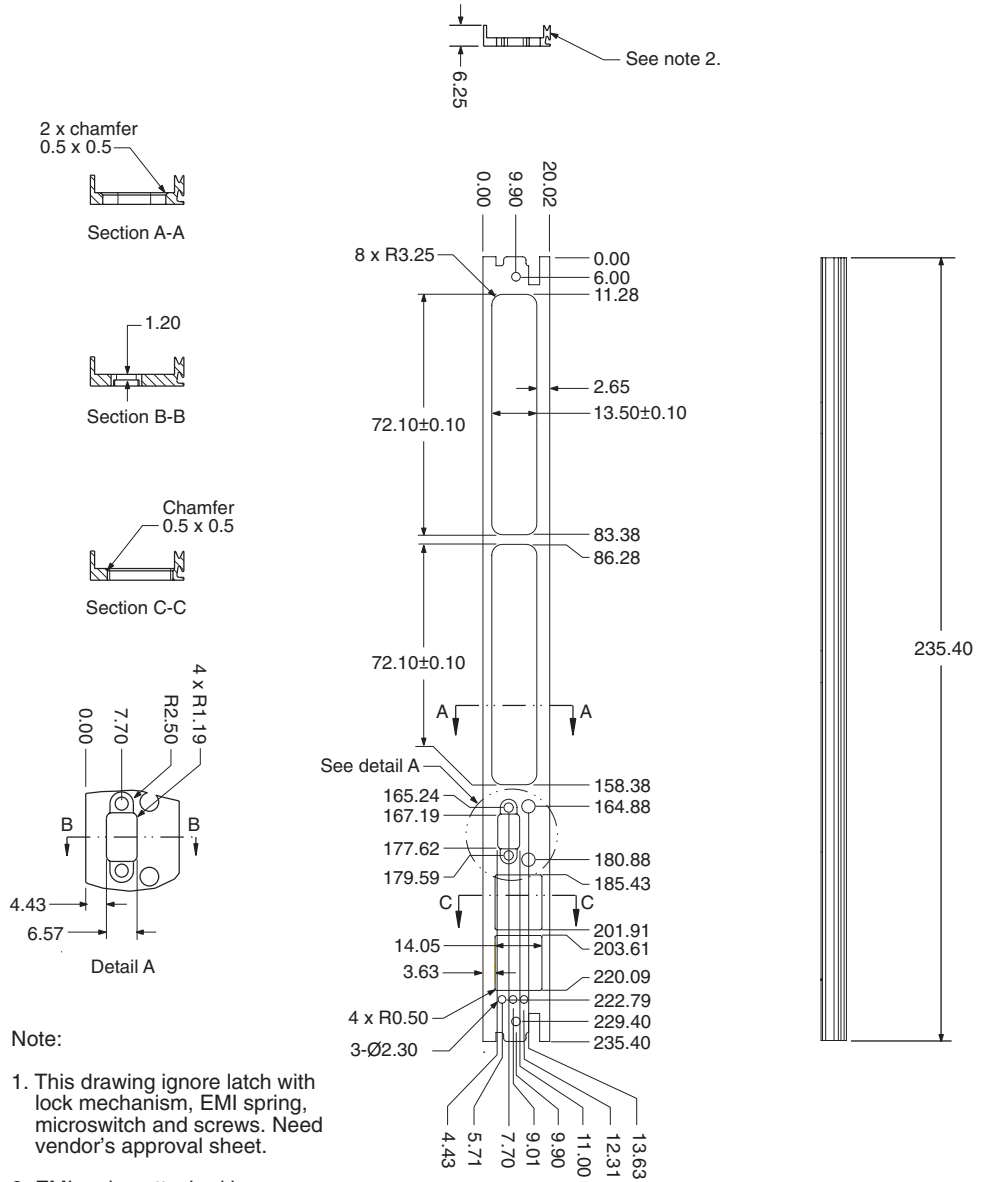
‡ The typical figures are calculated as measured on a similar cPCI board, no PMC cards, with or without the XCP2060-TRN I/O Transition Card and while running SunVTS.

§ The maximum memory supported is up to 2GB.

A.7 Mechanical Specifications

These products comply with the mechanical specifications to be found in the CompactPCI specification PICMG 2.0 R3.0. See Appendix D for a reference to this specification.

FIGURE A-1 shows a mechanical illustration of the Netra CP2160 board panel.



Note:

1. This drawing ignore latch with lock mechanism, EMI spring, microswitch and screws. Need vendor's approval sheet.

2. EMI spring attached here.

FIGURE A-1 Mechanical Illustration of the Netra CP2160 Board Front Panel

A.8 Environmental Specifications

TABLE A-7 Environmental Conditions and Limits

Ambient Conditions	Low Limit*	High Limit
Transportation and storage temperature	-40^0 C	+70^0 C
Transportation and storage humidity	5% RH† non-condensing	95% RH non-condensing
Operating temperature	0^0 C (-5^0 C short term)	40^0 C (55^0 C short term)
Operating humidity	15% RH non-condensing	85% RH (90% RH short term) non-condensing
Shock and vibration	As stated in NEBS GR-63 CORE specifications, section 4.3.1 and 4.3.2 for shock criteria and 4.4.3 for vibration criteria; MIL-STD 810E, Method 514.4, CAT I MIL-STD 810E, Method 516.4, II-3.2	
Electrostatic discharge	NEBS GR-1089 Section 2	

* Short term, in this column, refers to a period of not more than 96 consecutive hours and a total of not more than 15 days in 1 year.

† RH is relative humidity.

A.9 Thermal Validation

The ASM CPU sensor should not exceed 85^0 C when installed in the system. Refer to the *Netra CP2000 and CP2100 Series CompactPCI Boards Programming Guide (*816-2485-*xx)* for more information on ASM thermal validation.

A.10 Reliability / Availability Specifications

Reliability prediction is the first measurement point of expected behavior of the inherent design mean time between failures (MTBF) of the product. MTBF values calculated are shown in TABLE A-8.

TABLE A-8 Reliability Prediction for Board Level MTBF

Items	MTBF (hours)	Annualized Failure Rate (AFR in %)†
Netra CP2160 board* (includes 1 GB soldered memory and power module)	180,098	4.75%
XCP2060-TRN card	2,083,333	0.42%
Memory card 1GB (P/N 375-3026-01)	758,529	1.15%

* Board ambient temperature at 40^0 C

† AFR (%) is Annualized Failure Rate based on 8,760 power on hours (POH) per year.

A.11 Compliance Specifications

A.11.1 Agency Compliance

All printed wiring boards (PWBs) are manufactured by UL recognized manufacturers, and have a flammability rating of 94-V0 or better.

Compliance with EMI and safety regulations for products including the Netra CP2160 board is entirely the responsibility of OEMs. The Netra CP2140 board has passed FCC Class B tests in representative enclosures. However, the EMI Class of the end use system is dependent upon system level EMI design parameters.

The Netra CP2160 boards are intended to be incorporated into systems meeting the following regulations and compliances:

- USA FCC part 15
- USA Safety UL 60950

- Canadian EMI ICES-003
- Canadian Safety CSA C22.2 Number 60950
- European Union EMC CE Mark EN55022, EN555024 and EN300-386 v1.3.1
- European Union Low Voltage Directive Safety CE Mark EN 60950
- Japanese EMI VCCI
- Taiwanese EMI BSMI
- Korean EMI MIC

A.11.2 NEBS Level 3

Board requirements for NEBS Level 3 criteria provide the highest assurance of product operability with minimal service interruptions over the life of the equipment. The requirements include the following categories and all associated sections and subcategories:

- GR-63-CORE, Issue 1, October 1995 - Network Equipment-Building System Requirements: Physical Protection
- GR-1089-CORE, Issue 2, Revision 1, February 1999 - Electromagnetic Compatibility and Electrical Safety - Generic Criteria for Network Telecommunications Equipment

APPENDIX **B**

Connectors, Pinouts and Switch Settings

This chapter contains the following subsections:

B.1 PMC Connectors

FIGURE B-1 illustrates PMC port connectors. The tables show contact allocations.

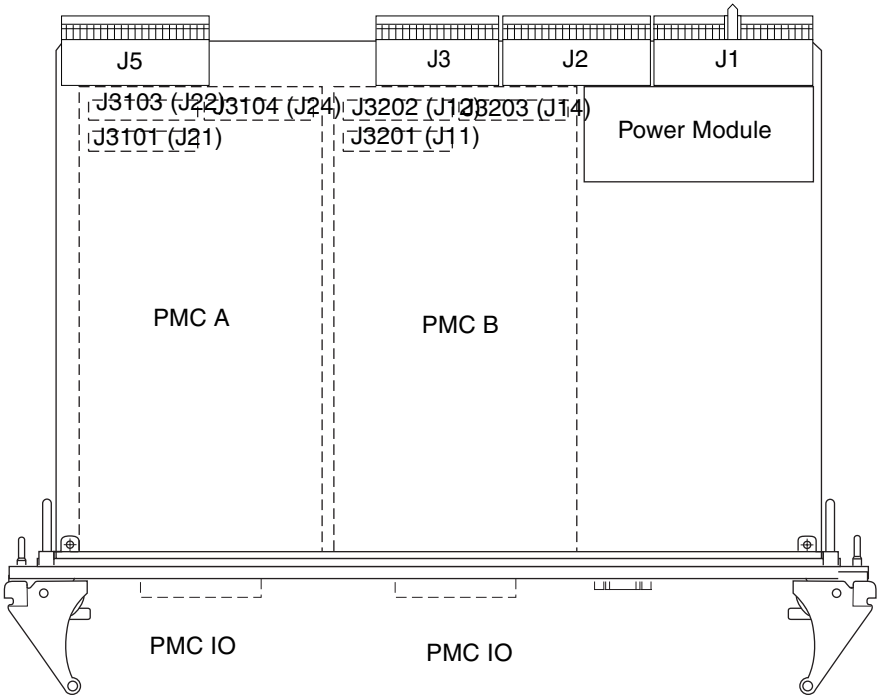


FIGURE B-1 Netra CP2160 Board PMC Port Connectors

B.1.1 PMC-A Interface

TABLE B-1 PMC-A J3101 (J21) Connector Interface

Pin	Description	Pin	Description
1	TCK; JTAG clock signal.	2	-12V
3	GND	4	PMC_A_INT_A_L
5	PMC_A_INT_B_L	6	PMC_A_INT_C_L

TABLE B-1 PMC-A J3101 (J21) Connector Interface *(Continued)*

Pin	Description	Pin	Description
7	PMC_BUSMODE1_L*	8	VCC (5V)
9	PMC_A_INT_D_L	10	NC
11	GND	12	NC
13	PMC_CLK	14	GND
15	GND	16	PMC_GNT_L
17	PMC_REQ_L	18	VCC
19	LOCAL_VIO	20	PCI_B_AD<31>
21	PCI_B_AD<28>	22	PCI_B_AD<27>
23	PCI_B_AD<25>	24	GND
25	GND	26	PCI_B_CBE3_L
27	PCI_B_AD<22>	28	PCI_B_AD<21>
29	PCI_B_AD<19>	30	VCC
31	LOCAL_VIO	32	PCI_B_AD<17>
33	PCI_B_FRAME_L	34	GND
35	GND	36	PCI_B_IRDY_L
37	PCI_B_DEVSEL_L	38	VCC
39	GND	40	PCI_B_LOCK_L
41	PMC_SDONE	42	PMC_SB0_L
43	PCI_B_PAR	44	GND
45	LOCAL_VIO	46	PCI_B_AD<15>
47	PCI_B_AD<12>	48	PCI_B_AD<11>
49	PCI_B_AD<9>	50	VCC
51	GND	52	PCI_B_CBE_L<0>
53	PCI_B_AD<6>	54	PCI_B_AD<5>
55	PCI_B_AD<4>	56	GND
57	LOCAL_VIO	58	PCI_B_AD<3>
59	PCI_B_AD<2>	60	PCI_B_AD<1>
61	PCI_B_AD<0>	62	VCC
63	GND	64	PCI_B_REQ64_L

* BUSMODE signals require a pull-up

TABLE B-2 PMC-A 31013 (J22) Connector Interface

Pin	Description	Pin	Description
1	+12V	2	JTAG_PMC_RST_L
3	TMS	4	PMC_TDO
5	PMC_TDI	6	GND
7	GND	8	NC
9	NC	10	NC
11	PMC_BUSMODE2_L	12	VDD (3.3V)
13	PCI_B_RST_L	14	PMC_BUSMODE3_L
15	VDD	16	PMC_BUSMODE4_L
17	NC	18	GND
19	PCI_B_AD<30>	20	PCI_B_AD<29>
21	GND	22	PCI_B_AD<26>
23	PCI_B_AD<24>	24	VDD
25	PCI_B_IDSEL	26	PCI_B_AD<23>
27	VDD	28	PCI_B_AD<20>
29	PCI_B_AD<18>	30	GND
31	PCI_B_AD<16>	32	PCI_B_CBE_L<2>
33	GND	34	NC
35	PCI_B_TRDY_L	36	VDD
37	GND	38	PCI_B_STOP_L
39	PCI_B_PERR_L	40	GND
41	VDD	42	PCI_B_SERR_L
43	PCI_B_CBE_L<1>	44	GND
45	PCI_B_AD<14>	46	PCI_B_AD<13>
47	GND	48	PCI_B_AD<10>
49	PCI_B_AD<8>	50	VDD
51	PCI_B_AD<7>	52	NC
53	VDD	54	NC
55	NC	56	GND
57	NC	58	NC

TABLE B-2 PMC-A 31013 (J22) Connector Interface *(Continued)*

Pin	Description	Pin	Description
59	GND	60	NC
61	PCI_B_ACK64_L	62	VDD
63	GND	64	NC

Note – P1386.1 standard reserves Jn3 64-pin connector for PCI 64-bit extensions. It is not fitted on these boards.

TABLE B-3 PMC-A 3104 (J24) Connector Interface

Pin	Description
1-64	PMC_A_IO<1-64> are user defined IO pins

B.1.2 PMC-B Interface

The PMC-B interface is comprised of four connectors. They are connectors J11, J12, and J14 which conform to the Common Mezzanine Card (CMC) specification and J13 which is proprietary I/O connections.

TABLE B-4 PMC-B 3201 (J11) Connector Interface on Netra CP2160

Pin	Description	Pin	Description
1	TCK; JTAG clock signal.	2	-12V
3	GND	4	PMC_B_INT_A_L
5	PMC_B_INT_B_L	6	PMC_B_INT_C_L
7	PMC_BUSMODE1_L	8	VCC (5V)
9	PMC_B_INT_D_L	10	NC
11	GND	12	NC
13	PMC_CLK	14	GND
15	GND	16	PMC_GNT_L
17	PMC_REQ_L	18	VCC

TABLE B-4 PMC-B 3201 (J11) Connector Interface on Netra CP2160 *(Continued)*

Pin	Description	Pin	Description
19	LOCAL_VIO	20	PCI_B_AD<31>
21	PCI_B_AD<28>	22	PCI_B_AD<27>
23	PCI_B_AD<25>	24	GND
25	GND	26	PCI_B_CBE3_L
27	PCI_B_AD<22>	28	PCI_B_AD<21>
29	PCI_B_AD<19>	30	VCC
31	LOCAL_VIO	32	PCI_B_AD<17>
33	PCI_B_FRAME_L	34	GND
35	GND	36	PCI_B_IRDY_L
37	PCI_B_DEVSEL_L	38	VCC
39	GND	40	PCI_B_LOCK_L
41	PMC_SDONE	42	PMC_SB0_L
43	PCI_B_PAR	44	GND
45	LOCAL_VIO	46	PCI_B_AD<15>
47	PCI_B_AD<12>	48	PCI_B_AD<11>
49	PCI_B_AD<9>	50	VCC
51	GND	52	PCI_B_CBE_L<0>
53	PCI_B_AD<6>	54	PCI_B_AD<5>
55	PCI_B_AD<4>	56	GND
57	LOCAL_VIO	58	PCI_B_AD<3>
59	PCI_B_AD<2>	60	PCI_B_AD<1>
61	PCI_B_AD<0>	62	VCC
63	GND	64	PCI_B_REQ64_L

TABLE B-5 PMC-B J3202 (J12) Connector Interface on Netra CP2160

Description	Pin	Pin	Description
+12V	1	2	JTAG_PMC_RST_L
TMS	3	4	PMC_TDO
PMC_TDI	5	6	GND
GND	7	8	NC

TABLE B-5 PMC-B J3202 (J12) Connector Interface on Netra CP2160 *(Continued)*

Description	Pin	Pin	Description
NC	9	10	NC
PMC_BUSMODE2_L	11	12	VDD (3.3V)
PCI_B_RST_L	13	14	PMC_BUSMODE3_L
VDD	15	16	PMC_BUSMODE4_L
NC	17	18	GND
PCI_B_AD<30>	19	20	PCI_B_AD<29>
GND	21	22	PCI_B_AD<26>
PCI_B_AD<24>	23	24	VDD
PCI_B_IDSEL	25	26	PCI_B_AD<23>
VDD	27	28	PCI_B_AD<20>
PCI_B_AD<18>	29	30	GND
PCI_B_AD<16>	31	32	PCI_B_CBE_L<2>
GND	33	34	NC
PCI_B_TRDY_L	35	36	VDD
GND	37	38	PCI_B_STOP_L
PCI_B_PERR_L	39	40	GND
VDD	41	42	PCI_B_SERR_L
PCI_B_CBE_L<1>	43	44	GND
PCI_B_AD<14>	45	46	PCI_B_AD<13>
GND	47	48	PCI_B_AD<10>
PCI_B_AD<8>	49	50	VDD
PCI_B_AD<7>	51	52	NC
VDD	53	54	NC
NC	55	56	GND
NC	57	58	NC
GND	59	60	NC
PCI_B_ACK64_L	61	62	VDD
GND	63	64	NC

TABLE B-6 PMC-B J3203 (J14) Connector Interface

Pin	Description
1-64	PMC_B_IO<1-64> are user defined IO pins

B.2 Front Panel Connectors

This section contains the connector pin assignments for the front panel I/O ports. For pin assignments on the transition card I/O, see the transition card manual.

B.2.1 Serial Connectors

One serial port is available through the front panel with a single-stacked 9-pin connector. One connector is assigned to Port A and the other connector to Port B.

Note – The user will need to provide mini din DB 9-pin serial cable to connect to the serial port.

TABLE B-7 shows the serial port A connector pin assignments.

TABLE B-7 Dual 9-Pin Mini D-Sub Connector Signal Assignments for Serial Port A

Pin	Signal
P1A	DCD A
P2A	RXD A
P3A	TXD A
P4A	DTR A
P5A	GND A
P6A	DSR A
P7A	RTS A
P8A	CTS A
P9A	RI A

B.2.2 Ethernet Connectors

TABLE B-8 shows the Ethernet connector A and B pin assignments.

TABLE B-8 Ethernet Connector A and B Pin Assignments

Ethernet Port A		Ethernet Port B	
PIn	**Signal**	**Pin**	**Signal**
1	TX (+)	1	TX (+)
2	TX (-)	2	TX (-)
3	RX (+)	3	RX (+)
4		4	
5		5	
6	RX (-)	6	RX (-)
7		7	
8		8	

B.3 CompactPCI Backplane Connectors

FIGURE B-2 shows contact numbering as seen from the back of the Netra CP2160 board.

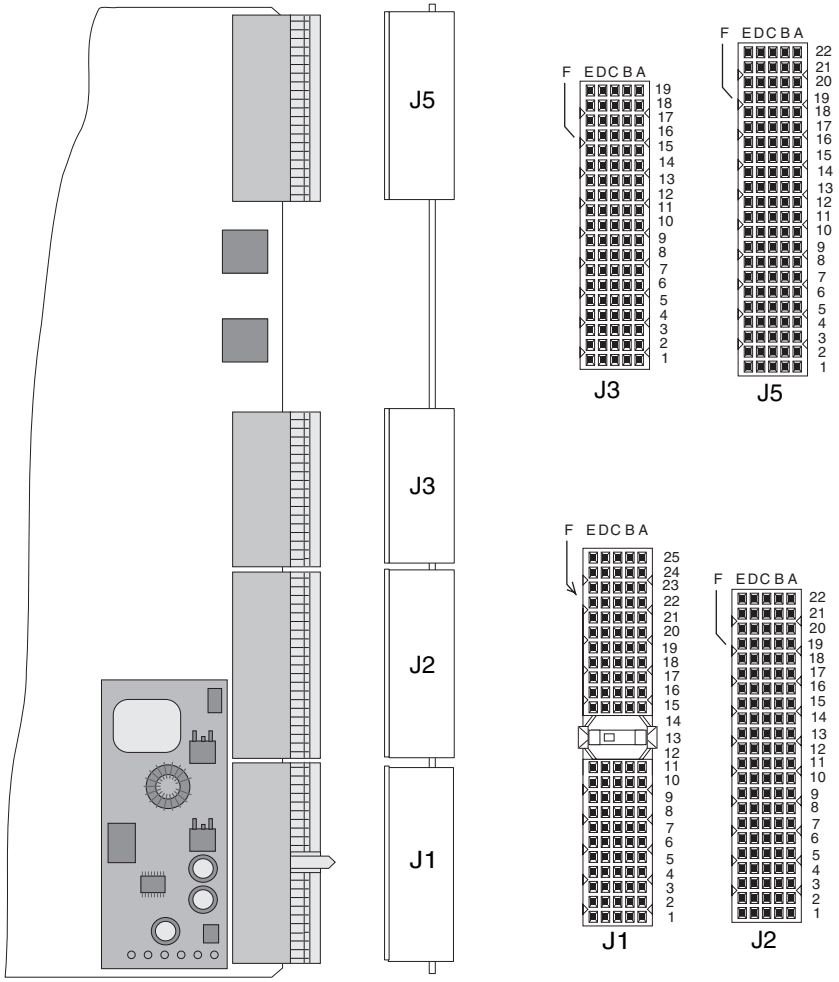


FIGURE B-2 CompactPCI Host Board Connector Contact Numbering

Note – A blue key on the J1 connector indicates a 5V PCI.

TABLE B-9 J1/P1 Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
25	GND	+5V	REQ64#	ENUM#	+3.3V	+5V	GND
24	GND	AD[1]	+5V	+5V	AD[0]	ACK64#	GND
23	GND	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND
22	GND	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
21	GND	+3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	+5V	AD[11]	AD[10]	GND
19	GND	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	+3.3V	PAR	C/BE[1]#	GND
17	GND	+3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	+5V	STOP#	LOCK#	GND
15	GND	+3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
14	Key						Key
13	Key						Key
12	Key						Key
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	+5V	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ0#	GND	+3.3V	CLK0	AD[31]	GND
5	GND			RST#	GND	GNT0#	GND
4	GND	IPMB_PWR	HEALTHY#	+5V			GND
3	GND	INTA#	INTB#	INTC#	+5V	INTD#	GND
2	GND		+5V				GND
1	GND	+5V	-12V		+12V	+5V	GND

Note – Gray fill indicates backplane long pin. Thick box border indicates short pin. All other pins are medium pins.

TABLE B-10 J2/P2 Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND				GND
20	GND	CLK5	GND		GND		GND
19	GND	GND	GND			ALERT	GND
18	GND				GND		GND
17	GND		GND	PRST#	REQ6#	GNT6#	GND
16	GND			DEG#	GND		GND
15	GND		GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	+5Va	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	+5Va	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	+5Va	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	+5Va	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#	GND	+5Va	C/BE[4]#	PAR64	GND
4	GND	+5V[a]		C/BE[7]#	GND	C/BE[6]#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

TABLE B-11 J3/P3 Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
19	GND	PMCB-1	PMCB-2	PMCB-3	PMCB-4	PMCB-5	GND
18	GND	PMCB-6	PMCB-7	PMCB-8	PMCB-9	PMCB-10	GND
17	GND	PMCB-11	PMCB-12	PMCB-13	PMCB-14	PMCB-15	GND
16	GND	PMCB-16	PMCB-17	PMCB-18	PMCB-19	PMCB-20	GND

TABLE B-11 J3/P3 Connector Pin Assignments *(Continued)*

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
15	GND	PMCB-21	PMCB-22	PMCB-23	PMCB-24	PMCB-25	GND
14	GND	PMCB-26	PMCB-27	PMCB-28	PMCB-29	PMCB-30	GND
13	GND	PMCB-31	PMCB-32	PMCB-33	PMCB-34	PMCB-35	GND
12	GND	PMCB-36	PMCB-37	PMCB-38	PMCB-39	PMCB-40	GND
11	GND	PMCB-41	PMCB-42	PMCB-43	PMCB-44	PMCB-45	GND
10	GND	PMCB-46	PMCB-47	PMCB-48	PMCB-49	PMCB-50	GND
9	GND	PMCB-51	PMCB-52	PMCB-53	PMCB-54	PMCB-55	GND
8	GND	PMCB-56	PMCB-57	PMCB-58	PMCB-59	PMCB-60	GND
7	GND	PMCB-61	PMCB-62	PMCB-63	PMCB-64	V I/O	GND
6	GND				GPIO1	GPIO2	GND
5	GND				BKRST# OUT	BKRST# IN	GND
4	GND				SMC RX	SMC TX	GND
3	GND			VISA RST#	PCI-B RST#		GND
2	GND						GND
1	GND			BP_XIR_L			GND

Note – The J4 connector is not populated on the Netra CP2160 boards.

TABLE B-12 J5/P5 Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	PMCA-5	PMCA-4	PMCA-3	PMCA-2	PMCA-1	GND
21	GND	PMCA-10	PMCA-9	PMCA-8	PMCA-7	PMCA-6	GND
20	GND	PMCA-15	PMCA-14	PMCA-13	PMCA-12	PMCA-11	GND
19	GND	PMCA-20	PMCA-19	PMCA-18	PMCA-17	PMCA-16	GND
18	GND	PMCA-25	PMCA-24	PMCA-23	PMCA-22	PMCA-21	GND
17	GND	PMCA-30	PMCA-29	PMCA-28	PMCA-27	PMCA-26	GND
16	GND	PMCA-35	PMCA-34	PMCA-33	PMCA-32	PMCA-31	GND
15	GND	PMCA-40	PMCA-39	PMCA-38	PMCA-37	PMCA-36	GND
14	GND	PMCA-45	PMCA-44	PMCA-43	PMCA-42	PMCA-41	GND
13	GND	PMCA-50	PMCA-49	PMCA-48	PMCA-47	PMCA-46	GND

TABLE B-12 J5/P5 Connector Pin Assignments *(Continued)*

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
12	GND	PMCA-55	PMCA-54	PMCA-53	PMCA-52	PMCA-51	GND
11	GND	PMCA-60	PMCA-59	PMCA-58	PMCA-57	PMCA-56	GND
10	GND		PMCA-64	PMCA-63	PMCA-62	PMCA-61	GND
9	GND	RTS A	DTR A	RI A	GND	CTS A	GND
8	GND	DCD A	TXD A	RXD A	DSR A	+5V	GND
7	GND	RTS B	DTR B	RI B	DSR B	CTS B	GND
6	GND	DCD B	TXD B	RXD B	GND	GND	GND
5	GND	I2C_SCL		-12V	ENET1 RX (+)	ENET1 RX (-)	GND
4	GND	I2C_SDA	I2C_PWR	GND	ENET1 TX (+)	ENET1 TX (-)	GND
3	GND	USB2 (+)	USB2 (-)	GND	GND	GND	GND
2	GND	USB1 (+)	USB1 (-)	GND	ENET0 RX (+)	ENET0 RX (-)	GND
1	GND	GND	+3.3V	+12V	ENET0 TX (+)	ENET0 TX (-)	GND

B.4 Switch Settings

A set of switches SW2501 and SW4101 are located between the heatsink and the front panel (see FIGURE B-3 for switch locations and direction of the arrows).

TABLE B-13 SW2501 Switch Settings

Switch #	Setting	Description	Default
1	Switch closed (in direction of arrow)	When switch is closed, boot flash is programmable	Yes

TABLE B-13 SW2501 Switch Settings

Switch #	Setting	Description	Default
	Switch open	When switch is open, boot flash is not programmable	No
2	Switch closed (in direction of arrow)	When switch is closed, the user flash is detected during OBP boot and the user flash is write enabled	Yes
	Switch open	When switch is open, the user flash is not detected during OBP boot and the write-protect switch for user flash is enabled.	No

TABLE B-14 SW4101 Switch Settings

Switch #	Setting	Description	Default
1	Switch closed	Reserved	Yes
	Switch open	Leave the switch in the default position - do not move it to the open position.	No
2	Switch closed (in direction of arrow)	Always boot from (main) boot flash	Yes
	Switch open	Check SMC configuration block setting Byte 7 bits <3:2>*	No

* Check TABLE B-15 for details.

TABLE B-15 SMC Configuration Block Setting Options; Byte 7 bits <3:2>

Boot Device Setting			
User Flash	**ROMBO**	**User Flash**	**Main Flash**
00	01	10	11
0..16MB=UF	0..4MB=RB	0..8MB=UF	0..4MB=BF
	4..12MB=UF	8:12MB=BF	4..12MB=UF
	12..16MB=BF	12..16MB=RB	12..16MB=RB

For details on SMC Configuration Block Setting see Section 4.7.2, "SMC Configuration Block" on page 4-20.

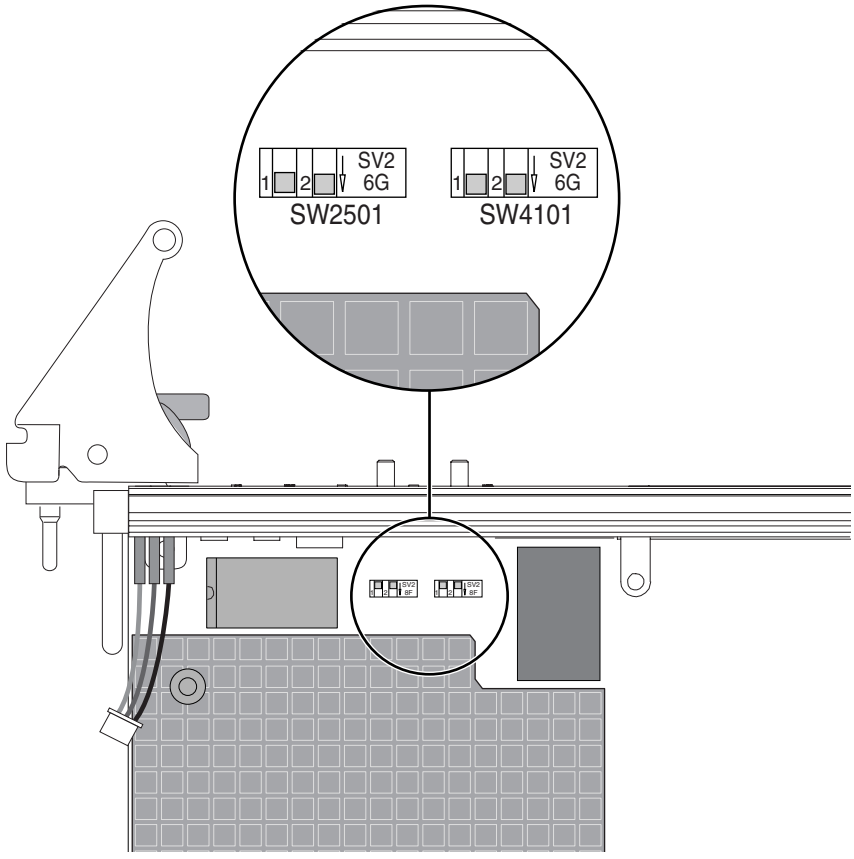


FIGURE B-3 Switches SW2501 and SW4101 on the Netra CP2160 Board

APPENDIX **C**

Solaris Sun FRU ID

The Solaris Sun FRU ID information is stored on a Netra CP2160 board EEPROM and is used to identify the board for service purposes. The Solaris Sun FRU ID is one of the standard features in the Solaris 8 2/02 operating environment and later compatible versions. The *CP2000 Supplemental 4.0 CD for Solaris 8* implements Solaris Sun FRU ID for the CP2160 board, when used with Solaris 8 update 2/02 and later compatible versions.

To access the Solaris Sun FRU ID infomation for a board, use the `prtfru` command. See the `prtfru(1M)` man pages for futher infomation on this command. The man pages can be found on the Solaris 8 2/02 operating environment default package.

C.1 `prtfru` Command

By typing in the `prtfru` command at the Solaris command line, the user can obtain an output with Solaris Sun FRU ID information that is similar to the output shown in the following code example. The fields that are displayed in the example are described below in TABLE C-1.

```
# prtfru
/frutree
/frutree/chassis (fru)
/frutree/chassis/CPU-slot?Label=CPU
/frutree/chassis/CPU-slot?Label=CPU/CPU-slot
(container)
   SEGMENT: SD
      /ManR
     /ManR/UNIX_Timestamp32: Fri May 11 19:00:00 PDT
2001
      /ManR/Fru_Description:
      /ManR/Manufacture_Loc:
      /ManR/Sun_Part_No: 375-302
      /ManR/Sun_Serial_No: 001379
      /ManR/Vendor_Name: Sun Microsystems
      /ManR/Initial_HW_Dash_Level:
      /ManR/Initial_HW_Rev_Level:
      /ManR/Fru_Shortname: CP2160
/frutree/chassis/CPU-slot?Label=CPU/CPU-
slot/c0?Label=c0
#
```

TABLE C-1 Description of Fields in Typical `prtfru` Command Display Output

Field	Description
/ManR/UNIX_Timestamp32: Fri May 11 19:00:00 PDT 2001	Board manufacturing timestamp
/ManR/Fru_Description:	Description for the board field replaceable unit
/ManR/Manufacture_Loc:	Location where board is manufactured
/ManR/Sun_Part_No: 375-302	Board identification part number
/ManR/Sun_Serial_No: 001379	Board identification serial number

TABLE C-1 Description of Fields in Typical `prtfru` Command Display Output

Field	Description
/ManR/Vendor_Name: Sun Microsystems	Name of the board vendor
/ManR/Initial_HW_Dash_Level:	Board identification dash number
/ManR/Initial_HW_Rev_Level:	Board identification revision number
/ManR/Fru_Shortname: CP2160	Short name for the board such as CP2160

APPENDIX **D**

Bibliography

D.1 General References

The following books and specifications are referenced that relate the Netra CP2160 board design.

D.1.1 Books and Specifications

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D.2 Sun Microsystems Publications

These books and papers are available in printed form, and some are also available through the World Wide Web.

The docs.sun.com[SM] Web site enables you to access Sun technical documentation online. You can browse the docs.sun.com archive or search for a specific book title or subject. The URL is `http://www.sun.com/documentation`

D.2.1 Solaris Operating Environment

Solaris 8 (SPARC Platform Edition) Installation Guide, Part No. 806-0955-*xx*

Solaris 8 Advanced Installation Guide, Part No. 806-0957-*xx*

Solaris 8 System Administration Supplement, Part No. 806-6611-*xx*

System Administration Guide, *Volume 1*, Part No. 805-7228-*xx* (contains chapters on device management and configuring devices—presently deals with hot- plug considerations).

System Administration Guide, Volume 2, Part No. 805-7228-*xx* (of general interest)

System Administration Guide, Volume 3, Part No. 805-7228-*xx* (of general interest)

man pages section 1M: System Administration Commands, Part No. 806-0625-*xx* (covers `cfgadm` command; see above discussion on hot-swap support in the reference to the *System Administration Guide, Volume 1*.)

OpenBoot 4.x Command Reference Manual, Part No. 816-1177-*xx*

Writing FCode 3.x Programs, Part No. 806-1379-*xx* February 2000, Rev

OpenBoot 3.x Quick Reference, Part Number 806-2908-10, February 2000, Revision A

Solaris Naming Administration Guide, Part No. 806-1387-*xx*

Solaris Naming Setup and Configuration Guide, Part No. 806-1386-*xx*

Writing Device Drivers, Part No. 805-7378-*xx* (includes information about the device tree)

D.2.2 Alternate Pathing

These documents can be read for an approximation of the installation procedure that will apply to the CP2000 HA platform.

Sun Enterprise Server Alternate Pathing 2.3 User Guide, Part No. 806-1933-*xx*

Sun Enterprise Server Alternate Pathing 2.3 Reference Guide, Part No. 806-1934-*xx*

D.2.3 Processors and Integrated Circuits

Advanced PCI Bridge Users Manual, Part No. 805-1251-*xx*

D.2.4 CP2000/CP2160 Family System Documents

Refer to the following web site to access the Netra CP2160 documentation, as well as the other Netra CP2000/CP2100 board documentation.

`http://www.sun.com/products-n-solutions/hardware/docs/CPU_Boards`

Glossary

The terminology used in this glossary conforms to PICMG and Telco industry terminology.

Glossary Listing

Advanced System Monitoring (ASM) The provision of hardware status information to the user or application program to enable an orderly shut down to be made before a hardware failure causes any damage.

Alternate Pathing (AP) Asoftware-driven facility that employs both redundant hardware and redundant software driver paths between a server and a disk subsystem or a network. If one path fails, AP can ensure that the disk subsystem or network is still available through the alternate path. For example, the alternate path can be a second port on an interface board, or an entirely separate interface board. See also Dynamic Reconfiguration.

availability The ratio of the total time that a functional unit can be used to the total time that the unit is required for use.

Baseboard Management Controller (BMC) Manages chassis environmental, configuration and service functions and receive event data from other parts of the system. It can receive data through sensor interfaces, and interprets these data by using the sensor data repository (SDR) to which it provides an interface. The BMC maintains and provides an interface to the system event log (SEL). The BMC allows both the SDR and the SEL to be accessed from the system or from the intelligent platform management bus (IPMB). A typical function of the BMC is to measure

processor temperature, power supply values, and cooling fan status. It can take some autonomous actions to preserve system integrity. For example, it might switch on a fan at a particular temperature threshold. An application interface may be provided to enable custom user-management applications to be built. The BMC describes an abstract function, or role. It carries no definition of how the role might be implemented.

checkpoint (1) A point at which information about the status of a job and the system can be recorded so that the job can later be restarted from that point. (2) A sequence of instructions in a computer program for recording the status of execution for restarting.

CompactPCI (CPCI) An adaptation of the PCI bus architecture defined in the *Peripheral Component Interconnect Specification 2.1* (or later) to an electrically-compatible robust industrial form. This form specifies an Eurocard-style circuit board assembly that uses "hard metric" connectors to connect it to the enclosure backplane. CompactPCI is an open specification supported by the PCI Industrial Computers Manufacturers' Group (PICMG).

CompactPCI bridge The PCI bridge between the system host processor and the CompactPCI bus. The CompactPCI bridge must reside in the system slot to provide CompactPCI clocking and arbitration that are only available from that slot. CompactPCI Bridges must be controllable by the system management controller to turn off clocks and arbitration.

Device Reconfiguration (DR) A process that is used in the CP2000 system to configure (add) or deconfigure (remove) device tree allocations and load or unload software driver modules while the system is running. It is analogous to *Dynamic Reconfiguration* that is used on some Sun high-end server systems with the important differences: it is not used to reconfigure memory or CPU resources and it can be used automatically in the full hot-swap and HA hot-swap cases when the hot-swap framework software is prompted by the System Management Controller. CP2000 HA device reconfiguration can also be invoked manually from a console.

domain That part of a computer network in which the data processing resources are under common control. See *PCI Domain.*

dropin A dropin is a code or data module that can be called by the OpenBoot PROM during system startup. It is placed in unused memory space between OpenBoot PROM and OpenBoot PROM. Most user-created dropins are used to initialize custom user hardware. They do not require that the user possesses OpenBoot PROM source code; only the binary OpenBoot PROM image need be licensed. Dropins are used to add firmware drivers for user hardware.

Dynamic Reconfiguration (DR) A software package that enables the administrator to (1) view a system configuration; (2) suspend or restart operations involving a port, storage device, or board; and (3) reconfigure the system (detach or attach hot-swappable devices such as disk drives or interface boards) without the need to power down the system. When DR is used with Alternate Pathing or Solstice DiskSuite software (and redundant hardware), the server can continue to communicate with disk drives and networks without interruption while a service provider replaces an existing device or installs a new device. DR supports replacement of a CPU/memory board, provided the memory on the board is not interleaved with memory on other boards in the system. Note that DR is used with Sun high-end server systems. See *Device Reconfiguration* for the analogous process that is applied to CP2000-based systems.

failover The transfer of function from a failed component subsystem to an alternate one while preserving the operational state of the overall system. The functions transferred may include those of control and management.

firmware An ordered set of instructions and data that is stored in a way that is functionally independent of main storage, for example, microprograms stored in a read-only memory (ROM). The term *firmware* describes microcode in ROM. At the time they are coded, microinstructions are software. When they are put into ROM they become part of the hardware (microcode) or a combination of hardware and software (microprograms). Usually, microcode is permanent and cannot be modified by the user.

Field Replaceable Unit (FRU) A part or subsystem that may be replaced in the field or at a customer-site. Parts that are not FRUs are only factory replaceable.

Gigabit Media-independent Interface (GMII) An Ethernet network specification that defines a standard 1000-megabit interface between the MAC layer and either of the physical layers: 1000BASE-X (fiber-channel family) or 1000BASE-T (UTP). The GMII accommodates these physical layers without having to modify the upper layers (that is, the protocol stacks) for the particular transmission medium. The GMII is defined in IEEE Std. 802.3z–1998, which is included in IEEE Std. 802.3–1998.

handover Synonymous with *switchover*. The transfer of function from a component subsystem to an alternate one while preserving the operational state of the overall system. The functions transferred may include those of control and management. Handover occurs when there is no failure in the system to prompt the transfer (compare *failover).*

heartbeat A repetitive signal passed from one system to another to communicate the state of integrity or “health” of the sending system.

High Availability (HA) The property of a system associated with a high in-service to out-of-service time ratio. This property can be engineered by reconfiguring the system "on the fly" to isolate failed elements so they can be replaced without affecting the operational condition.

host computer (1) A computer that usually performs network control functions and provides end-users with services such as computation and database access.
(2) The primary or controlling computer in a multicomputer installation.

hot-plug A slot must be powered down and isolated from the bus before an adapter card can be inserted. The hot-plug specification requires that board power be controlled and that means be provided to set or maintain the board in a quiescent state prior to its insertion or removal.

The method of putting the board in a quiescent state or of controlling power application to it is not defined in hot-plug but is left to the system manufacturer. The hot plug interface is defined by the PCISIG—see the hot-plug specification in the Bibliography.

hot-swap The ability of a system element to be removed or replaced while the system hardware is nominally operating under power. This ability is usually invoked after a failure and is implemented by a sequence that steers the functions of the element to other parts of the system.

Hot-swap, as defined by PICMG, can be classified as basic, full, or HA. Basic hot-swap requires manual software sequencing to bring a card out of commission. Full hot-swap uses hardware enumeration signals to indicate board status. Software automatically decommissions the card. HA hot-swap provides for a fully automated decision tree and use of software and a System Management Controller/Hot-Swap Controller to decommission or commission a card.

hot-swap controller The controller that takes care of the low-level sequencing associated with hot-swap.

Inter-Integrated Circuit Bus (I2C) A serial bus developed by Philips for inter-package communications and typically used by them in TV sets. In Sun CompactPCI systems, it is used to link card elements in a system for management communications.

Inter-Chassis Management Bus (ICMB) An IPMI/I^2C bus (analogous to the IPMB) used to accomplish chassis-to-chassis management.

Inter-Host Bus (IHB) An IPMI/I^2C bus (the IPMB) used for direct communications between controllers on host boards.

Input/output (I/O) Applies to system peripheral signals.

Intelligent platform management bus (IPMB) A bus that carries serial communication signals that comply with the IPMI; it is used to communicate between CompactPCI circuit boards in a chassis.

Intelligent Platform Management Interface (IPMI) A protocol interface with a protocol stack that includes link, transport, and session layers to provide reliability. IPMI resides on an I^2C physical layer.

Keyboard Control Style interface (KCS interface) One of the BMC to System Management Software (SMS) interfaces as defined in the IPMI specification (see the Bibliography).

LVD SCSI A version of the SCSI bus that uses LVTTL (3.3 V) differential logic technology, this bus is currently specified with an 80 MHz maximum transfer rate and a maximum cable length of 18 ft.

Medium Access Control (MAC Address Synonymous with Ethernet address. The MAC address is a 48-bit address used to direct data-link layer transactions.

Media-Independent Interface (MII): A specification that defines a standard interface between the MAC layer and any of the three physical layers: 100BASE-TX, 100BASE-T4, or 100BASE-FX. It can support both 10 Mbps and 100 Mbps data rates. Since the electrical signals are clearly defined, the MII may be implemented internally or externally in a network device.

nexus A nexus driver supports a bridging connection for communication between devices on separate buses. These devices can be arranged in a hierarchal tree configuration with a number of bridges. In this case a nexus driver is associated with each bridge to handle communications with adjacent levels in the hierarchy.

nines Used as a measure of system availability: three nines > 99.9% availability, four nines > 99.99%, five nines > 99.999%; six nines > 99.9999%; ...

Node An addressable point on a network. Each node in a Sun network has a different name. A node can connect a computing system, a terminal, or various other peripheral devices to the network.

Non-transparent bridge (NTB) 21555

OpenBoot PROM The OpenBoot PROM, or system PROM, contains code to run POST and a suite of user-accessible subsystem hardware tests. It has a Forth interpreter for custom user routines. Under a normal boot sequence, it provides a path to a system boot device which is accessed after POST completes. “Open Firmware” is controlled by IEEE Standard 1275.

PCI domain The functional entity that includes a host—usually with a host PCI bridge—and the peripherals that it controls. The domain does not necessarily uniquely include the PCI bus because this bus can be shared by multiple domains. For example, a second domain can comprise a second host/bridge element that controls a different set of peripherals on a shared bus. Separation and management of the domains is implemented by a controlling system mechanism that guarantees their mutual protection.

peripheral host See *satellite host*

PICMG PCI Industrial Computers Manufacturers' Group.

PCI mezzanine card (PMC) A PMC card fits into a special PCI-bus connector designed to attach compact peripherals. These peripherals may decode a variety of IO functions from this bus.

Power-on Self Test (POST) A suite of tests run out of system firmware before any other code is loaded. The purpose of such testing is to check the integrity of the hardware before loading a software system.

Reverse Address Resolution Protocol (RARP) The protocol broadcasts a MAC (ethernet) address and receives an IP address in response from a RARP server.

Reliability, Availability and Serviceability (RAS) The general concepts associated with high in-service time systems and their simplicity of maintenance.

reliability The ability of a functional unit to perform a required function under stated conditions for a stated period of time.

remote management The action of managing a system or group of systems from a physically distant location. Remote management of Sun systems may be performed using the *Sun Management Center* application.

satellite board See *satellite host*.

satellite host Synonymous with *peripheral host* and *satellite board*. A satellite host performs independent tasks in response to commands from the system host. The satellite host has no accessible PCI space and is limited to controlling its own on-board I/O.

sensor data repository (SDR) The database that the BMC uses to determine what sensors, FRU devices, and management controllers are in the system. This database contains an account of sensor locations, properties, and associations.

segment The extent to which a backplane and cards combination can be extended by accounting for signal loading. In CompactPCI, a segment spans a maximum of eight card slots, beyond which some bridge elements (system bridge) are needed to provide expansion into another segment.

system event log (SEL) The database of measured values and events that is created by the BMC based upon its sensor monitoring. This database resides in the host and is accessible by high-level applications.

serviceability The capability of performing effective problem determination, diagnosis, and repair on a data-processing system.

shelf A single physical computing system composed of one or more CompactPCI bus segments. Electrical limitations of the bridging interfaces may require that the segments be in close proximity.

switchover See *Handover.*

system board computer The processor board that connects to a backplane system slot.

system host A system host accepts interrupts and owns peripherals. It executes user applications and decides the distribution of tasks within a system. In Hot-Swap systems the system host acts as a traffic router and functions to activate and deactivate peripheral cards (plug-in boards). It is not a CompactPCI requirement that the system host reside in a system slot, although this is normally the case. If the board resides in a peripheral slot that slot must be wired to receive peripheral interrupts from the backplane.

system management bus A serial bus that carries data and control signal between System Management Controllers on peripheral boards and devices. Communications on this bus use the IPMI protocol over an I^2C hardware layer.

System Management Controller (SMC) There is a System Management Controller (SMC) on each card in the enclosure. One of these cards either assumes control by command or takes control after negotiation with the other System Management Controllers. The System Management Controller manages peripherals to improve the availability of the system. Through the IPMB, this entity receives information on IDs of, or problems with, cards in the system and can communicate that information with other cards or with a system host via another bus. The SMC can switch the PCI bridge, PCI arbitration, and PCI clocking on or off.

system slot The card location in an enclosure that provides for CompactPCI clocking and arbitration. The CompactPCI bridge, which supplies these functions, must be in the system slot.

system-slot bridge Provides clocks and arbitration. This device must be controllable from somewhere, including a controller. The system host need not reside on the same card but the card that performs the function of system host must be able to talk to the slot containing the system-slot bridge.

takeover See *failover.*

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