Netra™ CP2500 Board Installation and Technical Reference Manual

Sun Microsystems, Inc.
www.sun.com

Part No. 819-1747-11
March 2007, Revision A

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Preface

The *Netra CP2500 Board Installation and Technical Reference Manual* describes how to install and configure the Netra™ CP2500 board. This document is written for system integration engineers, field application engineers, service engineers, and other professionals involved in the integration of these boards into systems.

How This Document Is Organized

Chapter 1 presents an overview of the Netra CP2500 board.

Chapter 2 provides the hardware configuration and installation tasks.

Chapter 3 provides instructions on the software configuration.

Chapter 4 gives information on the firmware.

Chapter 5 contains hardware service procedures.

Appendix A lists the board specifications.

Appendix B defines the board connector pinouts.

Using UNIX Commands

This document might not contain information about basic UNIX® commands and procedures such as shutting down the system, booting the system, and configuring devices. Refer to the following for this information:

- Software documentation that you received with your system
- Solaris™ Operating System documentation, which is at:

  http://docs.sun.com

Shell Prompts

Shell	Prompt
C shell	*machine-name*%
C shell superuser	*machine-name*#
Bourne shell and Korn shell	$
Bourne shell and Korn shell superuser	#

Typographic Conventions

Typeface*	Meaning	Examples
AaBbCc123	The names of commands, files, and directories; on-screen computer output	Edit your .login file. Use ls -a to list all files. % You have mail.
AaBbCc123	What you type, when contrasted with on-screen computer output	% **su** Password:
AaBbCc123	Book titles, new words or terms, words to be emphasized. Replace command-line variables with real names or values.	Read Chapter 6 in the *User's Guide*. These are called *class* options. You *must* be superuser to do this. To delete a file, type rm *filename*.

* The settings on your browser might differ from these settings.

Related Documentation

The documents listed as online are available at:

http://www.sun.com/documentation

Application	Title	Part Number	Format	Location
Board installation and reference	*Netra CP2500 Board Installation and Technical Reference Manual*	819-1747	PDF HTML	Online
Board news and updates	*Netra CP2500 Board Release Notes*	819-1748	PDF HTML	Online
Programming	*Netra CP2500 Board Programming Guide*	819-1749	PDF HTML	Online
Safety information	*Important Safety Information for Sun Hardware Systems*	816-7190	Printed	Shipping kit
Safety and compliance	*Netra CP2500 Board Safety and Compliance Manual*	819-1750	PDF HTML	Online
Rear transition module installation and reference	*Netra CP2500 Rear Transition Module Installation and Technical Reference Manual*	819-1753	PDF HTML	Online

Documentation, Support, and Training

Sun Function	URL
Documentation	http://www.sun.com/documentation/
Support	http://www.sun.com/support/
Training	http://www.sun.com/training/

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You can obtain more information about PCI specifications at the PCI Industrial Computer Manufacturer Group (PICMG®) web site:

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Please include the title and part number of your document with your feedback:

Netra CP2500 Board Installation and Technical Reference Manual,
part number 819-1747-11

CHAPTER 1

Netra CP2500 Board Overview

The Netra CP2500 board is a crucial building block that network equipment providers (NEPs) and carriers can use when scaling and improving the availability of carrier-grade systems. Based on industry standards, the Netra CP2500 board provides high performance and is powered by a UltraSPARC® IIIi processor. The board enables you to add a third-party PCI mezzanine card (PMC) to tailor solutions to your specific application needs.

When replacing the Netra CP2140 host and Netra CP2160 satellite CompactPCI (cPCI) boards in the Netra CT 410 and 810 servers, the Netra CP2500 board provides a sizeable increase in Netra CT server performance.

The Netra CP2500 board provides PCI Industrial Computers Manufacturers' Group (PICMG) CompactPCI Packet Switched Backplane (cPSB) compliance. To meet the requirements of the communications and service provider environments, the board is NEBS Level 3 compliant, and the Netra CT 410 and 810 servers remain NEBS Level 3 certified with the Netra CP2500 board installed.

This chapter contains the following sections:

1.1 Netra CP2500 Board Features

The Netra CP2500 board is a single-board computer designed for high-performance, embedded, compute density applications. The Netra CP2500 board has system management controller (SMC) capability that supports hot-swap operations, system management, and environmental monitoring. Powered by a UltraSPARC IIIi processor and including on-board I/O and one PMC slot, the Netra CP2500 board is an ideal platform for NEPs to use for a wide variety of Solaris Operating System applications.

FIGURE 1-1 displays an illustration of a typical Netra CP2500 board, and TABLE 1-1 lists a summary of the board features.

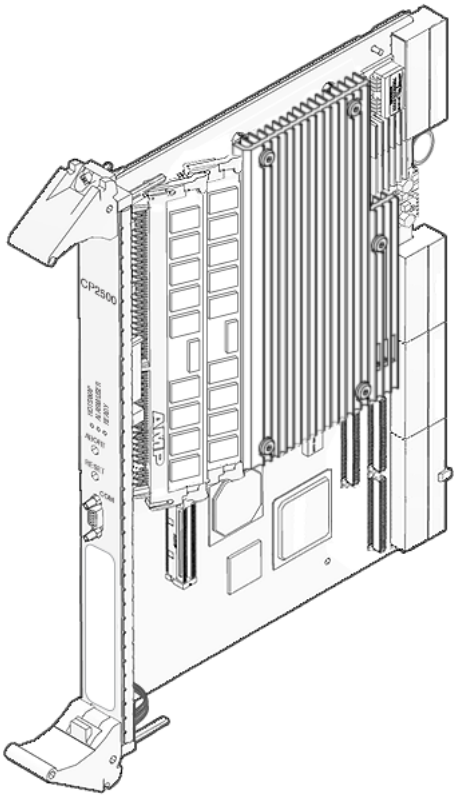

FIGURE 1-1 Typical Netra CP2500 Board

TABLE 1-1 Feature Summary

Feature	Description
CPU	UltraSPARC IIIi processor with 1 Mbyte L2 cache
Memory	Two 184-pin memory slots available for Sun-supplied, 0.72-inch DDR-1 very low-profile (VLP) DIMMs. Total memory capacity is 2 Gbytes using two 1 Gbyte DIMMs.
Power requirement	Estimated at 55 W (typical) and 65 W (peak maximum) with a RTM and two 1.0 GByte DIMMs installed. (The power requirements exclude PMC power.)
PICMG and PCI compatibility	• PICMG 2.0 R3.0 CompactPCI bus specification for 33 MHz PCI speed • PICMG 2.1 R2.0 Hot-Swap Specification* • PICMG 2.10 R1.0 Keying of cPCI boards and backplanes • PICMG 2.16 R1.0 CompactPCI packet switching backplane • PICMG 2.3 R1.0 PMC on CompactPCI Tables 1 and 3 • PICMG 2.9 R1.0 System Management Specification • PMC Specification P1386 Draft 2.4 • CMC P1386 Draft 2.4 Standard for CMC
cPSB node board support	The board functions as a cPSB node board in a cPSB chassis with the appropriate Solaris Operating System software installed.
cPCI host-mode support	The board functions as a system host board when installed in the host slot of a Netra CT 410 or 810 server with the appropriate Solaris Operating System software installed
cPCI satellite mode support	The board functions as a satellite board when installed in Netra CT 410 or 810 server with the appropriate Solaris Operating System software installed.
IPMI system management	Uses IPMI communications with Baseboard Management Controller (BMC); performs environmental monitoring on local board interface for example temperature sense, FRU ID, and control.
Hot-swap support	Basic and full hot-swap support. High-availability (HA) hot-swap support when used as a cPSB node board, Netra CT 410 or 810 satellite or host cPCI board.
Operating system	Solaris 9 Operating System
Front I/O and connectors	• One PMC slot • One serial port (can only be used if rear serial port COM A is not used)

TABLE 1-1 Feature Summary *(Continued)*

Feature	Description
Rear transition modules (RTM) connectors (optional) RTM-H	CompactPCI rear transition module host card (referred to in this document as RTM-H). The RTM-H is only supported in Netra CT 410 and 810 servers, and contains the following features: • Four 10/100 Ethernet ports • Two serial ports (One is mutually exclusive with the front panel serial connector) • Two internal SCSI connectors on the J4 and J5 connectors provided by the dual PCI to SCSI controller in a Netra CT 410 or 810 server (not accessible from the rear panel)
RTM-S	CompactPCI rear transition module satellite card (referred to in this document as RTM-S). While in cPCI mode, the RTM-S is supported in Netra CT 410 and 810 servers only. However, you can set mechanical DIP switches on the Netra CP2500 board and the RTM-S card to enable the Netra CP2500 board to be used as a node board in a cPSB chassis: • Four 10/100 Ethernet ports • Two serial ports (one is mutually exclusive with the front panel serial connector)
PMC I/O	Provision for adding one independent hardware vendor (IHV) supplied PMC expansion ports on front panel.
Watchdog timer	Two-level watchdog timer
NVRAM	8 Kbyte nonvolatile serial I^2c EEPROM (SEEPROM) to save OpenBoot™ PROM configuration.
Flash memory	Single 16 Mbyte flash memory, divided into: • 2 Mbyte system flash • 14 Mbyte user flash
NEBS	NEBS Level 3 compliant; Netra CT 410 and 810 servers remain NEBS Level 3 certified with installed Netra CP2500 boards installed.
Flash update	Flash memory can be updated from downloaded files.

* The Netra CP2500 blue hot-swap LED is in a noncompliant location.

Note – Sun does not support installing a PMC interface module (PIM) device on either the RTM-S or the RTM-H.

Note – For EMI compliance of the front access ports, use shielded cables on all I/O ports. The shields for all shielded cables must be terminated on both ends.

1.2 Netra CP2500 Board System Configurations

The Netra CP2500 board can be installed in the host or a satellite slot of a Netra CT 410 or 810 CompactPCI server, as shown in FIGURE 1-2 and described in TABLE 1-2. Refer to the Netra CT 410 and 810 server documentation for information about installing and using the Netra CP2500 board in a Netra CT server.

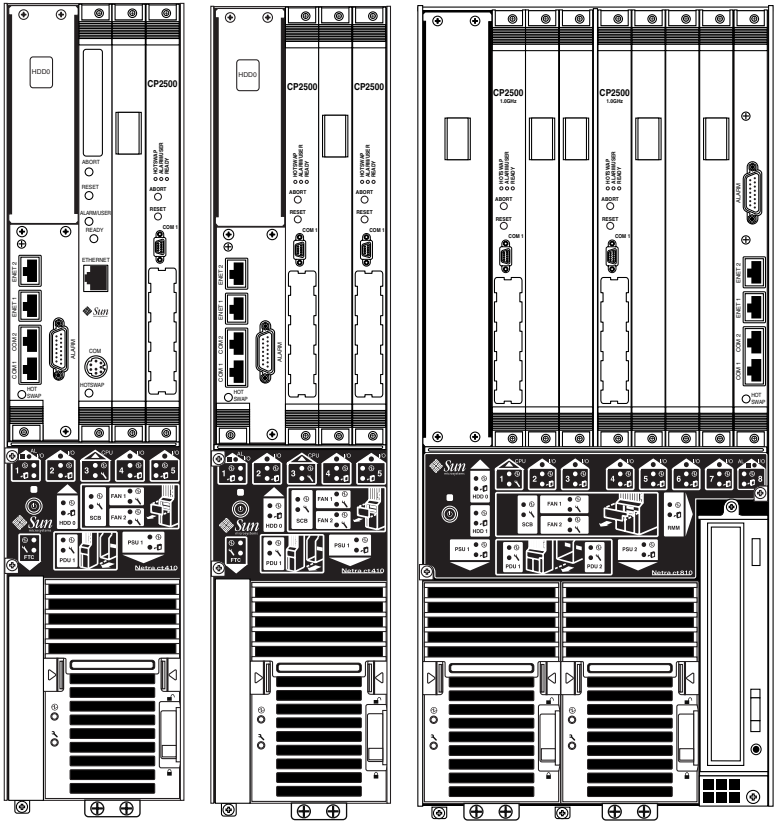

FIGURE 1-2 Netra CP2500 Boards Installed in Netra CT 410 and 810 Servers

TABLE 1-2 Netra CP2500 Board Role Examples

Callout Number	Netra Board and Role in Netra CT Server
1	Netra CP2140 board as a host board in a Netra CT 410 server
2	Netra CP2500 board as a satellite board in a Netra CT 410 server
3	Netra CP2500 board as a host board in a Netra CT 410 server
4	Netra CP2500 board as a satellite board in a Netra CT 410 server
5	Netra CP2500 board as a host board in a Netra CT 810 server
6	Netra CP2500 board as a satellite board in a Netra CT 810 server

The Netra CP2500 board can also be mounted in various cPSB enclosures, such as those shown in FIGURE 1-3 and FIGURE 1-4.

You can deploy the Netra CP2500 boards in a number of cPSB configurations to suit your specific requirements. For example, the board can be configured to boot from a network as a diskless client over either a cPSB backplane network or an RTM Ethernet network connection. Alternatively, the Netra CP2500 board can be purchased with an installed PMC hard drive, which can provide local disk support I/O and may optionally be used as a boot path. The installation procedure is independent of the type of enclosure, whether a floor-mounting rack or a bench-top cabinet is used.

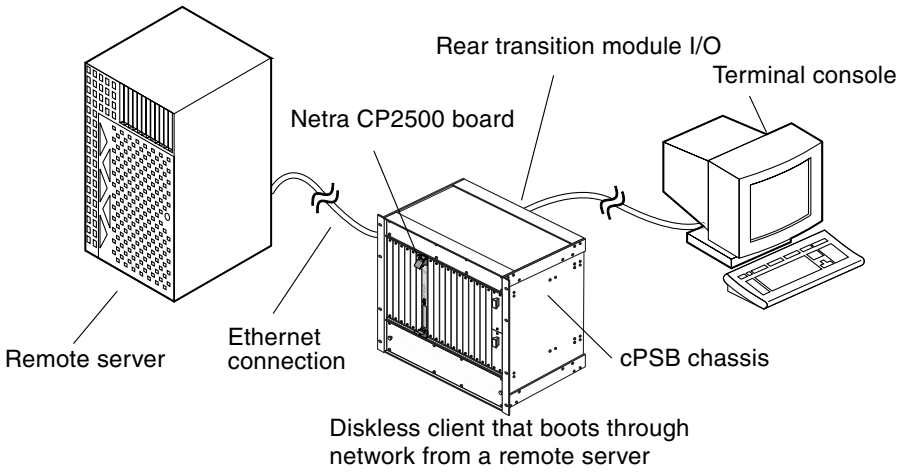

FIGURE 1-3 Netra CP2500 Board Diskless Client Configuration Example

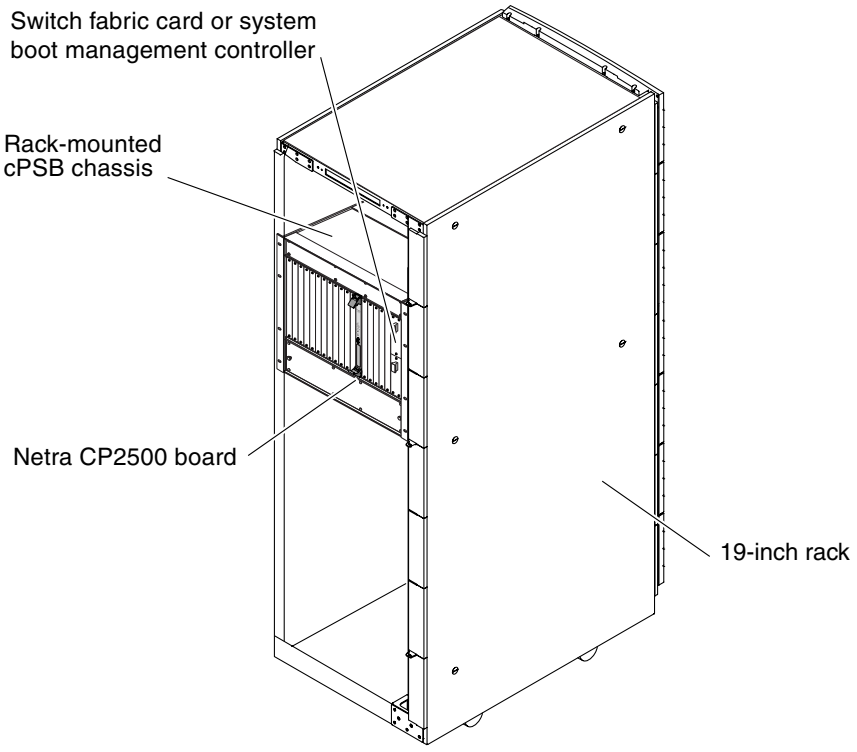

FIGURE 1-4 Netra CP2500 Node Board Mounting Configuration Example

1.2.1 PMC Modules

While the Netra CP2500 board has only one serial port on the front panel, IHV-built PMC modules can provide additional I/O to the front panel. PMC modules decode their custom I/O from the Netra board's on-board PCI bus signals.

Note – Sun does not support installing a PMC interface module (PIM) device on either the RTM-S or the RTM-H.

Note – The Netra CP2500 board has one PMC I/O slot. If you purchase a board with a PMC disk drive, you will not be able to install an additional PMC device.

1.2.2 Rear Transition Modules

There are two optional transition modules (RTMs) available for the Netra CP2500 board:

- Netra CP2500 RTM-H (FIGURE 1-5) – Designed to work exclusively in the host slot of the Netra CT 410 and 810 cPCI servers (see FIGURE 1-2)
- Netra CP2500 RTM-S (FIGURE 1-6) – Usable in either a satellite slot of a Netra CT 410 and 810 cPCI servers (see FIGURE 1-2) or in a node slot of a cPSB chassis (see FIGURE 1-7)

You can install the RTM-H and RTM-S into rear slots of the Netra CT server, opposite the appropriate Netra CP2500 board. These rear transition modules connect with the board's CompactPCI connectors through the Netra CT server midplane pins and carry four Ethernet ports, and two serial ports out to its rear panel. Refer to the *Netra CT Server Installation Guide* (819-2740) for installation and cabling instructions.

After setting a DIP switch on the Netra CP2500 board and two banks of DIP switches on the RTM-S, you can install the Netra CP2500 board and the RTM-S into a cPSB chassis (see FIGURE 1-7). See Chapter 2 for cPSB chassis installation instructions, including how to set these mechanical switches.

Note – For complete information about the two Netra CP2500 rear transition modules, refer to the *Netra CP2500 Rear Transition Module Installation and Technical Reference Manual* (819-1753).

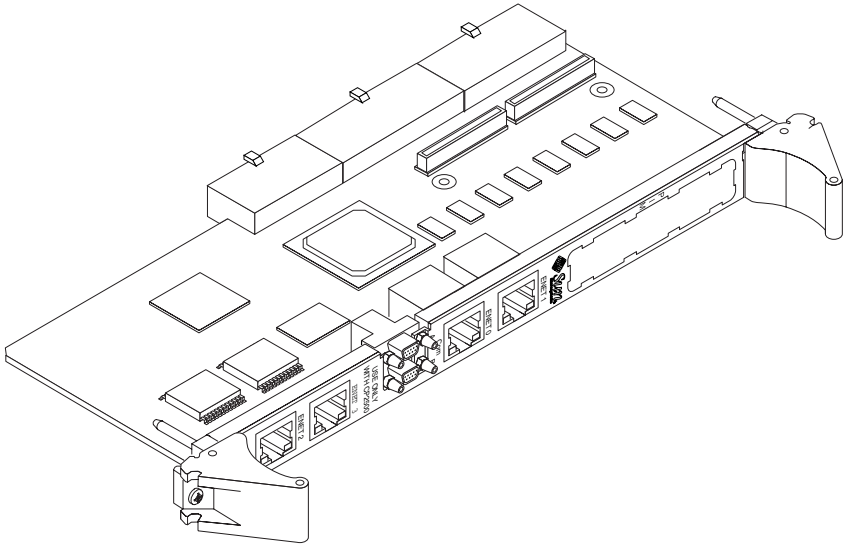

FIGURE 1-5 Netra CP2500 RTM-H for Netra CT Server Host Slots

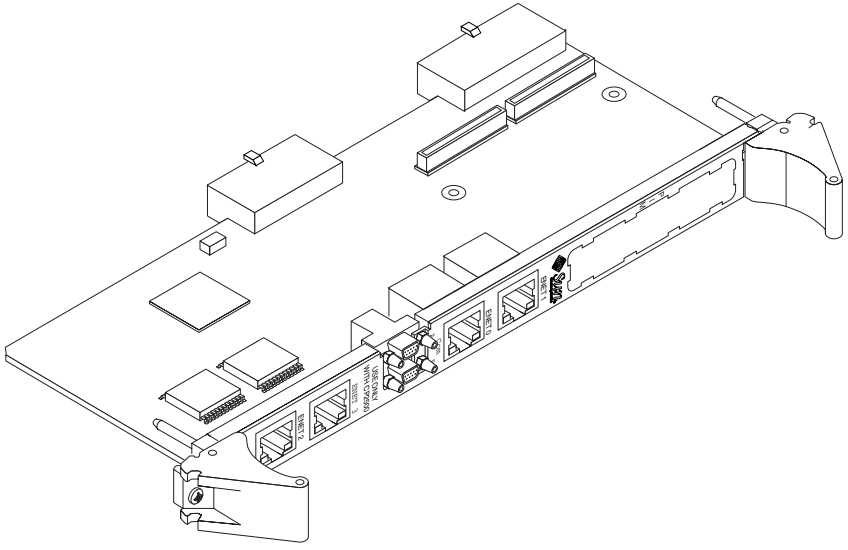

FIGURE 1-6 Netra CP2500 RTM-S for Netra CT Satellite Slots and cPSB Node Slots

FIGURE 1-7 shows the relationship between the Netra CP2500 board, the RTM-S, and the backplane in a typical cPSB chassis.

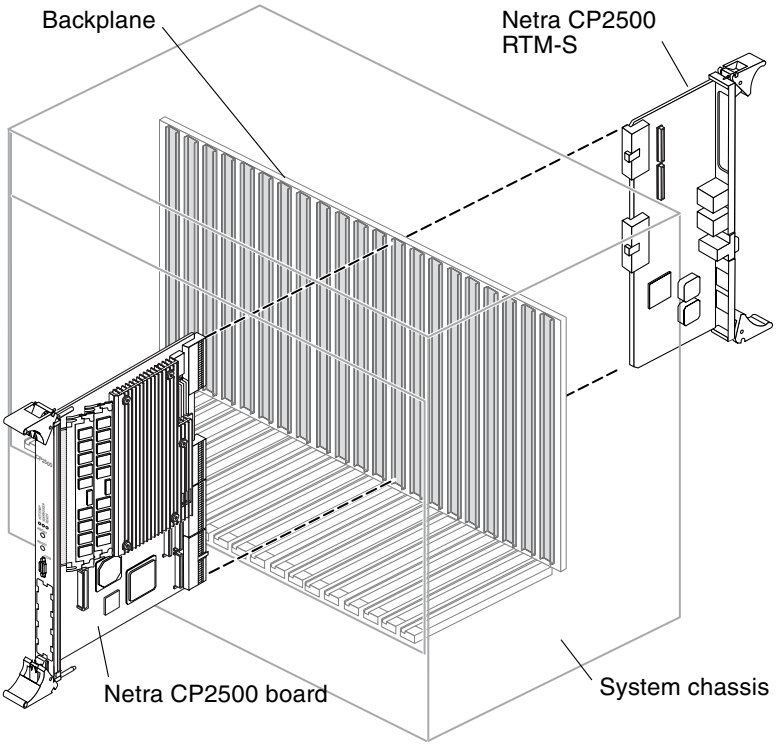

FIGURE 1-7 Netra CP2500 Board and a RTM-S in a Typical cPSB Chassis

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Note – To satisfy EMI compliance standards, you must use shielded cables for serial ports when using an RTM with the Netra CP2500 board. The shields for all shielded cables must be terminated on both ends. You can use unshielded cables on Ethernet ports.

The customer can order a Netra CP2500 RTM-S, build a custom card, or buy from an independent hardware vendor (IHV). A minimal set of I/O must provide for a boot path for the host board, and for a path for console I/O to deliver commands and to read board and system status.

TABLE 1-3 describes the possible Netra CP2500 board boot and I/O configurations. Sun Microsystems provide the Netra CP2500 boards and compatible RTMs. These RTMs provide four Ethernet RJ45 ports from the host to the rear of the system. These ports can optionally be used to accomplish a network boot as a diskless client. The other configurations require IHV hardware.

TABLE 1-3 Netra CP2500 Board I/O Configurations

Hardware Configuration	I/O Descriptions
Netra CP2500 board	Serial I/O – Serial port A on the front panel provides the path of the default console I/O.
Netra CP2500 board and RTM-H in a Netra CT server	Serial I/O – Serial port A can be accessed either from the front of the board or through the RTM-H serial port A, but not both through the front and rear ports at the same time. Serial port B is available through the RTM-H. SCSI – SCSI controller with SCSI I/O routed only to the Netra CT 410 or 810 internal drive bays. SCSI PIM I/O is not supported. Ethernet: Four RJ-45 ports on the RTM-H provide Ethernet network I/O
Netra CP2500 board and RTM-S in a Netra CT server	Serial I/O – Serial port A can be accessed either from the front of the board or through the RTM-S serial port A, but not through the front and rear ports at the same time. Serial port B is available through the RTM-S. Ethernet - Four RJ-45 ports on the RTM-S provide Ethernet network I/O.
Netra CP2500 board and RTM-S in a cPSB chassis	Serial I/O – Serial port A can be accessed either from the front of the board or through the RTM-S serial port A, but not through the front and rear ports at the same time. Serial port B is available through the RTM-S. Ethernet – Depends on how you set the mechanical switches on the RTM-S. • Switches set to cPSB-mode – Ethernet I/O routed to cPSB network in chassis, and *not* to the RTM-S RJ-45 ports. • Switches set to non-cPSB-mode – Ethernet I/O routed to the four RJ-45 ports on the RTM-S.
Optional third-party SCSI or IDE PMC interface card	A third-party PMC interface card can be installed to provide external SCSI, serial, or IDE I/O.

1.3 Hot-Swap Support

This section briefly discusses the hot-swap support on the Netra CP2500 board.

Refer to the PICMG *CompactPCI Hot-Swap Specification*, for a detailed description of this subject. In general, the hot-swap process includes the orderly connection of the hardware and software.

This process uses hardware connection control to connect the hardware in an orderly sequence. Hot-swapping uses backplane pins of different lengths to perform signal sequencing, which protects the hardware and avoids corrupting the backplane bus.

There are three models of hot-swap described in the PICMG *CompactPCI Hot-Swap Specification* – basic hot-swap, full hot-swap, and high-availability (HA) hot-swap.

TABLE 1-4 lists the hot-swap support details when a Netra CP2500 board is installed in a Netra CT 410 or 810 server, or when the board functions as a cPSB node board in a cPSB enclosure.

TABLE 1-4 Netra CP2500 Board Hot-Swap Support

Netra CP2500 Role	Basic Hot-Swap	Full Hot-Swap	HA Hot-Swap*
Netra CT 410 or 810 host board	Yes	Yes	Yes†
Netra CT 410 or 810 satellite board	Yes	Yes	Yes
cPSB node board	Yes	Yes	Yes

* When a board is full hot-swap capable, it implies that the board will also be fully hot-swappable in an HA system.

† When a board is full hot-swap capable, it implies that the board will also be fully hot-swappable in an HA system.

1.4 System Requirements

1.4.1 Hardware Requirements

You can order the following items from Sun:

- Netra CP2500 board with 2 Gbytes of memory
- Netra CP2500 CompactPCI satellite/cPSB blade rear transition module (RTM-S)

Note – The Netra CP2500 CompactPCI host rear transition module (RTM-H) cannot be ordered separately, but the RTM-H is included the Netra CT 410 and Netra CT 810 Netra CP2500 board upgrade kits.

Rear transition modules are optional and must be ordered separately from the Netra CP2500 board. Refer to the *Netra CP2500 Rear Transition Module Installation and Technical Reference Manual* (819-1753) for complete details about installing and using the Netra CP2500 RTMs.

Acquire the following components if needed:

- Serial terminal or terminal emulation for console output
- Cables for terminal and network connection

  Refer to the *Netra CP2500 Rear Transition Module Installation and Technical Reference Manual* (819-1753) for descriptions of the RTM I/O connections.
- PMC hardware for additional I/O

TABLE 1-5 lists additional hardware requirements.

TABLE 1-5 cPSB System and Other Minimum Requirements

Requirements	Netra CP2500 as Node Board
cPSB system enclosure for 6U boards (includes chassis, backplane, power supply*)	Yes
Console output device/serial terminal	Yes
Boot device (such as hard drive or network)	Yes
Peripheral device for network access	Yes
System management controller	Yes

* See Appendix A to ensure that your system enclosure meets the power supply and cooling requirement specifications.

Caution – You can damage the Netra CP2500 board components if you install the board in a chassis that does not provide sufficient cooling or has incorrect cPCI I/O voltage (VIO).

Note – If you will be updating the host or satellite CompactPCI boards in a Netra CT 410 or 810 server, refer to the *Netra CT Server Upgrade Guide* (819-2745) for the hardware requirements.

1.4.2 Software Requirements

Refer to the *Netra CP2500 Board Release Notes* (819-1748) for Solaris OS information, including a list of the required software patches and where to find installation instructions. You can view and download the latest version of this document at the following web site:

`http://www.sun.com/documentation/`

1.5 Physical Description

The Netra CP2500 board is a 6U circuit board with CompactPCI connectors J1 and J2 for PCI, and J3 and J5 for I/O. The CompactPCI J4 connector is not fitted to the board. See FIGURE 1-8 and FIGURE 1-9 for top and solder-side views of the board.

Note – The heat sink is not shown in this diagram to illustrate the components on the board that lie beneath the heat sink.

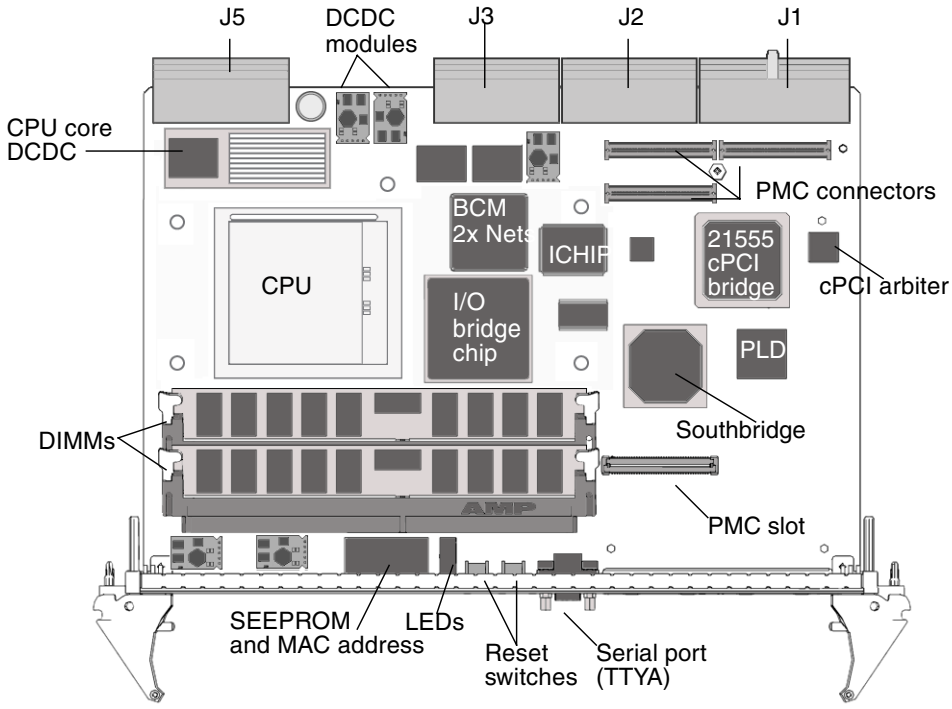

FIGURE 1-8 Netra CP2500 Board Layout

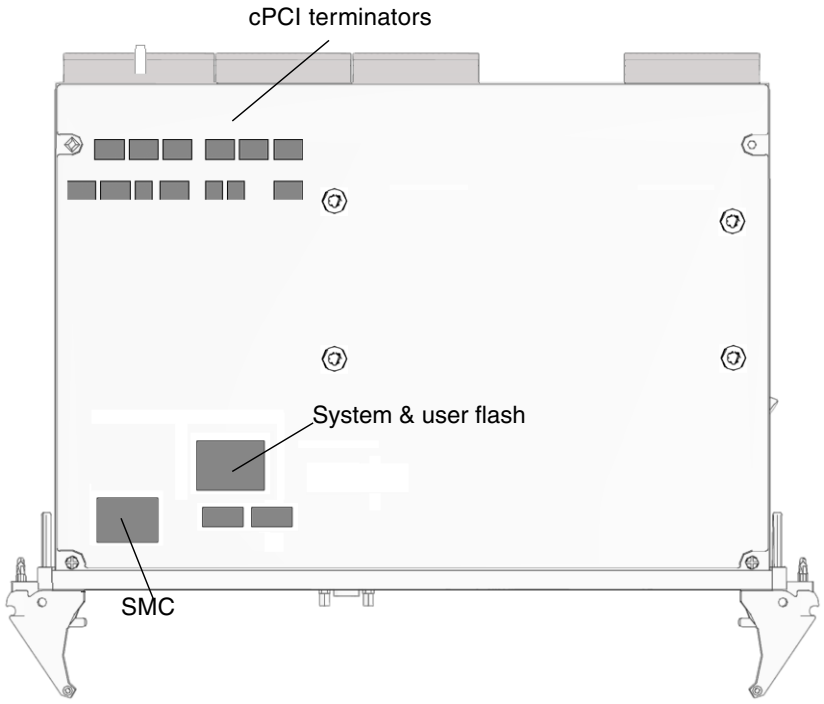

FIGURE 1-9 Typical Netra CP2500 Board – Solder Side

1.5.1 Front Panel Components

FIGURE 1-10 displays the locations of the Netra CP2500 board front panel LEDs, buttons, serial port, and PMC slot. TABLE 1-6 describes these front panel components.

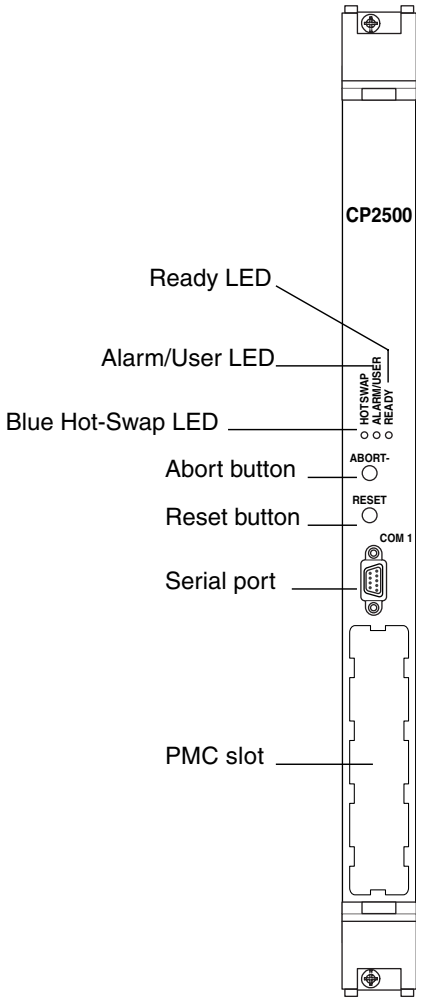

FIGURE 1-10 Netra CP2500 Board Front Panel

TABLE 1-6 Front Panel I/O

Front panel component	Description
Ready green LED	A green LED showing that the board is receiving power, which is sourced from the power module and controlled by the system management controller (SMC).
Alarm/User yellow LED	You can define the operation of this yellow LED. The default function of this LED shows that the board is at an OK status. The colors are CPU controlled by way of the SMC. Refer to the *Netra CP2500 Board Programming Guide* (819-1749) for information on programming the alarm/user LED.
Hot-swap blue LED	A blue LED that shows the hot-swap status of the board. See Section 3.1, "Hot-Swap Information" on page 3-2 for more information about hot-swap operations. **Note** - The hot-swap LED is in a noncompliant location of the front panel.
Abort button	An abort button, which passes an externally initiated reset (XIR) signal to the SMC when pressed.
Reset button	A reset button, which passes an power-on-reset (POR) signal to the SMC when pressed.
Serial port (COM1)	One micro DB9 connector is available for serial port (TTYA) I/O. This port can only be used if rear serial port COM A is not being used.
PMC slot	One peripheral mezzanine card (PMC) slot is available for additional I/O.

1.5.2 Functional Block Diagram

FIGURE 1-11 displays a simplified schematic diagram of the Netra CP2500 board.

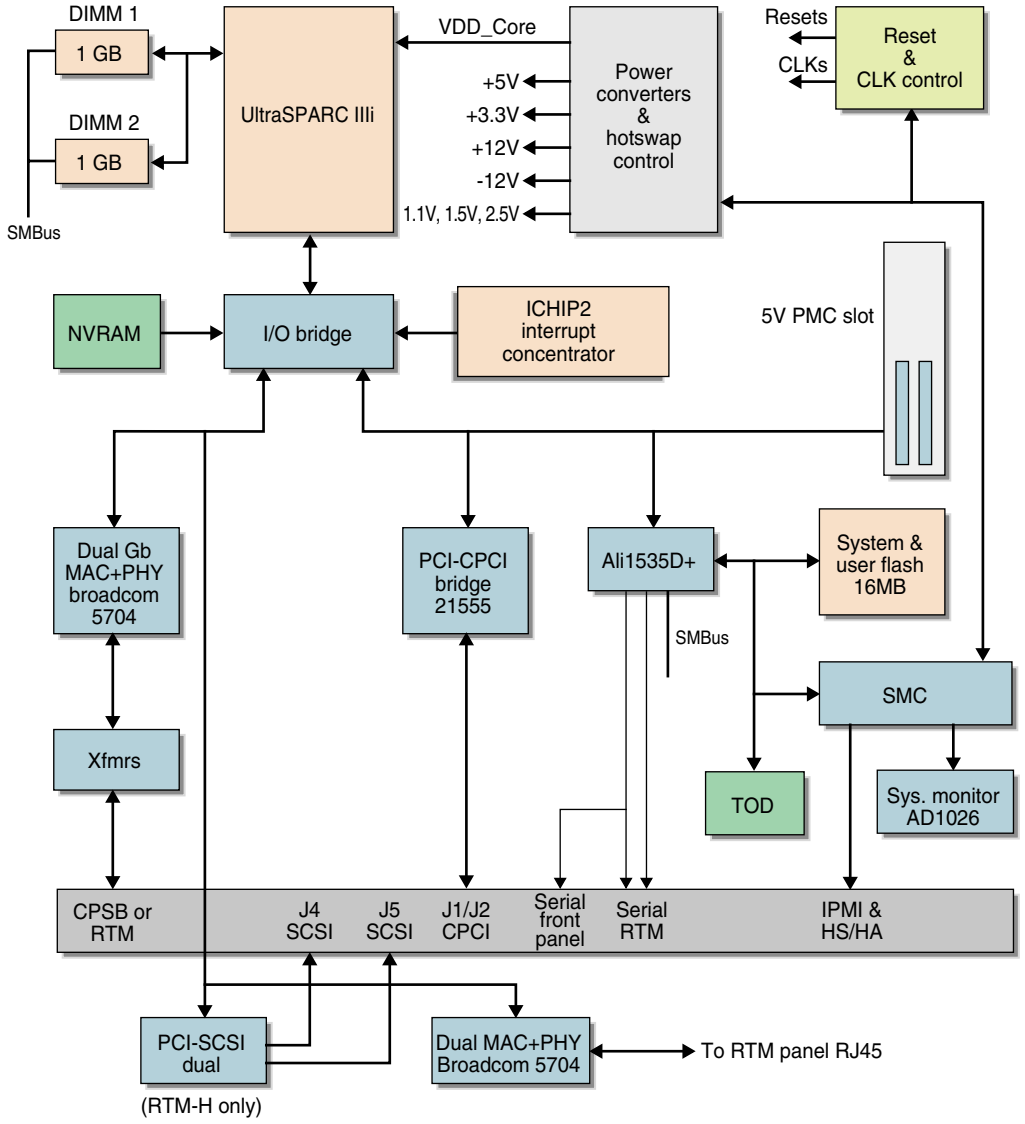

FIGURE 1-11 Netra CP2500 Board Functional Block Diagram

1.6 Contacting Technical Support

Should you have any technical questions or support issues that are not addressed in the Netra CP2500 documentation set or on the web site, contact your local Sun Services representative. Find the World Wide Solution Center nearest you by visiting our web site:

`http://www.sun.com/service/contacting/solution.html`

When you call Sun Services, be sure to indicate if the Netra CP2500 board was purchased separately and is not associated with a system. Please have your Sun support contract number and the board identification information ready when you call. For proper identification of the board be prepared to give the representative the board part number, serial number, and board revision level (see FIGURE 1-12).

1.6.1 Board Identification

The Netra CP2500 board can be identified by the barcode labels placed on the board (see FIGURE 1-12). You will need to locate the following labels to identify the board properly:

- Serial number barcode label – provides the board's serial number (for example, 1005LCB-0532JM000V).
- Assembly label – contains the board's part number, the revision number (for example, Rev. 04), and the country where the board was assembled.
- MAC address label – displays the MAC address for the board in printed and barcode form. See Section 2.5.3, "Replacing the SEEPROM" on page 2-13 for information on replacing the SEEPROM.

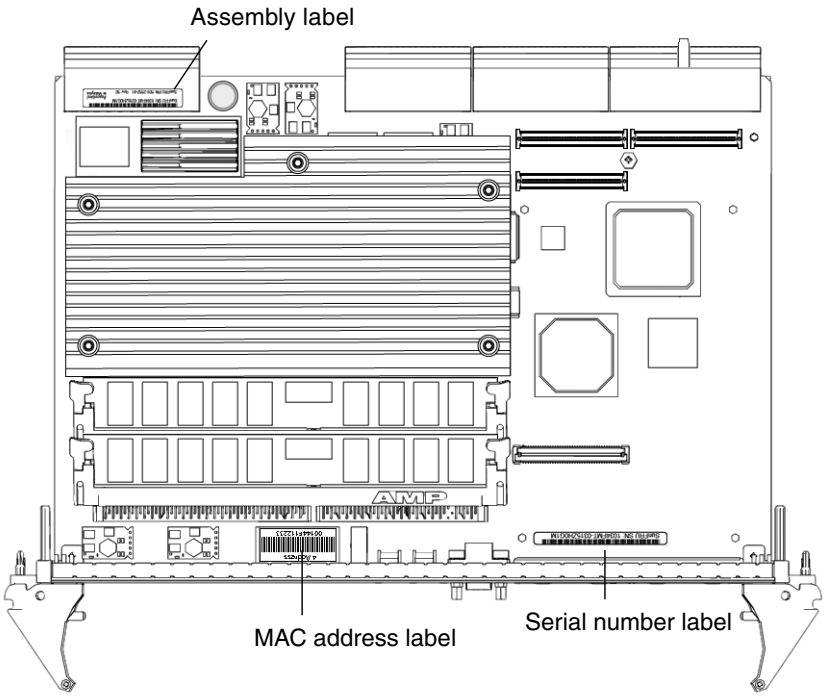

FIGURE 1-12 Typical Netra CP2500 Board Barcode Labeling

Note – You might find the labels shown in FIGURE 1-12 on other locations on your board. Also, your board configuration might appear different than shown in the preceding illustration.

CHAPTER 2

Installing the Netra CP2500 Board in a cPSB Chassis

This chapter describes how to install a Netra CP2500 board hardware in a cPSB chassis.

Note – This chapter does *not* describe how to install the board in a Netra CT 410 or 810 server, or how to replace a Netra CP2300 cPSB board installed in a cPSB chassis. See Section 2.1, "Installation Options" on page 2-2 for more information.

This chapter contains the following sections:

2.1 Installation Options

This chapter describes how to install the Netra CP2500 board in a cPSB chassis. TABLE 2-1 lists other installation options and where you can find the installation procedures.

TABLE 2-1 Hardware Installation Options

Installation Option	Installation Procedure Location
Upgrading the host or satellite board in a Netra CT 410 or 810 server	Refer to the *Netra CT Server Upgrade Guide* (819-2745) for the upgrade procedures.
Installing a new satellite board in a Netra CT 410 or 810 server	Refer to the *Netra CT Server Installation Guide* (819-2740) for these procedures.
Replacing a defective board in a Netra CT 410 or 810 server	Refer to the *Netra CT Server System Administration Guide* (819-2741) for these removal and installation procedures.
Installing the board in the Netra CT 820 cPSB server	The Netra CP2500 board is not supported in the Netra CT 820 server.
Installing the board in a third-party cPSB chassis	This chapter describes how to install the board in a third-party cPSB chassis.

You can download PDF and HTML versions of Sun documentation at the following web site:

`http://www.sun.com/documentation/`

Note – While the Netra CP2500 board can operate as a CompactPCI host or satellite CPU board in the Netra CT 410 and 810 servers, the board is *not* supported in third-party CompactPCI systems or chassis.

2.2 Equipment and Operator Safety

Refer to the *Important Safety Information for Sun Hardware Systems* (816-7190) for general safety information.

Read these safety statements specific to the Netra CP2500 board carefully before you install or remove any part of the system.

Caution – Depending on the particular chassis design, operations with open equipment enclosures can expose the installer to hazardous voltages with a consequent danger of electric shock. Ensure that line power to the equipment is disconnected during operations that make high voltage conductors accessible.

The installer must be familiar with commonly-accepted procedures for integrating electronic systems and with the general practice of Sun systems integration and administration. Although parts of these systems are designed for hot-swap operation, other components must not be subjected to such stresses. Work with power connected to a chassis only when necessary and follow these installation procedures to avoid equipment damage.

This equipment is sensitive to damage from electrostatic discharge (ESD) from clothing and other materials. Use the following antistatic measures during an installation:

- If possible, disconnect line power from the equipment chassis when servicing a system or installing a hardware upgrade. If the chassis cannot be placed upon a grounded antistatic mat, connect a grounding strap between the facility electrical input ground (usually connected to the equipment chassis) and facility electrical service ground.
- Use an antistatic wrist strap when:
  - Removing a board from its antistatic bag
  - Connecting or disconnecting boards or peripherals

  Connect the other end of the strap lead to one of the following:

  - A ground mat
  - Grounded chassis metalwork
  - A facility electrical service ground
- Keep boards in the antistatic bags until they are needed.
- Place circuit boards that are out of their antistatic bags on an antistatic mat if one is available. The mat must be grounded to a facility electrical service ground. Do not place boards on top of an antistatic bag unless the outside of the bag also has antistatic protective properties.
- Remove a board from its antistatic bag only when wearing a properly connected ground strap.

2.3 Materials and Tools Required

This section provides information on the materials and tools required to perform installation. The minimum tools required to perform installation are:

- Straight blade screwdriver, 1/4 inch
- Phillips screwdrivers, No. 1, No. 2
- Antistatic wrist strap
- Needle nose pliers
- Needle, metal pick, scribe tool, or small screwdriver to set the DIP switches
- Terminal

Refer to Section 1.4.1, “Hardware Requirements” on page 1-13 for information on hardware requirements.

2.4 Preparing for the Installation

Read the following subsections before starting to install these boards. In addition, do the following:

1. Become familiar with the contents of the referenced documentation.
2. Verify that all listed hardware and software is available (see Section 1.4, “System Requirements” on page 1-13).
3. Check power, thermal, environmental, and space requirements (see Section 2.4.1, “Checking Power, Thermal, Environmental, and Space Requirements” on page 2-5).
4. Verify that local area networking (LAN) preparations are completed (see Section 2.4.2, “Determining Local Network IP Addresses and Hostnames” on page 2-5).
5. Ensure that the host names and their network IP addresses are allocated and registered at the site.

2.4.1 Checking Power, Thermal, Environmental, and Space Requirements

Ensure that:

- Your enclosure specifications support the sum of the specified maximum board power loads. See Section A.4, "Power Requirements" on page A-3 for board power specifications.
- Facility power loading specifications can support the rack or enclosure requirements.
- Your enclosure specifications support the cooling airflow requirements. See Section A.6, "Environmental Specifications" on page A-6.
- The Netra CP2500 board fits a standard CompactPCI packet switched backplane (cPSB) chassis. If your installation requirements are different, contact your field application engineer.

2.4.2 Determining Local Network IP Addresses and Hostnames

Collect the following information to connect hosts to the local area network (LAN). Ask your network administrator for help, if necessary. This information is not needed for a standalone installation. You can use TABLE 2-2 to record this information.

TABLE 2-2 Your Local Network Information

Information Needed	Your Information
IP addresses* and hostname for each Netra CP2500 client	
Domain name	
Type of name service and corresponding name server names and IP addresses – for example, DNS and NIS (or NIS+)	
Subnet mask	
Gateway router IP address	
NFS server names and IP addresses	
Web server URL	

* Local IP addresses are not needed if they are assigned by a network DHCP server.

You might need the MAC addresses of the local hosts to make nameserver database entries. The MAC address can be seen in the console output while booting to the `ok` prompt. It can also be derived from the host ID seen on the barcode label of the SEEPROM (see Section 1.6.1, "Board Identification" on page 1-20).

2.4.3 Installation Procedure Summary

Note – This chapter does *not* describe how to install the board in a Netra CT 410 or 810 server, or how to replace a Netra CP2500 cPSB board installed in a cPSB chassis. See Section 2.1, "Installation Options" on page 2-2 for more information.

This section summarizes the Netra CP2500 board installation at a high level. Ensure that you read the details in Section 2.5, "Configuring the Board Hardware" on page 2-7 through Chapter 3 before installing the board.

The process to set up and configure a Netra CP2500 board in a cPSB chassis includes the following steps:

1. Configure the board's physical hardware.

   For example, install the PMC card, replace the SEEPROM (if required), and set DIP switches if necessary.

2. If your environment requires rear access to connect cables, configure and install the RTM-S module.

   a. Configure the RTM-S module.

      For example, set DIP switch settings or prepare connector attachments, as necessary.

   b. Physically install the RTM-S.

3. Physically install the Netra CP2500 board, and any peripheral boards, into the chassis.

4. Connect the node(s) to a local network. Alternatively, the board can be run as a standalone system without a network connection.

5. Install the Solaris Operating System.

2.5 Configuring the Board Hardware

This section lists hardware installation and settings that might apply for your board configuration. Read and perform the procedures, as necessary, before installing the Netra CP2500 board into a cPSB chassis.

2.5.1 Installing an Optional PMC Device

A PCI mezzanine card (PMC) is a slim, modular mezzanine card that provides additional functionality to the Netra CP2500 board. The board contains one PMC slot in which you can install an optional PMC device (see FIGURE 2-1 for the location of the slot). You must install PMC devices on the Netra CP2500 board before you install the board into the chassis.

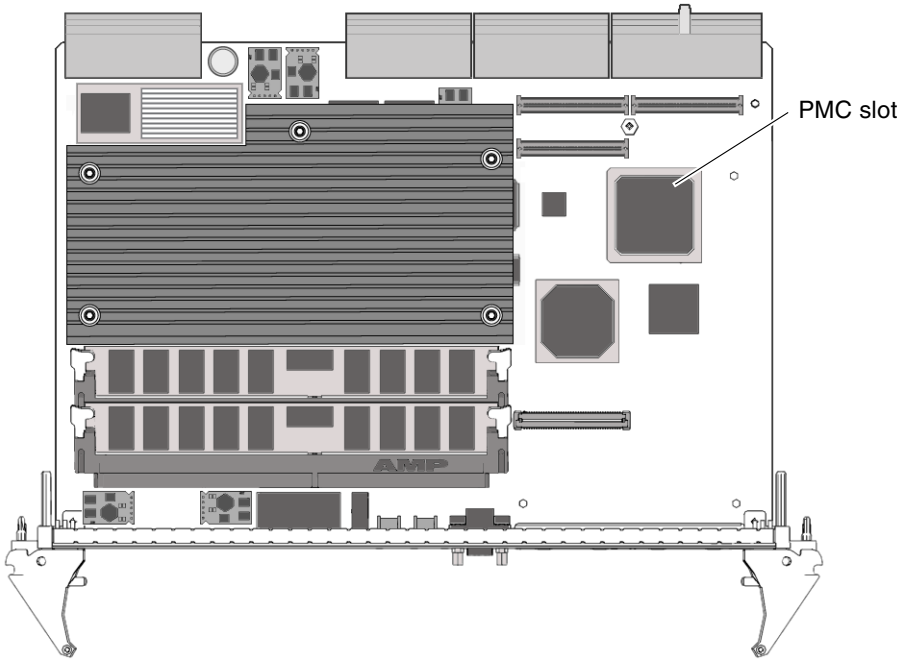

FIGURE 2-1 PMC Slot Location

Note – Before installing the PMC device, ensure that the device is keyed to 5V, or is set to universal voltage.

Note – The following procedure provides a generic set of instructions for installing PMC devices on the Netra CP2500 board. Refer to the PMC card manufacturer's documentation for specific instructions on installing these devices.

1. **Retrieve the wrist strap from the adapter's shipping kit.**
2. **Attach the antistatic wrist strap:**
   a. **Attach the adhesive copper strip of the wrist strap to the metal chassis.**
   b. **Wrap the other end twice around your wrist, with the adhesive side against your skin.**
3. **Remove the Netra CP2500 board from its antistatic envelope and place it on an ESD mat (if one is available) near the chassis.**

   If an ESD mat is not available, you can place the card on the antistatic envelope it was packaged in.

Note – If EMI compliance is required, do not remove the PMC filler panel unless you are going to install a PMC on the board.

4. **If the PMC has a connector for cabling, or if the PMC has a faceplate that fits in the Netra CP2500 board's faceplate, remove the board's filler panel (**FIGURE 2-2**).**

   Depending on its application, a PMC might contain a connector where you need to attach a PMC-specific cable, or it might have LEDs that must be viewed while the operating. If the PMC has a connector, LEDs, or a protruding faceplate, remove the board's filler panel.

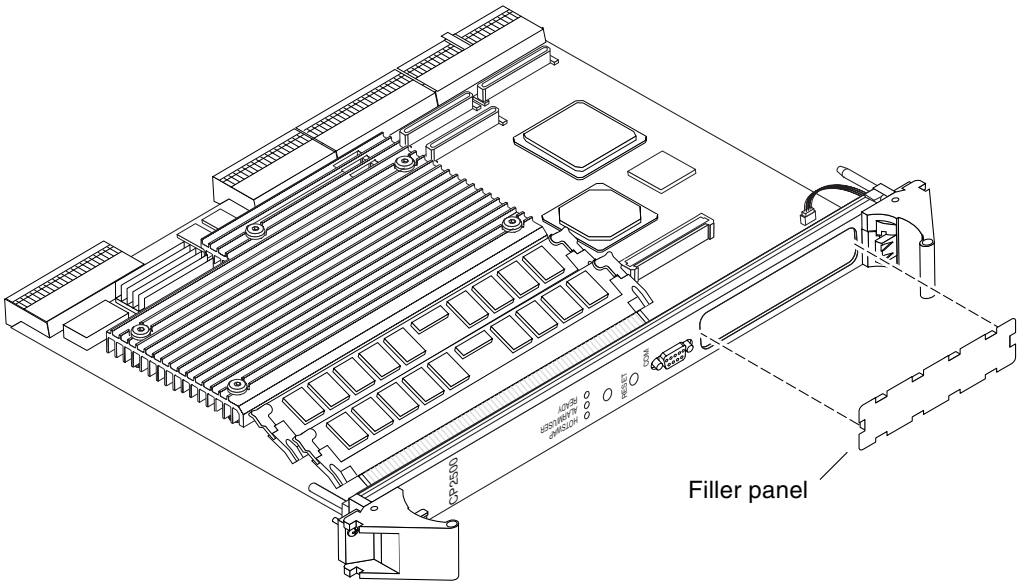

FIGURE 2-2 Removing the PMC Filler Panel

5. **Retrieve the PMC from its shipping kit and place it on an antistatic surface.**
6. **Insert the PMC at an angle into the appropriate PMC slot (**FIGURE 2-3**).**
   Ensure that the PMC's connector goes through the board's PMC slot.

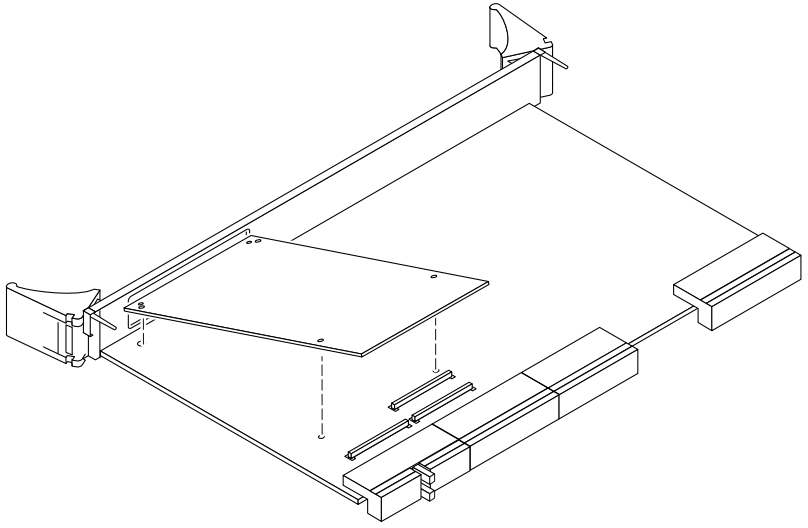

FIGURE 2-3 Inserting the PMC Into the PMC Slot

7. **Align the PMC over the PMC connectors.**

8. **Carefully press the PMC into the board's PMC connectors (**FIGURE 2-4**).**

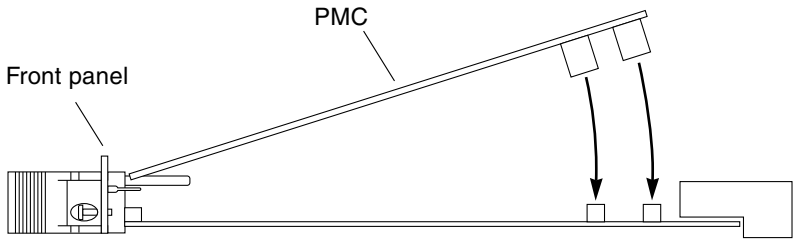

FIGURE 2-4 Pressing the PMC Into the PMC Connectors – Side View

Caution – Do not use excessive force when installing the PMC into the slot. You might damage the PMC's connectors or the connectors on the Netra CP2500 board, causing permanent damage to the PMC or the board. If the PMC does not seat properly when you apply even pressure, remove the PMC and carefully reinstall it.

9. **Turn the Netra CP2500 board over and use a No. 1 screwdriver to secure the four screws that attach the PMC to the Netra CP2500 board (**FIGURE 2-5**).**

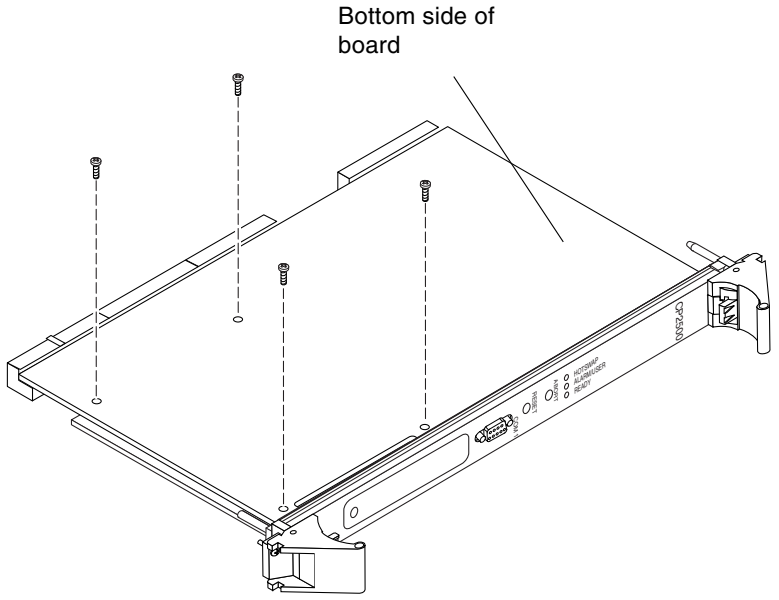

FIGURE 2-5 Securing the PMC Screws

Refer to the PMC device's documentation for PMC software and cabling installation instructions.

2.5.2 Setting the SW3301 DIP Switch

Switch 2 of the SW3301 DIP switch bank selects whether the board will operate in a Netra CT 410 or 810 CompactPCI server or in a cPSB chassis. By default, this switch is set so that the board will operate in a Netra CT 410 or 810 server. Prior to installing the Netra CP2500 board into a cPSB chassis, you must change the setting of this switch so that the board will operate in a cPSB chassis.

Note – See Section B.4, "DIP Switch Settings" on page B-18, for further details about the Netra CP2500 board switch settings.

To Set SW3301 Switch 2 to cPSB operation:

1. **Retrieve the wrist strap from the adapter's shipping kit.**
2. **Attach the antistatic wrist strap:**
   a. **Attach the adhesive copper strip of the wrist strap to the metal chassis.**
   b. **Wrap the other end twice around your wrist, with the adhesive side against your skin.**
3. **Remove the Netra CP2500 board from its antistatic envelope and place it on an ESD mat (if one is available) near the chassis.**

   If an ESD mat is not available, you can place the card on the antistatic envelope it was packaged in.
4. **Using a needle, metal pick, scribe tool, or a small screwdriver, set switch 2 from the open position (in the direction opposite of the arrow on the switch) to closed (in the direction of the arrow).**

   The SW3301 DIP switch bank is located on the component side of the board between the front panel and heat sink (see FIGURE 2-6). FIGURE 2-6 displays how to set switch 2 from the open to closed position.

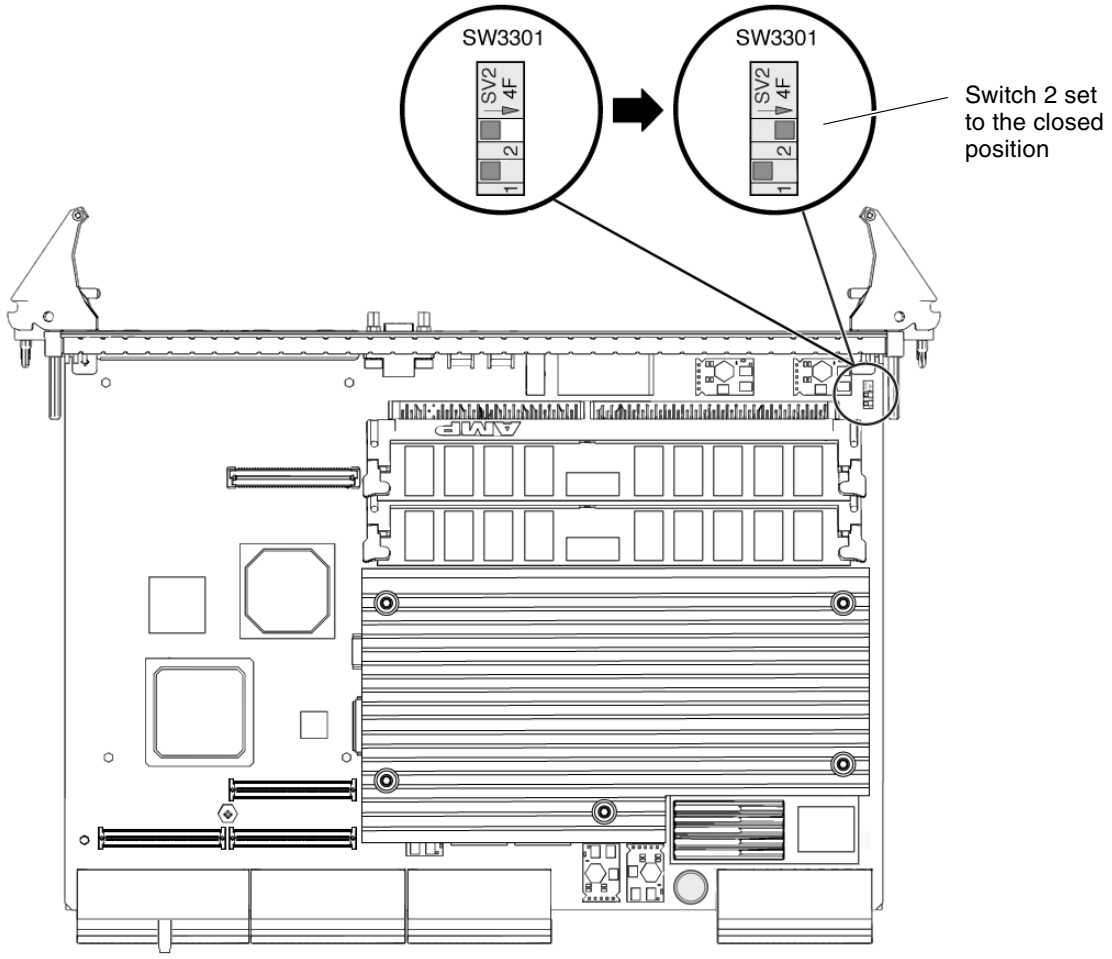

FIGURE 2-6 Setting the SW3301 Switch 2 to cPSB Chassis Operation

2.5.3 Replacing the SEEPROM

The SEEPROM stores the board MAC address and host ID information. You do not need to replace the SEEPROM unless you are installing a replacement board that does not have the correct host ID information.

If you need to replace the Netra CP2500 board, remove the SEEPROM from the original board and install it on the replacement Netra CP2500 board.

To Replace the SEEPROM:

1. **Retrieve the wrist strap from the adapter's shipping kit.**
2. **Attach the antistatic wrist strap:**
   a. **Attach the adhesive copper strip of the wrist strap to the metal chassis.**
   b. **Wrap the other end twice around your wrist, with the adhesive side against your skin.**
3. **Remove the Netra CP2500 board from its antistatic envelope and place it on an ESD mat (if one is available) near the chassis.**

   If an ESD mat is not available, you can place the card on the antistatic envelope it was packaged in.
4. **Locate the MAC address label on the board.**

   The MAC address label is located between the board's faceplate and the memory connectors (see FIGURE 2-7). The MAC address label is fastened on a plastic carrier that protects the SEEPROM.
5. **Carefully lift the plastic SEEPROM carrier off of the board (see FIGURE 2-7).**

   Removing the plastic contain will also remove the board's SEEPROM.

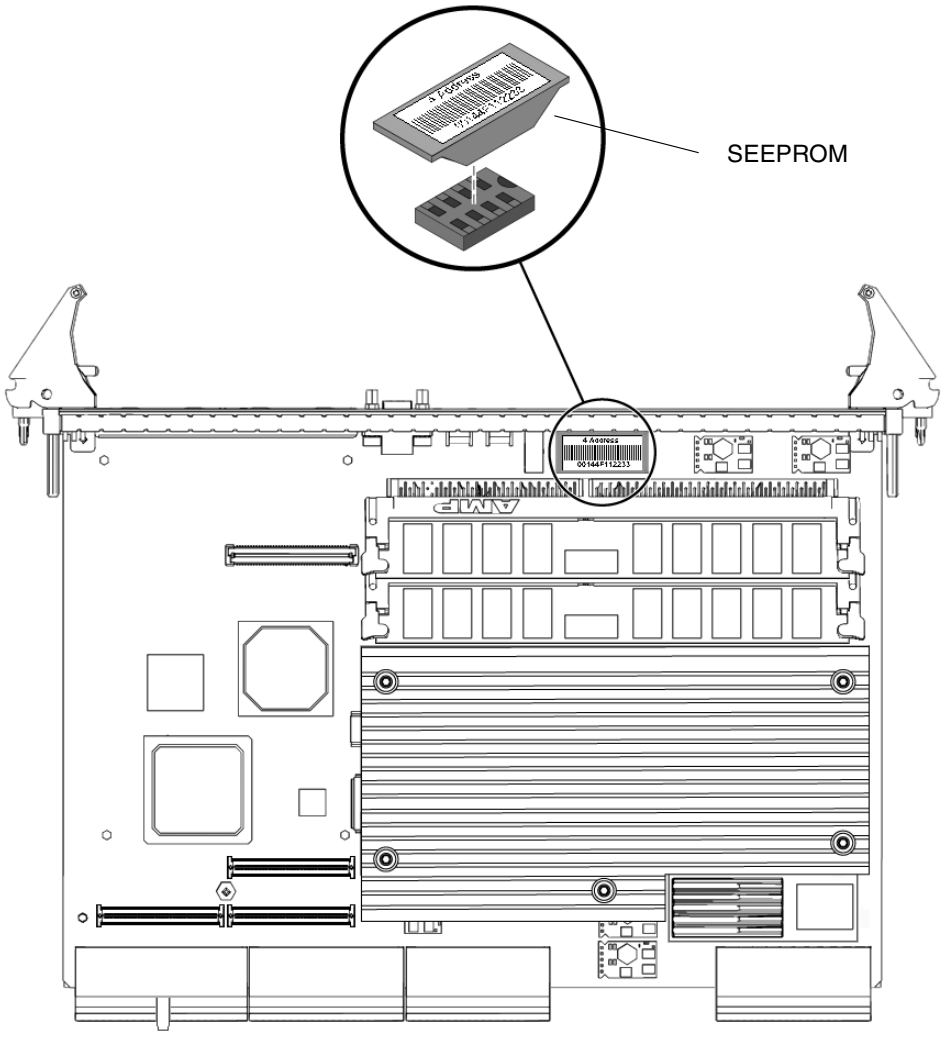

FIGURE 2-7 Replacing the SEEPROM

6. **Locate the SEEPROM that you removed from the original, defective board you returned to Sun Services.**

   The SEEPROM should still be encased in its protective plastic carrier with its MAC address label attached.

7. **Carefully press the SEEPROM carrier on the board.**

2.5.4 Preparing the RTM-S for Installation

If you are using the Netra CP2500 RTM-S, refer to the *Netra CP2500 Rear Transition Module Installation and Technical Reference Manual* (819-1753). You might also want to refer to this RTM manual for detailed connector pin assignments.

Note – An RTM is not required to operate Netra CP2500 board. However, an RTM is needed if you will be connecting cables to the rear of the system or chassis.

2.5.4.1 Differences Between Available Netra CP2500 Rear Transition Modules

Two rear transition modules are available from Sun for the Netra CP2500 board – the RTM-H and the RTM-S. The RTM-H is designed to be operated solely in the host CompactPCI slot of the Netra CT 410 and 810 servers. The RTM-H will not operate in a cPSB chassis, and it is not supported in any other CompactPCI server.

The RTM-S card can operate in either a Netra CT 410 or 810 server satellite slot or in a node slot of cPSB chassis. When installing a Netra CP2500 board into a cPSB chassis, you must use either this RTM-S or a custom-designed RTM.

2.5.4.2 Setting RTM-S DIP Switches

The Netra CP2500 RTM-S contains two DIP switch banks that must be set prior to installing the card into the cPSB chassis. These switch banks control whether the Ethernet network traffic of the board is routed to the RJ45 connectors on the RTM-S or whether the RTM-S runs in cPSB mode and the Ethernet network traffic is routed to the cPSB backplane. By default, these switch banks are set to route the traffic to the RJ45 connectors. Therefore, before installing the RTM-S into a cPSB chassis, set these switches to cPSB network operation.

Note – For additional information about these DIP switch settings, refer to the *Netra CP2500 Rear Transition Module Installation And technical Reference Manual* (819-1753).

To set the RTM-S DIP switches to cPSB network operation:

1. **Retrieve the wrist strap from the adapter's shipping kit.**

2. **Attach the antistatic wrist strap:**

   a. **Attach the adhesive copper strip of the wrist strap to the metal chassis.**

   b. **Wrap the other end twice around your wrist, with the adhesive side against your skin.**

3. **Remove the Netra CP2500 RTM-S from its antistatic envelope and place it on an ESD mat (if one is available) near the chassis.**

   If an ESD mat is not available, you can place the card on the antistatic envelope it was packaged in.

4. **Locate the S1301 DIP switch bank on the component side of the RTM-S (see** FIGURE 2-8**).**

   By default, all of the switches in the S1301 bank will be set to On.

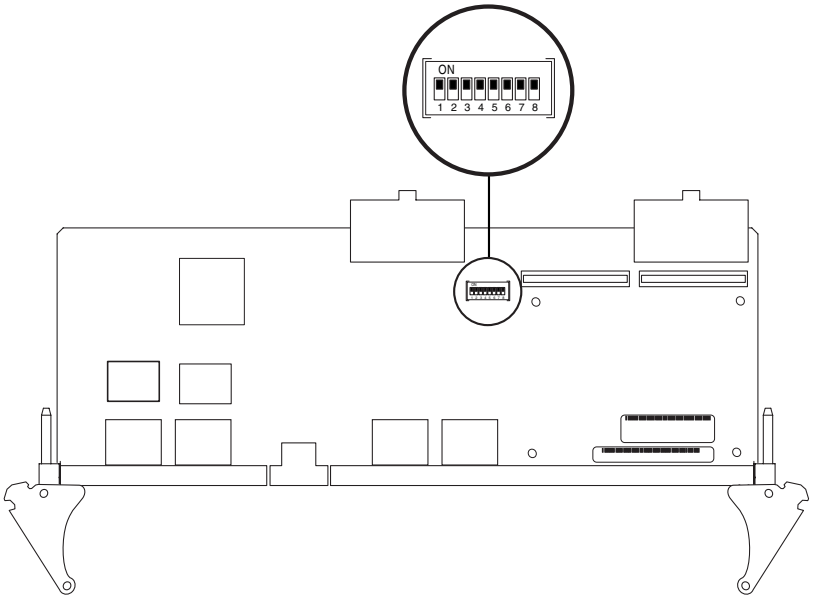

FIGURE 2-8 S1301 DIP Switch Bank Location on the RTM-S

5. **Using a needle, metal pick, scribe tool, or a small screwdriver, set all eight S1301 DIP switches to the Off position (see** FIGURE 2-9**).**

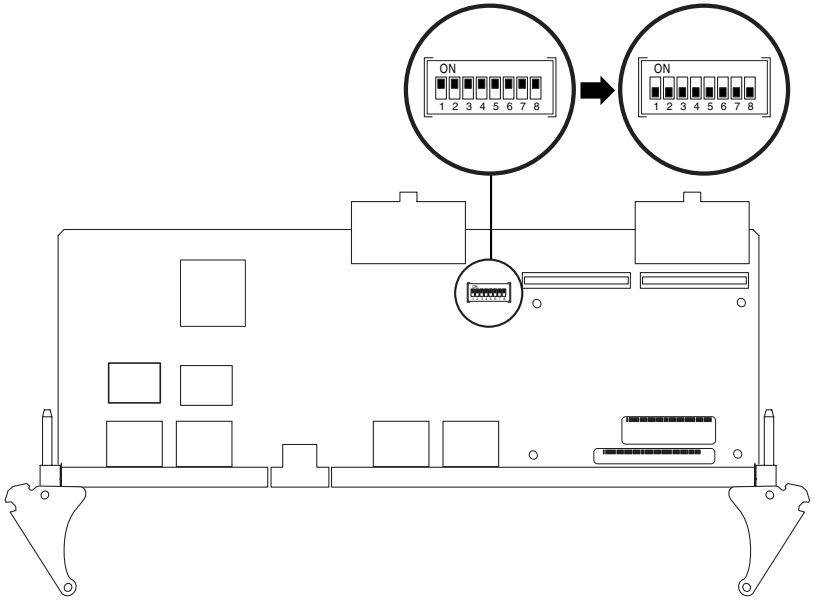

FIGURE 2-9 Setting the S1301 DIP Switches for cPSB Networks

6. **Carefully flip the RTM-S over to show its solder side and locate the S1302 DIP switch bank (see** FIGURE 2-10**).**

   By default, all of the switches in the S1302 bank will be set to On.

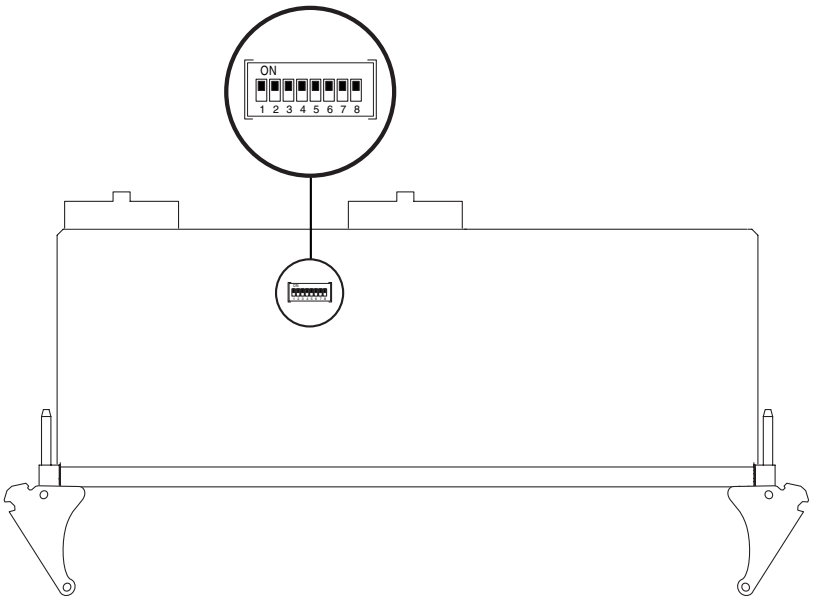

FIGURE 2-10 S1302 DIP Switch Bank Location on the Solder Side of the RTM-S

7. **Using a needle, metal pick, scribe tool, or a small screwdriver, set all eight S1302 DIP switches to the Off position (see** FIGURE 2-11**).**

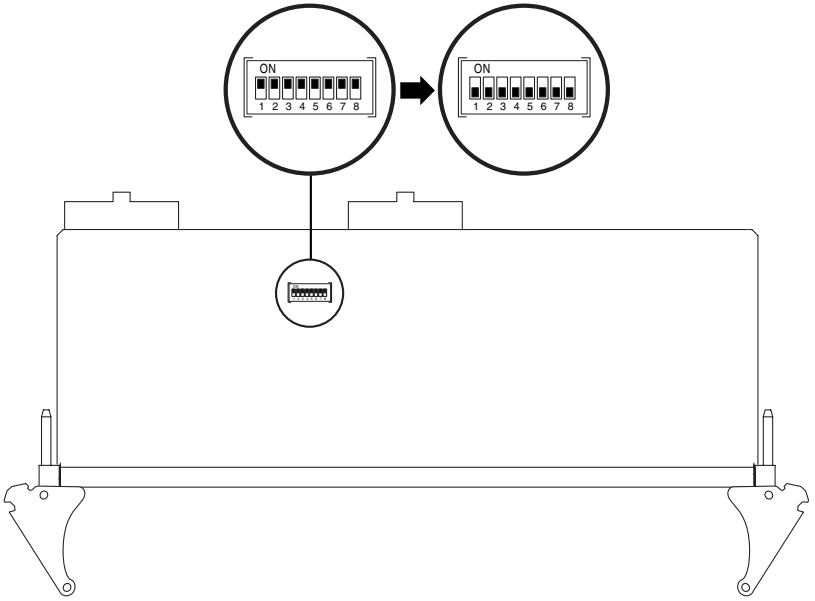

FIGURE 2-11 Setting the S1302 DIP Switches for cPSB Networks

2.6 Installing Boards Into a cPSB Chassis

This section describes the installation of the RTM-S and the Netra CP2500 board into an example cPSB system chassis. Refer to your cPSB chassis documentation for specific node board installation procedures.

2.6.1 Installing the RTM-S

If you will connect cables to the rear of the cPSB chassis, use a compatible RTM with the Netra CP2500 board. The Netra CP2500 RTM-S module provides rear I/O access and enables access to the network, to a boot device, and to a console terminal. You may use the Netra CP2500 RTM-S, or you may design your own RTM.

Refer to the installation procedure in the *Netra CP2500 Rear Transition Module Installation and Technical Reference Manual* (819-1753) to install the Netra CP2500 RTM-S.

Note – If the system power is on when installing the Netra CP2500 RTM-S, the RTM-S *must* be installed before you install the Netra CP2500 board.

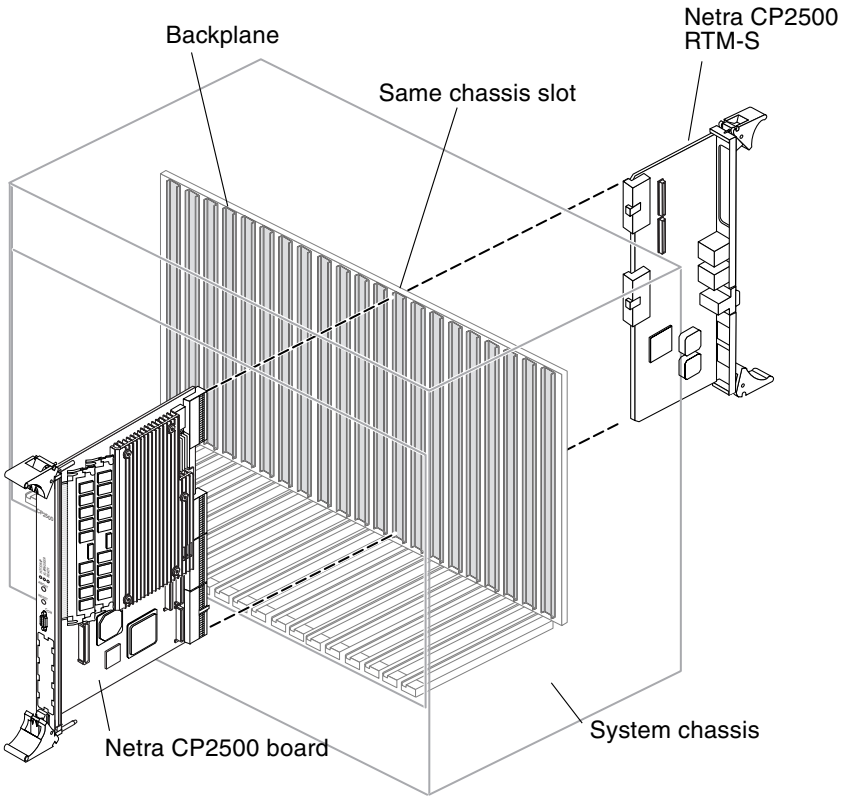

FIGURE 2-12 Installing the Netra CP2500 Board and RTM-S in an cPSB Chassis

2.6.2 Installing the Netra CP2500 Board

A cPSB chassis usually contains:

- A system slot. This slot is indicated by a triangle symbol on the backplane, if the chassis meets the PICMG 2.0 CompactPCI specification.
- One or two fabric card slots, which are labeled with a fabric card slot symbol (⋉).
- cPSB node slots (for a single-segment chassis). Node slots are identified by a circle symbol on the backplane.

1. **Ensure that power is disconnected from the chassis.**

   The Netra CP2500 board can be installed while the chassis is powered, however *only start with a powered chassis if necessary.* Check that the corresponding Netra CP2500 RTM is installed.

Note – If you need an RTM for I/O for the Netra board, ensure that it is already present in the chassis. This step is essential if the chassis is powered during the installation.

---

2. **Slide the Netra CP2500 board into the appropriate slot on the corresponding top and bottom mounting rails, and toward the backplane while gently pushing the board levers inward.**

   While sliding the board, ensure that the Netra CP2500 ejector levers are aligned perpendicular to the card flange in the unlocked position and that the board connectors are aligned with the RTM connectors (FIGURE 2-13).

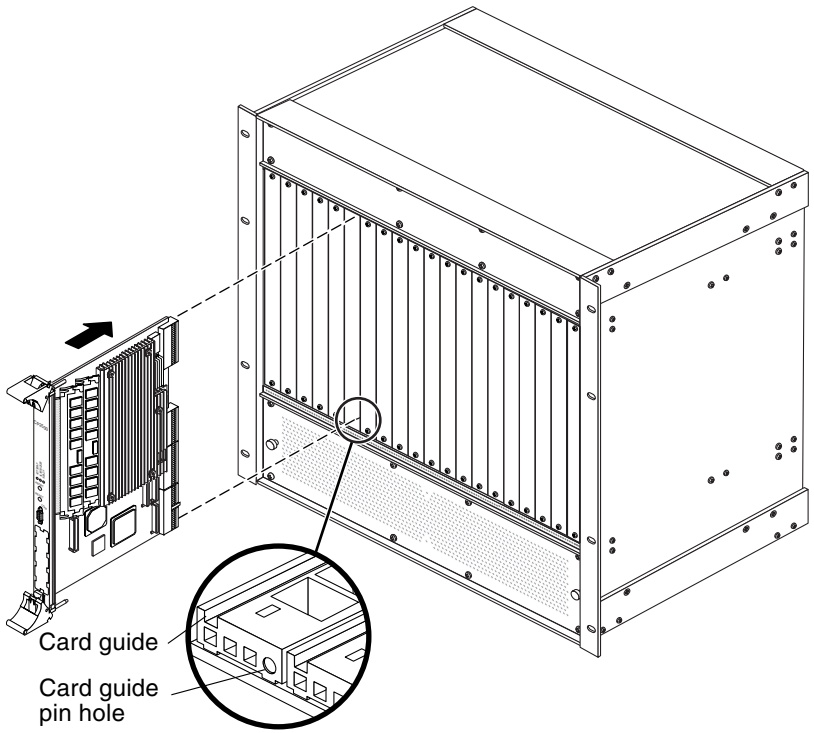

FIGURE 2-13 Installing a Netra CP2500 Board Into a cPSB Chassis Slot

3. **Install two screws through the top and bottom of the front connector plate to secure the board (see FIGURE 2-14).**

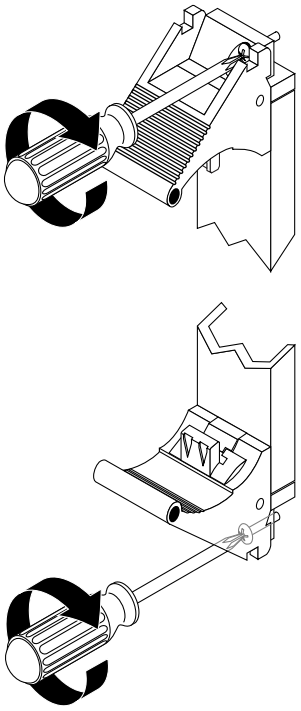

FIGURE 2-14 Securing the Board in the Chassis Slot

Note – Follow the chassis manufacturer's instructions to make sure the Netra CP2500 board is properly installed into the chassis slot.

2.7 Setting Up an Assembled Netra CP2500 Board

This section describes how to set up a system that contains the Netra CP2500 board.

1. **Using a category 5 grade network cable, connect one RJ45 connector into the receptacle of a chassis Ethernet fabric card or in the receptacle of the Netra CP2500 board's RTM.**

   The other end must be connected to a suitable Ethernet hub on the local subnet.

Note – Use shielded cables for Ethernet ports on the RTM. Ensure that the shield is grounded at both ends.

2. **Connect I/O cabling to the host board and to the serial port of the host system.**
3. **Connect a serial cable to the TTYA port on the front panel of the Netra CP2500 board or the Netra CP2500 RTM of the target machine, and to the serial port of the host machine.**
4. **Use the Tip utility on the host system to establish a full-duplex terminal connection with the Netra CP2500 board.**
5. **At the UNIX prompt in a command tool or shell tool, type:**

```
# tip -9600 /dev/ttya
```

2.8 Initial Power On and Firmware Upgrade

2.8.1 Powering On the System

Note – In order for the Netra CP2500 board to power on, the cPSB chassis must contain a management controller board.

1. **Power on the chassis that contains the Netra CP2500 board.**

   The board will run power-on self-tests (POST). For additional details on using POST, see Chapter 4.

2. **After running POST, install the Solaris Operating System on the Netra CP2500 board.**

   Refer to the *Netra CP2500 Board Release Notes* (819-1748) for information about the software installation and patch information.

2.8.2 Booting From a PMC Disk

To boot from a PMC disk installed on the Netra CP2500 board, you will need to change the default boot device from the OpenBoot PROM prompt.

To boot from the PMC disk, use the `setenv` command to change the `boot-device` parameter. The following is an example of the `setenv` command and output.

```
ok setenv boot-device pmc0/disk net
boot-device = pmc0/disk net
ok
```

Where `pmc0` corresponds to a disk installed in the PMC slot.

Note – The preceding `setenv` command can be used only when the board is installed in a standalone chassis. If the board is installed in a Netra CT 410 or CT 810 server, you will need to set the boot device using the Netra CT boot device variables. Refer to the *Netra CT Server System Administration Guide* (819-2743).

2.8.3 Determining Firmware Versions

If the installed firmware version is not current, update the OpenBoot PROM before continuing with the board installation (see Section 2.8.4, "Upgrading the OpenBoot PROM and SMC Firmware" on page 2-26).

2.8.3.1 Determining Firmware Versions From OpenBoot PROM Prompt

To determine the installed OpenBoot PROM version, use the `.version` OpenBoot PROM command at the `ok` prompt. See the following example for typical `.version` command output.

```
ok .version
Release 4.x.y created 2005/10/17 09:40
OBP 4.x.y 2005/10/17 09:40 Netra(tm) CP2500
OBDIAG 4.x.y 2005/08/06 10:28
POST 4.x.y 2005/09/06 10:51
ok
```

To determine the installed SMC firmware version, use the `.properties` command at the OpenBoot PROM prompt. See the following example for typical `.properties` command output.

```
ok cd ipmc
ok .properties
firmware-version          SMC Firmware Version 5.1.8
                          SMC Boot Code Version 5.15.1
                          CPLD Version 1.1
reg                       00000000 00000320 00000002
interrupt-priorities      00000003
interrupts                00000001
                          00000002
#size-cells               00000000
#address-cells            00000001
protocol                  SUNW,kcs-smc
compatible                SUNW,smc-ipmi
                          nct-ds80ch11-smc
device_type               ipmc
name                      ipmc
ok
```

2.8.3.2 Determining Firmware Versions From the Solaris Prompt

Use the `prtconf` command at a Solaris terminal prompt to display the OpenBoot PROM firmware version of the board.

```
$ /usr/sbin/prtconf -V
OBP 4.x.y 2005/10/17 09:40
```

Use the `prtpicl` command at a Solaris terminal prompt to display the SMC firmware version of the board.

```
# prtpicl -v | grep SMC
                    | SMC Firmware Version 5.1.8 |
                    | SMC Boot Code Version 5.15.1 |
```

2.8.4 Upgrading the OpenBoot PROM and SMC Firmware

The board's firmware can be upgraded using a patch downloaded from the SunSolve^{sm} web site. The Netra CP2500 board firmware patch contains the binary files for both the SPARC OpenBoot PROM firmware and the SMC firmware. The FWupdate installation tool enables you to update the firmware while the board is running the Solaris Operating System.

Note – Refer to the README file included with the Netra CP2500 firmware patch. The README file might contain a different upgrade procedure than is documented in this section. The README file also contains known issues and limitations specific to the firmware version included with the patch.

---

1. **Download the latest Netra CP2500 board firmware updates from the SunSolve web site.**

   Contact your Sun Services representative for information about the latest Netra CP2500 firmware patch.

2. **Ensure that the board has booted and is running the Solaris Operating System.**

   If your Netra CP2500 board is currently running the Solaris Operating System, skip to the next step. Otherwise, type the following at the board's OpenBoot PROM `ok` prompt to boot the operating system:

   ```
   ok boot
   ```

3. **After the board has booted the Solaris Operating System, open a terminal window and log into the board as superuser.**

   See Section 2.7, "Setting Up an Assembled Netra CP2500 Board" on page 2-22, for instructions on logging into the board.

4. **Change directories to directory where you extracted the firmware patch.**

   For example, if you extracted the files to `/var/tmp`, type:

   ```
   # cd /var/tmp/patch-number
   ```

   Where *patch_number* is the number and revision of the firmware patch.

5. **Use the FWupdate tool to update the SPARC® OpenBoot PROM and SMC firmware.**

   Use the full path and file name of the firmware binaries when updating the firmware. The `/var/tmp` directory is shown in the following examples.

   - To update the SPARC OpenBoot PROM firmware, type:

```
# /usr/platform/SUNW,Netra-CP2500/sbin/FWupdate \
-s -f /var/tmp/patch-number/FWBin/CP2500.SPARC.revision -t sparc
```

   Where *patch-number* is the name of the patch and *revision* is the OpenBoot PROM firmware level.

   - To update the SMC firmware, type:

```
# /usr/platform/SUNW,Netra-CP2500/sbin/FWupdate \
-s -f /var/tmp/patch-number/FWBin/CP2500.SMC.revision -t smc
```

   Where *patch_number* is the name of the patch and *revision* is the OpenBoot PROM firmware level.

Note – For more information about using the FWupdate tool, refer to the README file included with the firmware patch.

---

6. **Reboot the Netra CP2500 board to make the new firmware version effective.**

   Refer to your server or chassis documentation for specific instructions on rebooting the board in your environment.

CHAPTER 3

Configuring Netra CP2500 Board Software

This chapter contains the following sections:

3.1 Hot-Swap Information

3.1.1 Hot-Swapping the Netra CP2500 Board

If the Solaris Operating System is running on a Netra CP2500 board, and you open the board's ejector levers, you will see a message that the operating system will shut down. When the OS achieves the OpenBoot PROM `ok` prompt level, you can safely remove the board.

CODE EXAMPLE 3-1 displays a typical example of these Solaris OS shut down messages, where *hostname* is the host name of the Netra CP2500 board being shut down.

CODE EXAMPLE 3-1 Netra CP2500 Board Shut Down Messages

```
Broadcast Message from root (???) on hostname Wed Dec  7 15:09:22...
THE SYSTEM hostname IS BEING SHUT DOWN NOW ! ! !
Log off now or risk your files being damaged


#
INIT: New run level: 0
The system is coming down.  Please wait.
System services are now being stopped.
Dec  7 15:09:21 hostname last message repeated 1 time
Dec  7 15:09:39 hostname pseudo: pseudo-device: tod0
Dec  7 15:09:39 hostname genunix: tod0 is /pseudo/tod@0
Dec  7 15:09:39 hostname pseudo: pseudo-device: pm0
Dec  7 15:09:39 hostname genunix: pm0 is /pseudo/pm@0
Print services already stopped.
Dec  7 15:09:41 hostname syslogd: going down on signal 15
umount: /xfn busy
The system is down.
syncing file systems... done
Program terminated
ok
```

3.1.1.1 Hot-Swap Status LED

The blue hot-swap LED, located on the front panel of the Netra CP2500 board (FIGURE 3-2), lights up when the hot-swap function is enabled by the system software. The hot-swap LED indicates that the board can be extracted from the chassis. When a board is inserted into a cPSB system, the LED is lit automatically until the hardware connection process is completed. The LED then remains off until the extraction is once again enabled by the system software.

FIGURE 3-1 shows how to release the Netra CP2500 levers. FIGURE 3-2 shows the location of the blue hot-swap LED.

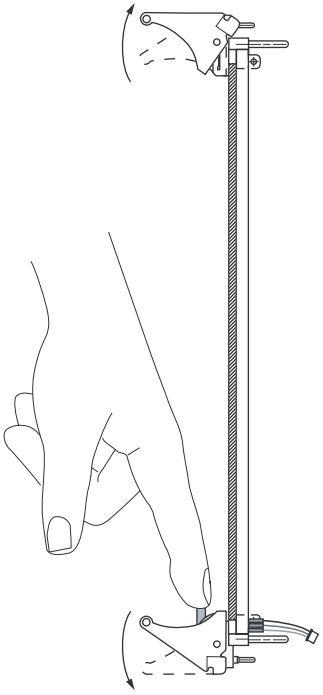

FIGURE 3-1 Releasing the Netra CP2500 Ejector Levers

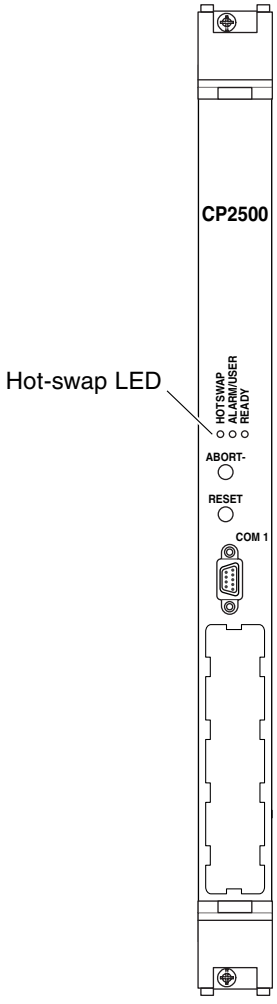

FIGURE 3-2 Blue Hot-Swap LED Location

3.1.2 Retrieving Device Information

You use the Solaris platform information and control library (PICL) framework for obtaining the state and condition of the Netra CP2500 board, rather than the Solaris `cfgadm` framework used with other CompactPCI boards.

The PICL framework provides information about the system configuration that it maintains in the PICL tree. Within this PICL tree is a subtree named *FRU tree*, that represents the hierarchy of system FRUs with respect to a root node in the tree called *chassis*. The FRU tree represents physical resources of the system. The PICL tree is updated whenever a change occurs in the device status.

The `prtpicl -v` command shows the condition of all devices in the PICL tree. CODE EXAMPLE 3-2 displays example Netra CP2500 board output from the `prtpicl` command.

CODE EXAMPLE 3-2 `prtpicl` Command Output

```
# prtpicl -v
...
     frutree (picl, 36000005b5)
      :_class    picl
      :name      frutree
         chassis (fru, 36000005b8)
          :ConditionTime         Fri Dec  9 09:16:43 2005
          :Condition     ok
          :ChassisType   SUNW,NetraCT-810
          :StatusTime    Fri Dec  9 09:16:43 2005
          :State         configuring
          :_class        fru
          :name  chassis
             CPU (location, 36000005f8)
              :State     connected
              :AutoConfig        enabled
              :StatusTime        Fri Dec  9 09:16:54 2005
              :Power     on
              :PdevProbePath     /pci@1e,600000
              :devfs-path        /pci@1e,600000
              :GeoAddr   0x1
              :UnitAddress       1e,600000
              :bus-addr  0x1
              :Label     CPU 1
              :SlotType  cpci
              :_class    location
              :name      CPU
                 SUNW,Netra-CP2500 (fru, 3600000602)
                  :AdminLock     disabled
```

CODE EXAMPLE 3-2 `prtpicl` Command Output *(Continued)*

```
                :ConditionTime          Fri Dec  9 09:16:54 2005
                :Condition      ok
                :StatusTime     Fri Dec  9 09:16:54 2005
                :State          configured
                :FRUType        bridge/fhs
                :HostCPU
                :_class         fru
                :name  SUNW,Netra-CP2500
                   PMC-1 (location, 3600000605)
                    :devfs-path         /pci@1e,600000
                    :GeoAddr    0x1
                    :bus-addr   0x4
                    :Label      PMC
                    :SlotType   pci
                    :_class     location
                    :name       PMC-1
             ...
             RTM (location, 360000066c)
              :StatusTime         Fri Dec  9 09:16:43 2005
              :devfs-path         /pci@1f,700000
              :bus-addr   1,1
              :Label      RTM
              :SlotType   rtm
              :State      connected
              :GeoAddr    0x1
              :_class     location
              :name       RTM
                 RTM (fru, 3600000675)
                  :AdminLock      disabled
                  :Condition      ok
                  :State          configured
                  :FRUType        RTM
                  :_class         fru
                  :name  RTM
                     su0 (port, 360000067c)
                      :devfs-path         /pci@1e,600000/isa@7/serial@0,3f8
                      :PortType   serial
                      :GeoAddr    0x1
                      :bus-addr   0,3f8
                      :Label      COM A
                      :_class     port
                      :name       su0
                     su1 (port, 3600000684)
                      :devfs-path         /pci@1e,600000/isa@7/serial@0,2e8
                      :PortType   serial
                      :GeoAddr    0x2
                      :bus-addr   0,2e8
```

CODE EXAMPLE 3-2 `prtpicl` Command Output *(Continued)*

```
                    :Label      COM B
                    :_class     port
                    :name       su1
                   bge0 (port, 360000068c)
                    :devfs-path         /pci@1f,700000/network@1
                    :PortType   network
                    :GeoAddr    0x1
                    :bus-addr   1
                    :Label      ENET A
                    :_class     port
                    :name       bge0
                   bge1 (port, 3600000694)
                    :devfs-path         /pci@1f,700000/network@1,1
                    :PortType   network
                    :GeoAddr    0x2
                    :bus-addr   1,1
                    :Label      ENET B
                    :_class     port
                    :name       bge1
                   bge2 (port, 360000069c)
                    :devfs-path         /pci@1f,700000/network@3
                    :PortType   network
                    :GeoAddr    0x3
                    :bus-addr   3
                    :Label      ENET C
                    :_class     port
                    :name       bge2
                   bge3 (port, 36000006a4)
                    :devfs-path         /pci@1f,700000/network@3,1
                    :PortType   network
                    :GeoAddr    0x4
                    :bus-addr   3,1
                    :Label      ENET D
                    :_class     port
                    :name       bge3
```

TABLE 3-1 shows the FRU tree (`frutree`) entries and properties that describe the condition of the Netra CP2500 board.

TABLE 3-1 PICL FRU Tree Entries and Description for the Netra CP2500 Board

FRU Tree Entry:Property	Entry Description	Example of Condition
`CPU (location) :State`	State of the receptacle or slot	`connected`
`CPU (fru) :Condition`	Condition of the board or occupant	`ok`
`CPU (fru) :State`	State of the board or occupant	`configured`
`CPU (fru) :FRUType`	FRU type	`bridge/fhs`

For more information on the PICL framework, refer to the `picld(1M)` man page.

3.2 Setting the Time of Day

The Netra CP2500 board does not have a battery backup to save the time of day (TOD) over reboots and power-outages. However, the board contains a capacitor that will keep the TOD during power-outages of 4 hours in length.

If the TOD is not powered through the capacitor, the TOD will be programmed with a default date and time of 01/01/2000 00:00:00 GMT. You can update the date and time using the Solaris `date` command.

To set the time of day manually after the power is restored:

- **As superuser, use the `date` command at a Solaris prompt to set the correct time.**

```
# date [mmddHHMMccyy]
```

where:

- *mm* is the current month.
- *dd* is the current day of the month.
- *HH* is the current hour of the day.
- *MM* is the current minutes past the hour.
- *cc* is the current century (a year divided by 100 and truncated to an integer) as a decimal number [00-99]. For example, *cc* is 19 for the year 1988 and 20 for the year 2007.
- *yy* is the current year.

Refer to the `date`(1M) command man page for additional information. After you set the date, you must reboot (but not power cycle) the system for the changes to take full effect. Failing to reboot can cause time conflicts among applications.

3.3 Downloading and Installing SunVTS

The Sun Validation Test Suite (SunVTS™ software) is a comprehensive software package that tests and validates the Netra CP2500 by verifying the configuration and function of most hardware controllers and devices on the board. SunVTS is used to validate a system during development, production, inspection, troubleshooting, periodic maintenance, and system or subsystem stressing. SunVTS can be tailored to run on various types of machines ranging from desktops to servers with modifiable test instances and processor affinity features.

You can perform high-level system testing by using the appropriate version of SunVTS. For detailed information on SunVTS support and downloads, refer to the following web site:

`http://www.sun.com/oem/products/vts/`

Download version 5.1PS11, or a future supported version, of the SunVTS software, if you want to test the Netra CP2500 board hardware.

Ensure that the SunVTS software version is compatible with the Solaris OS version being used.

You can find information about the SunVTS software version installed on your system by viewing the contents of the `.version` file:

```
# cat /opt/SUNWvts/bin/.version
```

To obtain SunVTS documentation, contact your local customer service representative or field application engineer.

Note – For security reasons, only a superuser is permitted to run SunVTS. Installation and starting instructions are included with the software when it is downloaded.

CHAPTER 4

Configuring and Using the Netra CP2500 Board Firmware

The Netra CP2500 board contains a modular firmware architecture that enables you to customize the initialization, test the firmware, and enable the installation of an operating system.

This platform also employs the system management controller (SMC), which controls the system management and hot-swap control, and some board hardware. The SMC configuration is controlled by separate firmware.

This chapter contains the following sections:

4.1 Firmware Initialization

Control flow at board startup is shown in FIGURE 4-1. Execution begins in the OpenBoot PROM. If you set the `diag-switch?` environmental variable to `true` (see Section 4.2, "Firmware Configuration Variables" on page 4-6 for more information), power-on self-tests (POST) will be run at startup.

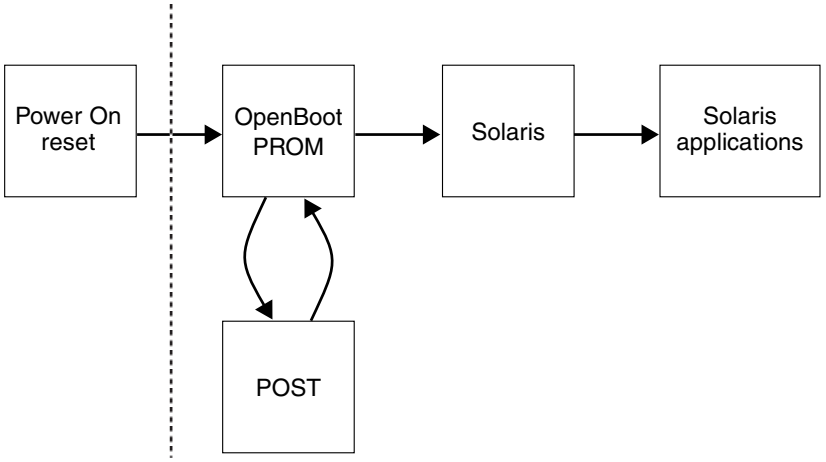

FIGURE 4-1 Control Flow From Power On for Firmware

4.1.1 OpenBoot PROM Operation

The OpenBoot PROM probes for devices and builds the device tree, which is a table that contains entries for how drivers communicate with connected hardware. Each line, or entry, of the device tree is a reference for the node entry for the peripheral in the `/dev` directory. The device tree is inherited by Solaris software as it is booted. The device tree can be seen by directory in the `/` directory. The device tree can be seen by typing `show-devs` at the `ok` prompt. CODE EXAMPLE 4-1 shows an example of a device tree.

CODE EXAMPLE 4-1 OpenBoot PROM `show-devs` Command Output

```
ok show-devs
/console
/i2c@1f,464000
/pci@1f,700000
/ppm@1e,0
/pci@1e,600000
/memory-controller@0,0
/SUNW,UltraSPARC-IIIi+@0,0
/multiplexer@0,0
/virtual-memory
/memory@m0,0
/aliases
/options
/openprom
/chosen
/packages
/i2c@1f,464000/idprom@0,ae
/i2c@1f,464000/nvram@0,ae
/pci@1f,700000/network@3,1
/pci@1f,700000/network@3
/pci@1f,700000/scsi@2,1
/pci@1f,700000/scsi@2
/pci@1f,700000/network@1,1
/pci@1f,700000/network@1
/pci@1f,700000/scsi@2,1/tape
/pci@1f,700000/scsi@2,1/disk
/pci@1f,700000/scsi@2/tape
/pci@1f,700000/scsi@2/disk
/pci@1e,600000/pci@1
/pci@1e,600000/isa@7
/pci@1e,600000/pmu@6
/pci@1e,600000/pci@1/pci@11
/pci@1e,600000/pci@1/pci@10
/pci@1e,600000/pci@1/pci@11/SUNW,isptwo@4
/pci@1e,600000/pci@1/pci@11/SUNW,isptwo@3
```

CODE EXAMPLE 4-1 OpenBoot PROM `show-devs` Command Output *(Continued)*

```
/pci@1e,600000/pci@1/pci@11/SUNW,qfe@1,1
/pci@1e,600000/pci@1/pci@11/pci108e,1000@1
/pci@1e,600000/pci@1/pci@11/SUNW,qfe@0,1
/pci@1e,600000/pci@1/pci@11/pci108e,1000@0
/pci@1e,600000/pci@1/pci@11/SUNW,isptwo@4/st
/pci@1e,600000/pci@1/pci@11/SUNW,isptwo@4/sd
/pci@1e,600000/pci@1/pci@11/SUNW,isptwo@3/st
/pci@1e,600000/pci@1/pci@11/SUNW,isptwo@3/sd
/pci@1e,600000/pci@1/pci@10/SUNW,isptwo@3
/pci@1e,600000/pci@1/pci@10/SUNW,qfe@1,1
/pci@1e,600000/pci@1/pci@10/pci108e,1000@1
/pci@1e,600000/pci@1/pci@10/SUNW,qfe@0,1
/pci@1e,600000/pci@1/pci@10/pci108e,1000@0
/pci@1e,600000/pci@1/pci@10/SUNW,isptwo@3/st
/pci@1e,600000/pci@1/pci@10/SUNW,isptwo@3/sd
/pci@1e,600000/isa@7/serial@0,2e8
/pci@1e,600000/isa@7/serial@0,3f8
/pci@1e,600000/isa@7/rtc@0,70
/pci@1e,600000/isa@7/flashprom@2,0
/pci@1e,600000/isa@7/ipmc@0,320
/pci@1e,600000/isa@7/ipmc@0,320/i2c@5
/pci@1e,600000/isa@7/ipmc@0,320/i2c@5/rtm-fru-prom@7,a0
/pci@1e,600000/isa@7/ipmc@0,320/i2c@5/hardware-monitor@5,5c
/pci@1e,600000/isa@7/ipmc@0,320/i2c@5/motherboard-fru-prom@5,a4
/pci@1e,600000/pmu@6/gpio@80000000,8a
/pci@1e,600000/pmu@6/i2c@0,0
/pci@1e,600000/pmu@6/i2c@0,0/dimm-spd@0,a2
/pci@1e,600000/pmu@6/i2c@0,0/dimm-spd@0,a0
/openprom/client-services
/packages/SUNW,asr
/packages/SUNW,fru-device
/packages/SUNW,i2c-ram-device
/packages/obp-tftp
/packages/kbd-translator
/packages/console-pkg
/packages/dropins
/packages/terminal-emulator
/packages/disk-label
/packages/deblocker
/packages/SUNW,builtin-drivers
```

The OpenBoot PROM also contains aliases for some of the devices shown in the device tree. These aliases can simplify hardware access at the `ok` prompt. CODE EXAMPLE 4-2 shows how the OpenBoot `devalias` command lists the available device tree aliases.

CODE EXAMPLE 4-2 OpenBoot PROM `devalias` Command Output

```
ok devalias
output-mux               /multiplexer:output
input-mux                /multiplexer:input
ipmi-console             /console
ssp-serial               /console
ttyi                     /console
ipmc                     /pci@1e,600000/isa@7/ipmc@0,320
hsc                      /pci@1e,600000/isa@7/ipmc@0,320
net2                     /pci@1f,700000/network@1,1
net                      /pci@1f,700000/network@1
disk2                    /pci@1f,700000/scsi@2,1/disk@0,0
cdrom2                   /pci@1f,700000/scsi@2,1/cdrom@2,0:f
scsi2                    /pci@1f,700000/scsi@2,1
disk                     /pci@1f,700000/scsi@2/disk@0,0
cdrom                    /pci@1f,700000/scsi@2/cdrom@2,0:f
scsi                     /pci@1f,700000/scsi@2
ide                      /pci@1e,600000/ide@4
ttyb                     /pci@1e,600000/isa@7/serial@0,2e8
ttya                     /pci@1e,600000/isa@7/serial@0,3f8
name                     aliases
```

4.2 Firmware Configuration Variables

This section provides information on the firmware configuration variables, which are saved in the 8 Kbyte SEEPROM. The SEEPROM's contents are preserved across board power-cycles.

4.2.1 OpenBoot PROM Configuration Variables

TABLE 4-1 describes the OpenBoot PROM configuration variables stored in the NVRAM and displayed by the OpenBoot PROM `printenv` command. Use the `setenv` OpenBoot command to modify the environment variables. The boot process is controlled by several variables. For the values of each variable, refer to the *OpenBoot 4.x Command Reference Manual*, which is included with the Solaris documentation.

TABLE 4-1 OpenBoot PROM NVRAM Configuration Variables

Variable Name	Default Value	Description
`ansi-terminal`	`true`	When `true`, uses an ANSI terminal.
`asr-policy`	`normal`	Defines the Automatic system recovery (ASR) policy for the `asr-package`. • `normal` – user-disabled devices cannot be used • `service` – user-disabled devices will be used
`auto-boot-on-error?`	`false`	If variable is set to `true`, the board will attempt to reboot if a firmware error occurs.
`auto-boot?`	`true`	If variable is set to `true`, the board boots automatically after a power-on reset.
`boot-command`	`boot`	Command that is executed if `auto-boot?` is set to `true`.
`boot-device`	`disk net`	Device from which to boot.
`boot-file`		File from which to boot (an empty string lets the secondary boot choose the default).
`cpci-probe-list`	`0,1,2,3,4,5,6,7 ,8,9,a,b, . . .`	Defines the probe list for devices present on CompactPCI bus.
`diag-device`	`net`	Device from which to boot.
`diag-file`		File from which to boot in diagnostic mode.
`diag-level`	`max`	Sets the level of diagnostics to run (`max` or `min`).

TABLE 4-1 OpenBoot PROM NVRAM Configuration Variables *(Continued)*

Variable Name	Default Value	Description
diag-out-console	false	Reserved.
diag-passes	1	Repeat each diagnostic test the number of times specified.
diag-script	normal	Determines which devices are tested by OpenBoot diagnostics.
diag-switch?	false	If variable is set to true, POST is executed when system is next powered on.
diag-trigger	none	Reserved.
error-reset-recovery	sync	Command to execute following a system reset generated by an error.
fcode-debug?	false	OpenBoot PROM debug variable.
input-device	ttya	Input device used at power-on (usually keyboard, TTYA, or TTYB).
load-base	16384	Base address where the client image is loaded by the OpenBoot PROM.
local-mac-address?	false	If variable is set to true, network drivers use the board's MAC address, and not the system's address.
multiplexer-input-devices	ttya ttyi	Default input console multiplexer (mux) devices.
multiplexer-output-devices	ttya ttyi	Default output console multiplexer (mux) devices.
network-boot-arguments		Sets NVRAM arguments for network booting.
nvramrc		Contents of the NVRAMRC.
oem-banner	No default	Custom OEM banner (enabled by oem-logo? true).
oem-banner?	false	If variable is set to true, uses custom OEM banner.
oem-logo	No default	Byte array custom OEM logo (enabled by oem logo? true); displayed in hexadecimal numbers.
oem-logo?	false	If true, uses custom OEM logo, otherwise, uses Sun logo.
output-device	ttya	Console output device (usually a screen, TTYA, or TTYB).
screen-#columns	80	Screen width in columns.
screen-#rows	34	Screen height in rows.

TABLE 4-1 OpenBoot PROM NVRAM Configuration Variables *(Continued)*

Variable Name	Default Value	Description
scsi-initiator-id	7	Sets the SCSI bus address of host adapter, with a range of 0-7.
security-#badlogins	No default	OpenBoot PROM internal use.
security-mode	No default	Firmware security level (none, command, or full). • none: no password required. • command: all commands except for boot and go require password. • full: all commands except for go require password.
security-password	No default	Set the firmware security password (never displayed).
service-mode?	false	Reserved.
test-args		Sets configuration arguments for POST and OpenBoot diagnostics tests.
ttya-ignore-cd	true	If variable is set to true, the operating system ignores TTYA carrier-detect.
ttya-mode	9600,8,n,1,-	TTYA settings (baud, #bits, parity, #stop, handshake).
ttya-rts-dtr-off	false	If variable is set to true, the operating system does not assert DTR and runs on TTYA.
ttyb-ignore-cd	true	If variable is set to true, the operating system ignores TTYB carrier-detect.
ttyb-mode	9600,8,n,1,-	TTYB settings (baud, #bits, parity, #stop, handshake).
ttyb-rts-dtr-off	false	If variable is set to true, the operating system does not assert DTR and runs on TTYB.
use-nvramrc?	false	If variable is set to true, executes commands in NVRAMRC during the board start-up.
verbosity	min	Sets the amount and detail of firmware message output. Can be set to min, normal, or max.

Note – The diag-switch? and diag-level variables listed in TABLE 4-1 affect the path through the various embedded tests.

4.3 System Flash PROM Memory Map

The node board boots from the 2 Mbyte system flash PROM device, which contains the POST code and OpenBoot PROM. The contents map of this PROM is shown in FIGURE 4-2.

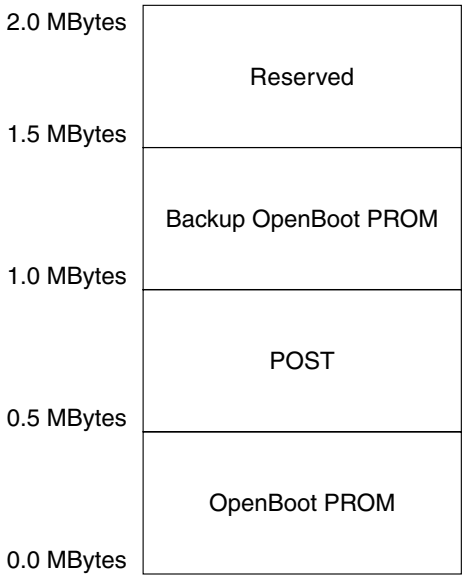

FIGURE 4-2 System Flash PROM Map

4.4 Environmental Monitoring Support at OpenBoot PROM

The Netra CP2500 board has an intelligent fault detection environmental monitoring system to increase uptime and manageability at OpenBoot PROM. The system management controller (SMC) module on the Netra CP2500 board supports the temperature monitoring functions. Environmental monitoring tracks the following at regular intervals at the `ok` prompt:

- CPU heat sink thermal sensor
- Ejection switch
- ENUM signal

Note – Refer to the *Netra CP2500 Board Programming Guide* (817-1331) for additional information about the environmental monitoring features of the Netra CP2500 board.

4.4.1 CPU Thermal Sensor

At the OpenBoot PROM level, when an overtemperature condition occurs, corresponding messages are displayed on the console. The OpenBoot PROM displays the warning messages as soon as the board temperature reaches the warning temperature and is still below the critical temperature. The critical messages are displayed as soon as the board temperature reaches the critical temperature. Finally, the shutdown messages are displayed when the board temperature reaches the shutdown temperature.

Use the `show-sensors` command at OpenBoot PROM `ok` prompt to display the readings of all the temperature sensors on the board.

When the CPU temperature reaches the warning temperature limit, the following message is displayed at the `ok` prompt at regular intervals:

```
<<< !!! ALERT!!! Upper Non-critical - going high >>>
     The current threshold setting is: value
     The current temperature is      : value
```

When the CPU temperature reaches the critical temperature limit, the following message is displayed at the `ok` prompt at regular intervals:

```
<<< !!! ALERT!!! Upper Critical - going high >>>
     The current threshold setting is: value
     The current temperature is      : value
```

The warning, critical, and shutdown temperature values are set by the SMC. You cannot configure them at the OpenBoot PROM prompt. However, you can set these temperature values on a board running the Solaris Operating System. Refer to the *Netra CP2500 Board Programming Guide* (819-1749) for instructions.

4.4.2 Reading the CPU Temperature Limits

You can access the CPU temperature sensor current readings and environmental monitoring settings from the Solaris prompt by using the `prtpicl` and `prtdiag` commands. Sample output is listed after each command.

`prtpicl` command example:

```
# prtpicl -c temperature-sensor -v
 CPU-sensor (temperature-sensor, 2600000041f)
            :Condition         ok
            :HighPowerOffThreshold  123
            :HighShutdownThreshold        118
            :HighWarningThreshold         110
            :LowPowerOffThreshold  -20
            :LowShutdownThreshold  -10
            :LowWarningThreshold  -5
            :Temperature            74
            :Label         Ambient
            :GeoAddr       0xe
            :_class        temperature-sensor
            :name          CPU-sensor
```

`prtdiag` command example:

```
# prtdiag -v

CPU Node Temperature Information
--------------------------------
Temperature Reading: 85

Critical Threshold Information
------------------------------
High Power-Off Threshold           123
High Shutdown Threshold            118
High Warning Threshold             110
Low Power Off Threshold           -20
Low Shutdown Threshold            -10
Low Warning Threshold             -5
```

TABLE 4-2 shows which Solaris commands and values correspond to the environmental monitoring warning that runs when the CPU temperature exceeds the set limit.

TABLE 4-2 Description of Values Displayed by Solaris Commands

Environmental Monitoring Warning	`prtpicl`	`prtdiag`
The first-level temperature warning is displayed.	`HighWarningThreshold`	`High Warning Threshold`
The second-level temperature warning is displayed.	`HighShutdownThreshold`	`High Shutdown Threshold`
The CPU shutdown message is displayed and the CPU is shut off.	`HighPowerOffThreshold`	`High Power-Off Threshold`

4.5 System Management Controller (SMC) Firmware

The field upgradeable SMC firmware supports features such as Netra CP2500 resources, temperature monitoring, control of the power subsystem, IPMI communication with other boards, configurable reset handling, hot-swap capability, and watchdog timer heartbeat mechanism. The SMC firmware also has its own built-in self-test at power up. The SMC consists of DS80CH11, which is an 8051-compatible chip, and the PSD833F2 memory chip. Inside the PSD833F2 chip are the main flash and the boot flash and SRAM for data storage. The host CPU sends commands and data to the SMC by way of the serial bus.

The SMC architecture enables you to update the SMC firmware from a Solaris command prompt. You should update the SMC firmware to modify the firmware during a field upgrade, for fixing bugs, adding enhancements or new features, or providing special code for a specific OEM customer.

The SMC is capable of performing a flash update on its main and boot flash memory. The main flash can flash update the boot flash, and the boot flash can flash update the main flash. The boot code contains the minimum code to enable the system to boot to the `ok` prompt if the main flash fails, and to switch from boot flash to main flash for execution. Therefore, any attempt to perform a flash update of the boot flash would be considered risky and should not be done often.

Note – Due to interdependency between OpenBoot PROM, SMC, and hardware, you must take into account compatibility between various parts of the system among different version numbers when performing flash update.

4.5.1 SMC Configuration Block

The SMC power-on behavior and other attributes are stored in a 16-byte configuration block. This configuration block is stored in an accessible SEEPROM. In the absence of this configuration block, SMC boots up in a default mode. At the OpenBoot PROM level, the `setsmcenv` and `printsmcenv` commands in the SMC node are used to set parameters in the configuration block of SMC. The `printsmcenv` command prints the value of the parameters in the SMC configuration block.

To view the settings on the configuration block, read the block using the `printsmcenv` command. If you want to change the settings, use the `setsmcenv` command to change the SEEPROM configuration block. The following code example shows an example of the `printsmcenv` output.

```
ok printsmcenv
config-version      : 1
backplane-type      : 0
reset-mode          : 66
sir-xir-enable      : 2
byte5               : 0
chassis-type        : 5
flash-device        : 0
byte8               : 0
ha-signal-handler   : 1
poweron-vector      : 0
ipmi-checksum-ctlr  : 0
byteC               : 0
byteD               : 0
byteE               : 0
byteF               : 0
byte10              : 0
ok setsmcenv chassis-type 5
ok
```

Note – Each setting on the configuration block can change the behavior of the board significantly. For example, an invalid value in `config-version` would cause the OpenBoot PROM to reset the configuration block to the default values. Ask your Sun field application engineer for further details on the configuration block settings.

4.6 Using the Flash PROMs

On the Netra CP2500 board, both the system (boot) flash and the user flash memory reside on the same physical device. By default the system flash uses 2 MBytes of flash memory while the user flash uses 14 MBytes of flash memory.

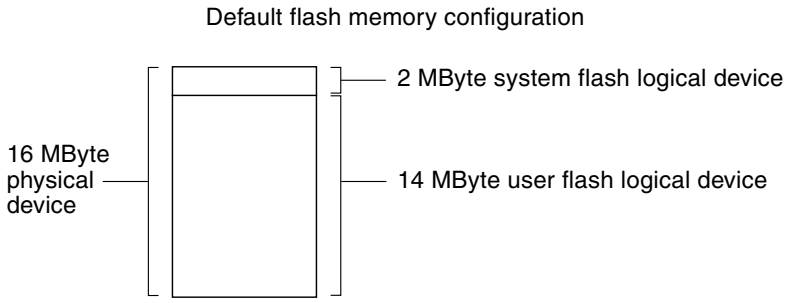

FIGURE 4-3 System Flash and User Flash Logical Devices on Same Physical Device

4.7 Booting the Board Using the Backup OpenBoot PROM

The main OpenBoot PROM image and a backup copy of the image are stored in the system flash memory (see Section 4.3, "System Flash PROM Memory Map" on page 4-9). If the OpenBoot PROM becomes corrupted, you can boot the board using the backup copy of the OpenBoot PROM. Booting this backup OpenBoot PROM will enable you to flash update and repair the main OpenBoot PROM image.

To boot the board from a backup image of the OpenBoot PROM in order to update the main OpenBoot PROM image:

1. **Power down the board and remove it from the server or chassis.**
2. **Retrieve the wrist strap from the adapter's shipping kit.**
3. **Attach the antistatic wrist strap:**
   a. **Attach the adhesive copper strip of the wrist strap to the metal chassis.**
   b. **Wrap the other end twice around your wrist, with the adhesive side against your skin.**

4. **Place the board on a static-free work area and locate the SW3301 switch on the board.**

   The SW3301 DIP switch bank is located on the component side of the board between the front panel and heat sink (see FIGURE 4-4).

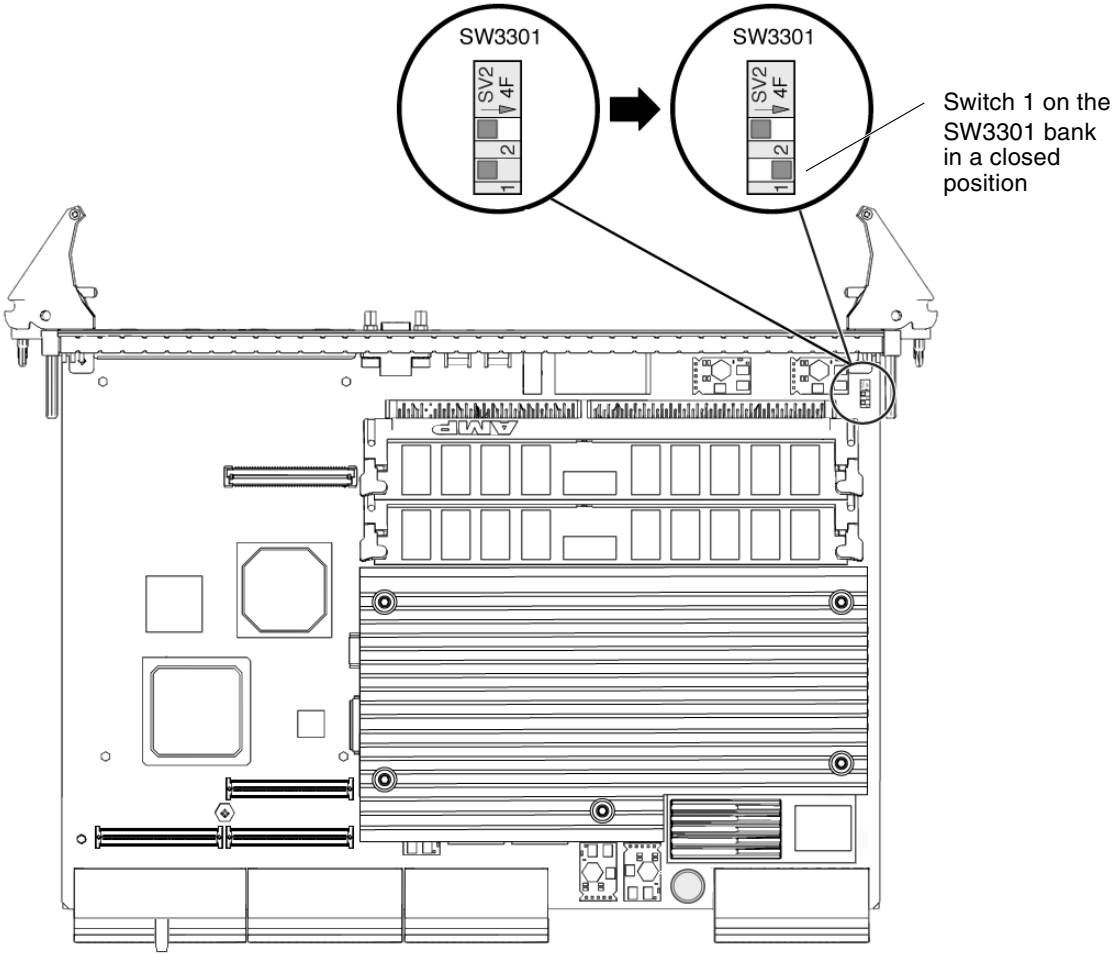

FIGURE 4-4 Setting Switch 1 on the SW3301 DIP Switch Bank to Closed

5. **Using a needle, metal pick, scribe tool, or small screwdriver, set switch 1 from open to closed.**

   The closed setting is in the same direction of the arrow located on the SW3301 DIP switch bank (see FIGURE 4-4). For more information about the SW3301 DIP switch settings, see Section B.4, "DIP Switch Settings" on page B-18.

6. **Install the Netra CP2500 board back in the chassis or server.**

   Enable the board to boot using the backup OpenBoot PROM and then start the Solaris OS.

7. **At a Solaris terminal prompt, update the main OpenBoot PROM firmware.**

   See Section 2.8.4, "Upgrading the OpenBoot PROM and SMC Firmware" on page 2-26, for the firmware upgrade procedure.

8. **After repairing the main OpenBoot PROM, power down the board and remove it from the chassis or server.**

9. **Place the board on a static-free work area.**

10. **Using a needle, metal pick, scribe tool, or small screwdriver, set switch 1 from closed to open.**

    The open setting is in the reverse direction of the arrow located on the SW3301 DIP switch bank (the open setting is also the default setting).

11. **Install the Netra CP2500 board back in the chassis or server.**

    Enable the board to boot using the main OpenBoot PROM and start the Solaris OS.

4.7.1 Updating the OpenBoot PROM and SMC Firmware

See Section 2.8.4, "Upgrading the OpenBoot PROM and SMC Firmware" on page 2-26, for the firmware upgrade procedure.

4.8 Firmware Diagnostics

The firmware contains a comprehensive set of hardware diagnostic modules that provide tests for most situations. FIGURE 4-1 shows the control flow relationship of the diagnostic modules with the system firmware. SunVTS can be executed from within the Solaris software if more tests are required. For more information, see Section 3.3, "Downloading and Installing SunVTS" on page 3-9.

The firmware diagnostic modules are:

- Power-on self-tests (POST)
- OpenBoot PROM diagnostics

The firmware diagnostics cover address and data bits on all system buses and exercise the function of the major hardware resources on the board.

Diagnostics can be performed at OpenBoot PROM level by using the `obdiag` command, or by typing individual test commands at the `ok` prompt. These test suites are similar to those in earlier OpenBoot PROM versions but they are comprised of drop-ins that can be placed by the user. Refer to the *OpenBoot 4.x Command Reference Manual* for additional information.

4.8.1 Setting Diagnostic Levels

The user interface for running POST at minimum or maximum remains the same. POST is executed when the `diag-switch?` environmental variable is set to `true`.

4.8.2 OpenBoot PROM On-Board Diagnostics

The OpenBoot PROM on-board diagnostics reside in the OpenBoot PROM drop-in. These diagnostics are described fully in the *OpenBoot 4.x Command Reference Manual*.

To execute the OpenBoot PROM on-board diagnostics, the system must be at the `ok` prompt. The OpenBoot PROM on-board diagnostics include:

- `watch-clock`
- `watch-net` and `watch-net-all`
- `probe-scsi`
- `test` *device path*
- `test-all`

4.8.3 OpenBoot Diagnostics

The OpenBoot Diagnostics are an enhancement of the traditional system tests. They reside in Forth script in a drop-in and are invoked with an interactive tool that is started from the `ok` prompt by typing `obdiag`.

When you start the OpenBoot Diagnostics, you should see the following menu:

```
ok obdiag
_____________________________________________________________________________
|                                o b d i a g                                  |
|_____________________________ _____________________________ _____________________________|
|                             |                             |                             |
|  1 ipmc@0,320               |  2 network@1                |  3 network@1,1              |
|  4 network@3                |  5 network@3,1              |  6 rtc@0,70                 |
|  7 serial@0,2e8             |  8 serial@0,3f8             |                             |
|_____________________________|_____________________________|_____________________________|
|       Commands: test test-all except help what setenv set-default exit      |
|_____________________________________________________________________________|
|                    diag-passes=1 diag-level=max test-args                   |
|_____________________________________________________________________________|
```

At the `obdiag` prompt, type `test 1` to display a printout similar to the following:

```
obdiag> test 1

          Alarmdiag Menu

          0 ..... Ethernet Port
          1 ..... Serial Port
          2 ..... Flash
          3 ..... Alarm Port
          4 ..... FRUid Present
          5 ..... FPGA Id
          6 ..... MidPlane Id
          7 ..... Continuity
          8 ..... Slot Leds
          9 ..... Disk Leds
         10 ..... Power Supply Leds
         11 ..... Fan Leds
         12 ..... SCB Leds
         13 ..... FTM Leds              (Netra CT 410 only)
         14 ..... Green Led Blink
         15 ..... FRU Present
         16 ..... Get Health
         17 ..... Power Supply Status
         18 ..... Fan Status
         19 ..... Power Supply Off/On   (Netra CT 810 only)
         20 ..... FruID Checksum
         21 ..... All Above
         22 ..... Quit
         23 ..... Display this Menu

Enter (0-21 tests, 22 -Quit, 23 -Menu) ===>
```

CHAPTER 5

Removing and Replacing Board Hardware

This chapter describes how to service the field replaceable hardware components of the Netra CP2500 board. This chapter contains the following sections:

Note – For instructions on servicing the Netra CP2500 rear transition modules, refer to the *Netra CP2500 Rear Transition Module Installation and Technical Reference Manual* (819-1753).

5.1 Field Replaceable Units

The following field-replaceable units (FRUs) are available from Sun Microsystems:

- Netra CP2500 board with 2 Gbytes of SDRAM
- Netra CP2500 host rear transition module (RTM-H)
- Netra CP2500 satellite/cPSB rear transition module (RTM-S)

Contact your field service representative for information about ordering these Netra CP2500 board and RTM FRUs.

5.2 Handling Equipment and Assembling Tools

Prior to servicing the Netra CP2500 board and its components, review and follow the safety guidelines outlined in Section 2.2, "Equipment and Operator Safety" on page 2-3.

Also, assemble a set of tools as described in Section 2.3, "Materials and Tools Required" on page 2-4.

Caution – The system is sensitive to static electricity. To prevent damage to the assembly, always connect an antistatic wrist strap between you and the system or chassis. Also, use an antistatic mat whenever possible.

Caution – Do not flex the Netra CP2500 board, as the surface-mounted components can break if the board is bent.

Caution – The heat sink on the board can be damaged by incorrect handling. Do not touch the heat sink while installing or removing a card. Hold the board only by the edges. If the heat sink is loose or broken, obtain a replacement card.

5.3 Displaying the Solaris FRU ID

The Sun field-replaceable unit ID (FRU ID) information is stored on a Netra CP2500 board SEEPROM. The FRU ID contains a short description of the board, part numbers, and manufacturing information that can be used to identify the board for service purposes.

To view the board's FRU ID information, use the `prtfru` command. Refer to the `prtfru`(1M) man page for further information on this command. The man page can be found on the Solaris documentation web site at:

`http://docs.sun.com/`

Using the `prtfru` command at the Solaris command line, you can display the Solaris Sun FRU ID information, which should look similar to the output shown in the following code example. TABLE 5-1 describes the fields shown in the subsequent example.

```
# prtfru
/frutree
/frutree/chassis (fru)
/frutree/chassis/CPU?Label=CPU 1
/frutree/chassis/CPU?Label=CPU 1/SUNW,Netra-CP2500 (container)
. . .
SEGMENT: SD
      /ManR
      /ManR/UNIX_Timestamp32: Wed Dec 27 16:00:00 PST 2006
      /ManR/Fru_Description: FRUID,PRGM INSTR,MBD,JADE
      /ManR/Manufacture_Loc:
      /ManR/Sun_Part_No: 5017031
      /ManR/Sun_Serial_No:
      /ManR/Vendor_Name:
      /ManR/Initial_HW_Dash_Level: 07
      /ManR/Initial_HW_Rev_Level:
      /ManR/Fru_Shortname: CPU
. . .
```

TABLE 5-1 Description of Fields in Typical `prtfru` Command Display Output

Field	Description
`/ManR/UNIX_Timestamp32:`	Board manufacturing timestamp
`/ManR/Fru_Description:`	Description for the board field-replaceable unit
`/ManR/Manufacture_Loc:`	Location where the board was manufactured
`/ManR/Sun_Part_No:`	Board identification part number
`/ManR/Sun_Serial_No:`	Board identification serial number
`/ManR/Vendor_Name:`	Name of the board vendor
`/ManR/Initial_HW_Dash_Level:`	Board identification dash number
`/ManR/Initial_HW_Rev_Level:`	Board identification revision number
`/ManR/Fru_Shortname:`	Short name for the board (such as CP2500)

5.4 Removing and Replacing the Board From the Chassis

This section provides a general procedure for removing and replacing a Netra CP2500 board from a cPSB chassis. Refer to your system documentation for board replacement instructions specific to the system and the software application environment.

Note – If you are removing and replacing a Netra CP2500 board from a Netra CT 410 or 810 server, refer to replacement procedures in the *Netra CT Server Service Manual* (819-2741).

5.4.1 Removing the Board From the Chassis

1. **Log into the Netra CP2500 board and gracefully stop any applications operating on the board.**

   Refer to your system's documentation for application procedures specific to your system or chassis.

2. **On the front of the chassis, and use a No. 1 screwdriver to loosen the ejection lever captive screws securing the board to the chassis.**

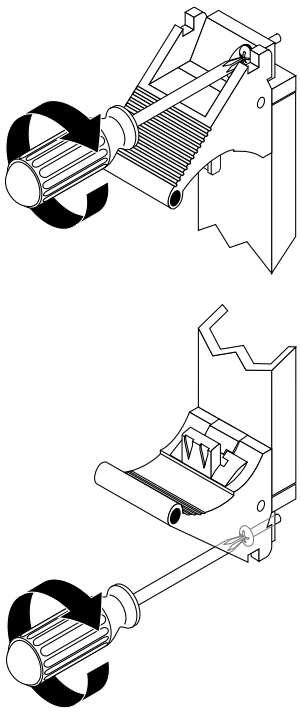

FIGURE 5-1 Loosening the Ejector Lever Captive Screws

3. **Unlock and press down on the lower ejector lever to start the hot-swap ejection process (see** FIGURE 5-2**).**

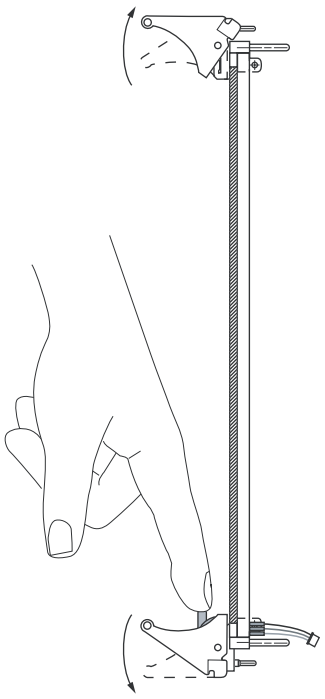

FIGURE 5-2 Releasing the Netra CP2500 Ejector Levers

4. **Wait until the front panel blue hot-swap LED lights up.**

   The Netra CP2500 board's hot-swap LED is located in the middle of the board's front panel, and not at the bottom of the panel, as it might be on other boards.

   When the blue hot-swap LED lights up, you can safely remove the board from the chassis.

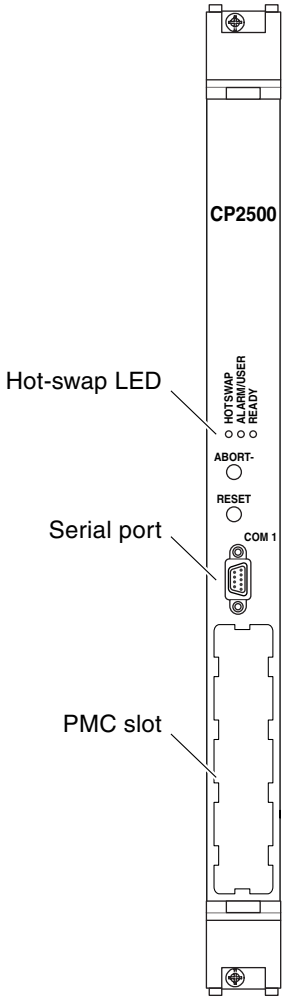

FIGURE 5-3 Blue Hot-Swap LED Location

5. **If necessary, remove any cable connected to the serial port, or any installed PMC device, from the board (see** FIGURE 5-3**).**

6. **Unlock the top ejection lever, and using two hands, simultaneously open the top and bottom ejector levers to disengage the board from chassis backplane (**FIGURE 5-4**).**

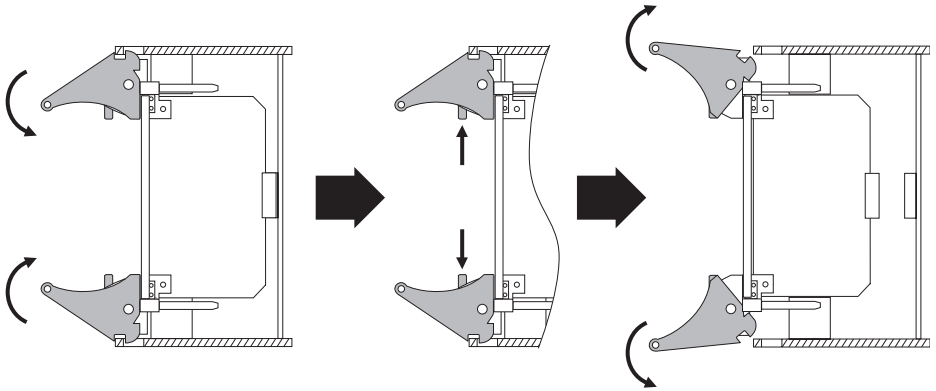

FIGURE 5-4 Unlocking and Using the Ejector Levers to Remove the Board

7. **Take antistatic precautions by attaching and electrically grounding an antistatic wrist strap.**

8. **Remove the board from the chassis and place the board on an ESD mat (if one is available) on a suitable work area.**

   If an ESD mat is not available, place the card on the antistatic envelope it was originally packaged in.

9. **(Optional) If you will be returning the board to Sun Services, remove the board's SEEPROM and any installed PMC device.**

   See the following removal procedures:

   - Section 5.5.2, "Replacing the SEEPROM" on page 5-10
   - Section 5.6.1, "Removing a PMC Device" on page 5-11

5.4.2 Replacing the Board in the System

Follow the installation procedures found in Chapter 2 to install the Netra CP2500 board into a cPSB chassis. Refer to your system documentation for board replacement instructions specific to the system and the software application environment.

5.5 Removing and Replacing the SEEPROM

The SEEPROM stores the board MAC address and host ID information. You do not need to replace the SEEPROM unless you are installing a replacement board that does not have the host ID information.

5.5.1 Removing the SEEPROM

1. **Remove the board from the chassis and place the board on an ESD mat (if one is available) on a suitable work area.**

   See Section 5.4.1, “Removing the Board From the Chassis” on page 5-4 for the board removal procedure.

   If an ESD mat is not available, place the card on the antistatic envelope it was originally packaged in.

2. **Take antistatic precautions by attaching and electrically grounding an antistatic wrist strap.**

3. **Carefully remove the plastic carrier containing the SEEPROM from the board.**

   The label is positioned on top of the SEEPROM carrier. See FIGURE 5-5 for the location of the board’s SEEPROM carrier.

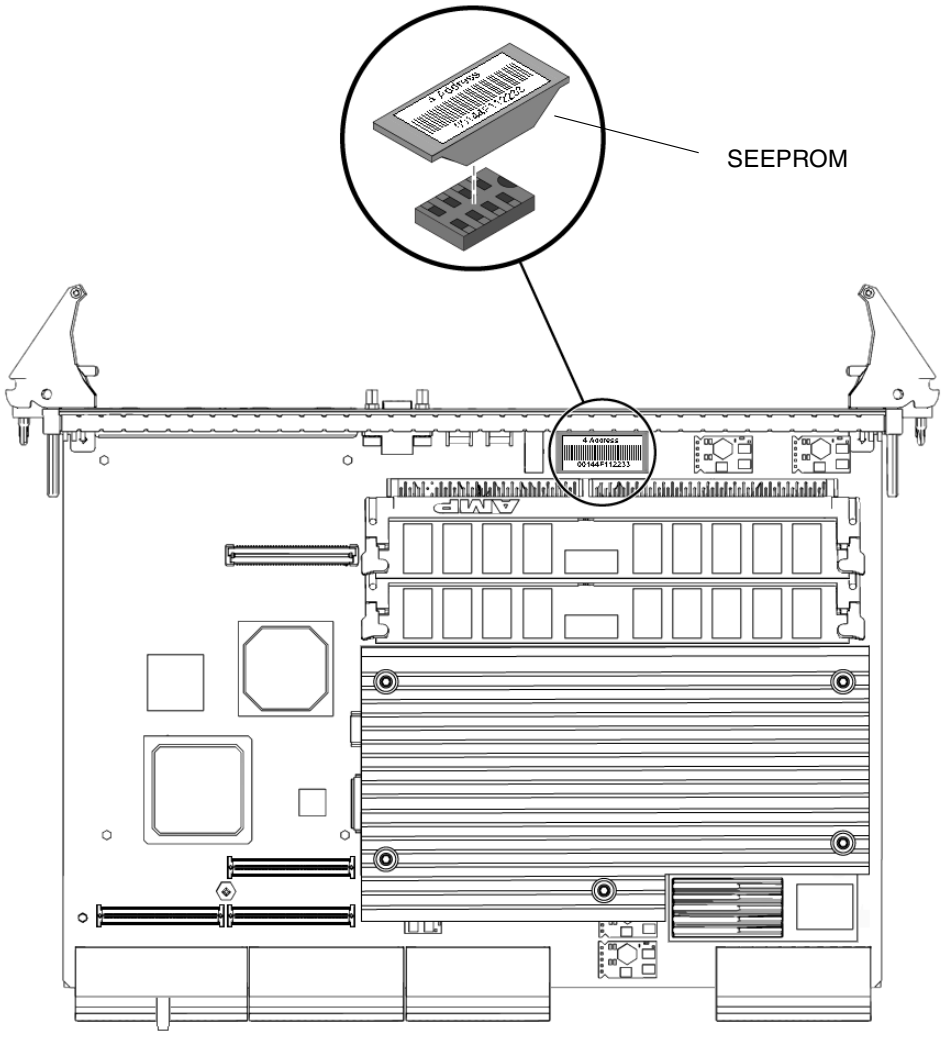

FIGURE 5-5 Removing the SEEPROM

4. **Store the removed plastic carrier, which includes the board's SEEPROM, in a safe location.**

5.5.2 Replacing the SEEPROM

For the SEEPROM replacement procedure, see Section 2.5.3, "Replacing the SEEPROM" on page 2-13.

5.6 Removing and Replacing a PMC Device

A PCI mezzanine card (PMC) is a slim, modular mezzanine card that provides additional functionality to the Netra CP2500 board. The board contains one PMC slot in which you can an install optional PMC device (see FIGURE 5-8 for the location of the slot).

Note – Because an installed PMC device will block access to the memory connector's retainer clips, you need to remove the PMC device prior to removing and replacing the memory modules.

5.6.1 Removing a PMC Device

1. **Remove the board from the chassis and place the board on an ESD mat (if one is available) on a suitable work area.**

   See Section 5.4.1, "Removing the Board From the Chassis" on page 5-4 for the board removal procedure.

   If an ESD mat is not available, place the card on the antistatic envelope it was originally packaged in.

2. **Take antistatic precautions by attaching and electrically grounding an antistatic wrist strap.**

3. **Flip the board over on the ESD mat so that the board's solder-side is facing you.**

   You can only access the screws securing the PMC device from the solder-side of the board.

4. **Using a No. 2 screwdriver, remove the four screws securing the PMC device to the board (FIGURE 5-6).**

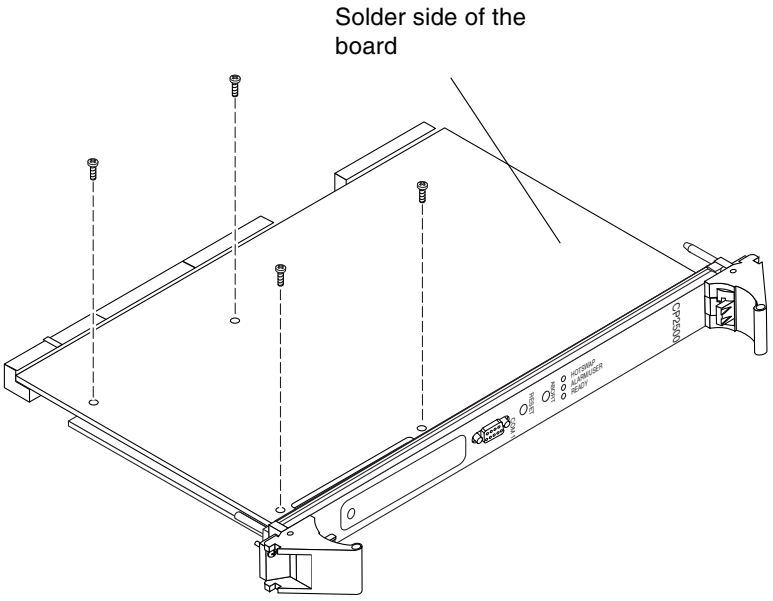

FIGURE 5-6 Loosening the PMC Device Screws

5. **Flip the board over on the ESD mat so that the component side of the board is facing you.**

6. **Carefully lift the PMC device up and off of the board's PMC connectors (see** FIGURE 5-7**).**

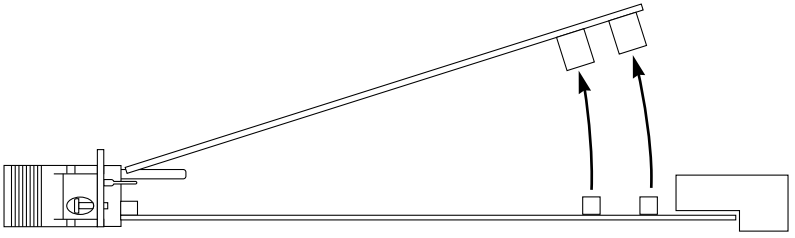

FIGURE 5-7 Lifting the PMC Device From the Board PMC Connectors

7. **Lift the PMC device up and off of the board and place the PMC device into an antistatic envelope.**

   Store the PMC device in a safe location.

8. **(Optional) Retrieve and replace the PMC filler panel onto the board's faceplate.**

Note – To meet EMI compliance standards, your board must contain either an installed PMC device or an installed PMC filler panel.

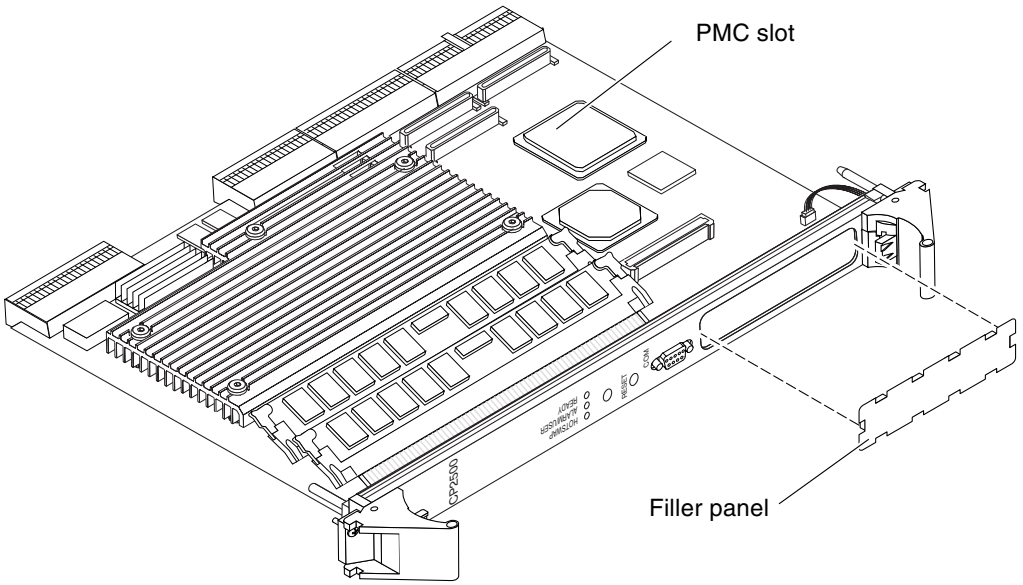

FIGURE 5-8 Replacing the PMC Filler Panel

9. **(Optional) If necessary, remove any installed rear transition module from the rear of the chassis.**

   Refer to your chassis documentation for the RTM removal procedure.

5.6.2 Replacing a PMC Device

For the PMC device replacement procedure, see Section 2.5.1, "Installing an Optional PMC Device" on page 2-7.

5.7 Removing and Replacing Memory Modules

The Netra CP2500 board accommodates two 184-pin, very low profile (VLP) DDR-1 SDRAM dual in-line memory modules (DIMMs). The board does not have any on-board memory, so it will not operate without installed memory modules. New Netra CP2500 boards that ship from Sun contain two preinstalled memory modules.

Caution – The Netra CP2500 board supports memory modules sold by Sun Microsystems only. Do not install a DIMM pair sold by any other vendor or manufacturer.

Note – You must install memory DIMMs in matched pairs. For example, the board will not operate if you install one 512 Mbyte DIMM and one 1 Gbyte DIMM on the board, or if you install only one DIMM on the board.

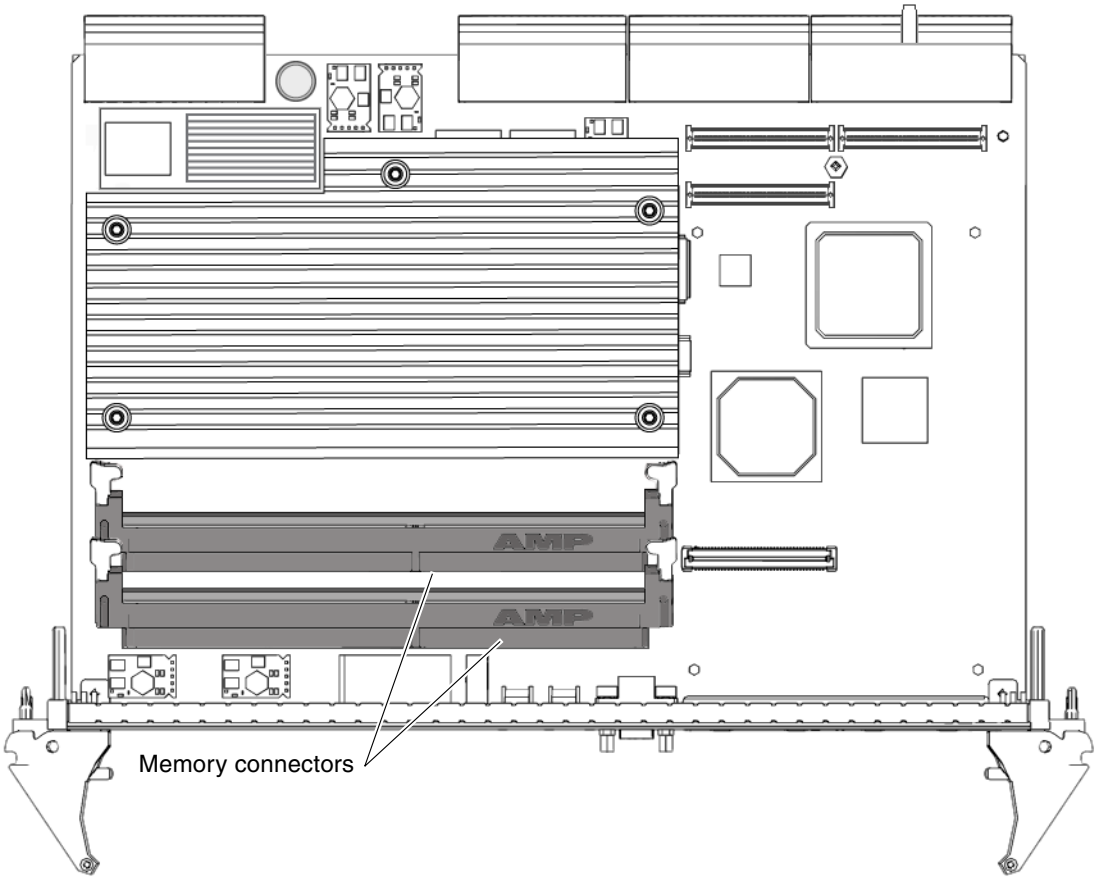

FIGURE 5-9 Location of Memory Connectors

5.7.1 Removing DIMM Memory Modules

You might need to remove a DIMM module from the Netra CP2500 board if you are returning the DIMM module pair or the board for service, or if you are replacing a DIMM module pair with another DIMM pair purchased from Sun Microsystems.

Note – Prior to removing memory modules from the Netra CP2500 board, you will need to remove any installed PMC device. An installed PMC device might block access to the memory connector's retainer clips. For PMC device removal procedures, see Section 5.6.1, "Removing a PMC Device" on page 5-11.

Note – Safely store the original factory-shipped DIMM and related DIMM packaging. You might want to store any removed DIMM in the new DIMM packaging, or use the packaging for service.

To remove a DIMM from the Netra CP2500 board, perform the following steps:

1. **Remove the board from the chassis and place the board on an ESD mat (if one is available) on a suitable work area.**

   See Section 5.4.1, "Removing the Board From the Chassis" on page 5-4, for the board removal procedure.

   If an ESD mat is not available, place the card on the antistatic envelope it was originally packaged in.

2. **Take antistatic precautions by attaching and electrically grounding an antistatic wrist strap.**

Caution – Always wear a grounded antistatic wrist strap when handling memory modules.

3. **For the DIMM you want to remove, simultaneously pull both DIMM retainer clips outward from the slot.**

   The DIMM releases outward at an angle of about 20 degrees (see FIGURE 5-10).

4. **Grasp the DIMM by the edges, and carefully pull it out of its connector (see FIGURE 5-10).**

   Ensure that you pull the DIMM out at an angle of about 20 degrees, or you might damage the DIMM.

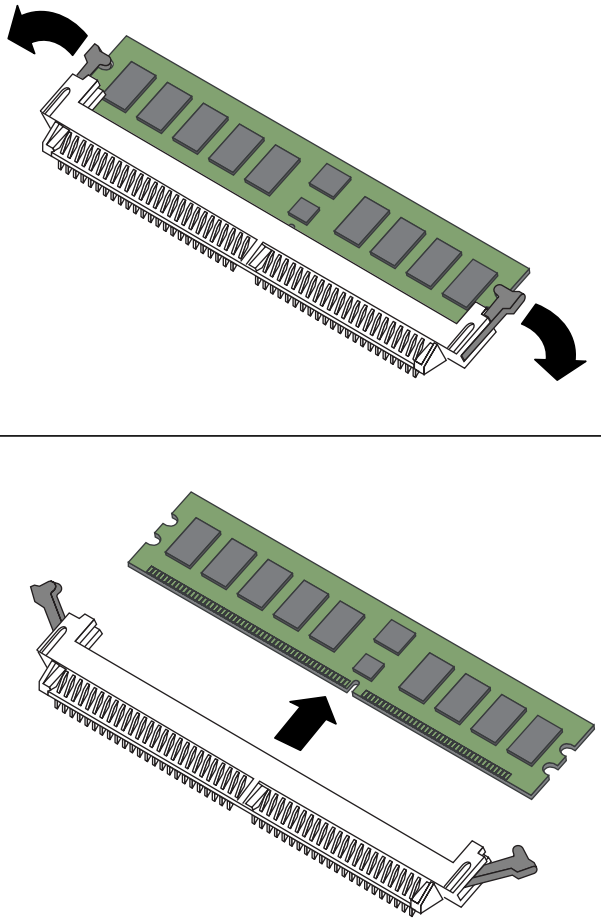

FIGURE 5-10 Removing a DIMM

5. **Place the DIMM in an antistatic bag.**
6. **Repeat this procedure for the second DIMM memory module.**

5.7.2 Installing Memory Modules

Note – Prior to installing memory modules on the Netra CP2500 board, you will need to first remove any installed PMC device. An installed PMC device may block access to the memory connector's retainer clips. For PMC device removal procedures, see Section 5.6.1, "Removing a PMC Device" on page 5-11.

The following procedure describes how to install memory onto the board.

Caution – Do not remove the memory module from its antistatic container until you are ready to install it on the board. Handle the module only by its edges. Do not touch module components or metal parts. Always wear a grounded antistatic wrist strap when handling modules.

1. **Place the board on an ESD mat (if one is available) on a suitable work area.**

   If an ESD mat is not available, place the card on the antistatic envelope it was originally packaged in.

2. **Take antistatic precautions by attaching and electrically grounding an antistatic wrist strap.**

Caution – Always wear a grounded antistatic wrist strap when handling memory modules.

3. **Locate the two DIMM connectors on the Netra CP2500 board.**

   Select the connectors where you will install the memory modules (see FIGURE 5-9). If you need to replace an existing memory module with a new module, see Section 5.7.1, "Removing DIMM Memory Modules" on page 5-15 for instructions on removing the DIMM module.

Caution – Do not install just one memory module. You must install memory in matched pairs, with each module containing the same memory capacity.

4. **Carefully pull the memory connector's retainer clips open (see FIGURE 5-11).**

5. **Remove the DIMM from its protective packaging, holding the module only by the edges.**

6. **Holding the DIMM at approximately a 20-degree angle to the board, insert the bottom edge of the DIMM into the bottom of the slot connector (see FIGURE 5-11).**

   The socket and module are both keyed, which means the module can be installed one way only. With even pressure, push simultaneously on both upper corners of the DIMM until its bottom edge (the edge with the gold fingers) is firmly seated in the connector.

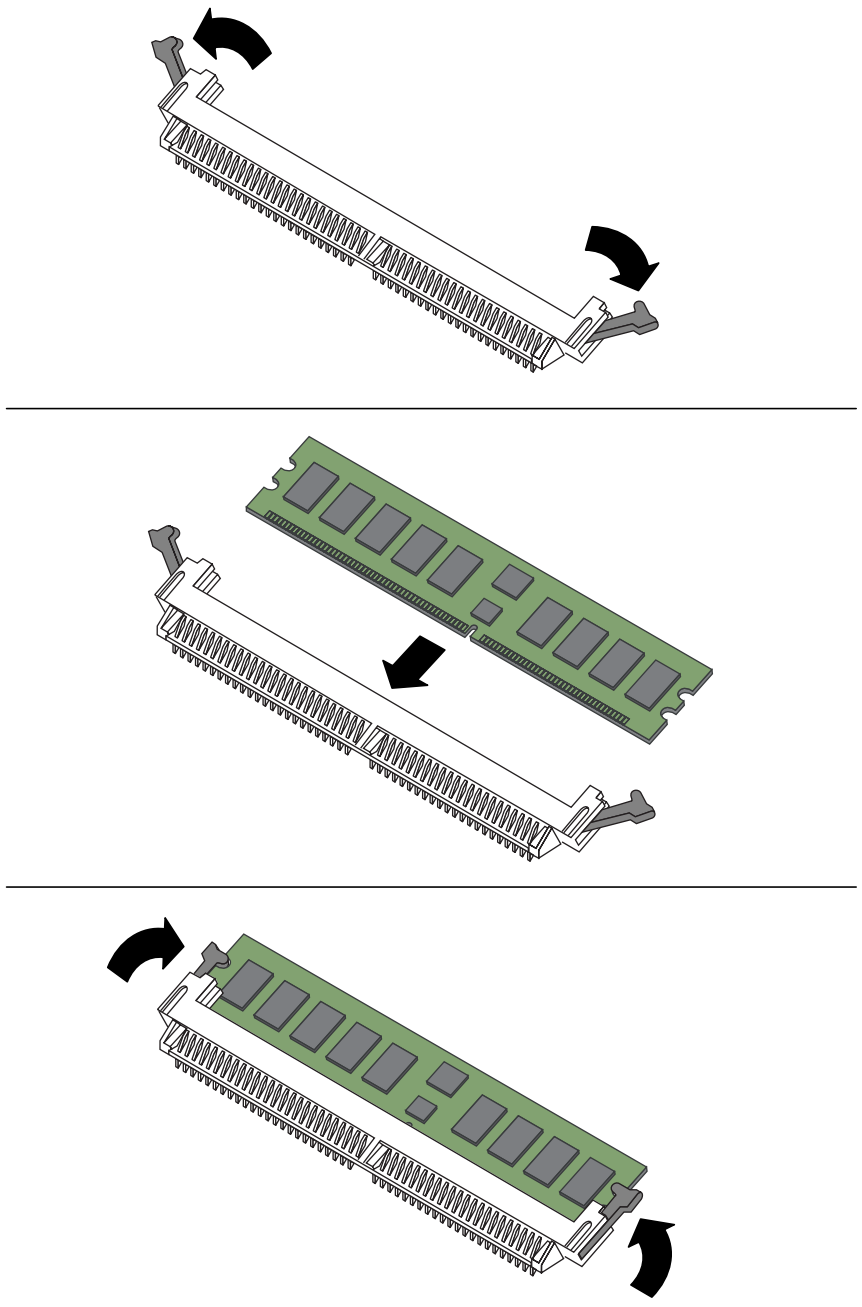

FIGURE 5-11 Installing a DIMM Into a Board Memory Connector

Caution – Evenly engage the DIMM in its slot at the 20-degree angle; uneven contact can cause shorts that will damage the Netra CP2500 board. Do not rock the DIMM into place. Ensure that all contacts engage at the same time. You feel or hear a click when the DIMM properly seats in the connector.

7. **Press the top edge of the DIMM toward the board until the retainer clips click into place (see FIGURE 5-11).**

   The small retainer clips on each side of the DIMM slot click into place in the notches on the DIMM sides.

8. **Repeat this procedure for the second DIMM memory module.**

Note – If you removed a PMC device prior to removing and replacing memory modules, see Section 2.5.1, "Installing an Optional PMC Device" on page 2-7 for the PMC device replacement procedure.

APPENDIX **A**

Specifications

Specifications for the Netra CP2500 board are provided in the following sections:

A.1 System Compatibility Specifications

The Netra CP2500 board is fully compatible with the Netra CT 410/810 servers. TABLE A-1 lists the attributes of a compatible cPSB chassis.

Property	Specification
H110 chassis compatible	CompactPCI J4 is unconnected at the board, which enables this board to be used in an H110 chassis
NEBS	NEBS Level 3 compliant chassis
I/O Voltage	Backplane power input (VIO) ***must*** be 5V.
CompactPCI compatibility	• PICMG 2.16 CompactPCI Packet Switched Backplane specification • PICMG 2.1 R1.0 Hot-Swap specification • PICMG 2.9 System Management specification

Caution – The backplane power input (VIO) ***must*** be 5V. Otherwise, the board and the chassis can become seriously damaged.

A.2 CPU Specifications

TABLE A-1 CPU Specifications

Property	Specification
CPU	UltraSPARC IIIi
Architecture	Sun 4U; 64-bit SPARC V9 architecture with the VIS instruction set
Cache	Integrated, 4 Mbyte, 4-way, set-associative internal L2 cache
PCI bus local interface	PCI Bus 2.1 compatible, 33 MHz, 32-bit, 3.3V (internal to board only)

A.3 PMC Interface Specifications

TABLE A-2 PMC Interface Specification

Property	Specification
PMC module interface on system board	One PMC interface
Interface IEEE P1386.1 compliance	With draft 2.1
Connector configuration, PMC A (P1386 designations)	Jn1, Jn2 carry PCI signals; Jn4 module I/O is connected to the CompactPCI J5 backplane connector
PCI clock	33 MHz
PCI bus width	32-bit
Max power load – per module, combined power rails (5V, 3.3V, 12V, -12V)	7.5 W (5V keyed or universal)

A.4 Power Requirements

This section provides information on power sequencing and power requirements by connection phase. TABLE A-3 shows the power drawn from the backplane connector by phase.

TABLE A-3 Netra CP2500 Backplane Connector Power Requirements by Connection Phase

Power Rail	No backplane power	Main power on medium pins (Typical configuration with two 1GB DIMMs installed)	Description
+5V	0	9 A	At CompactPCI connectors J1/J2
+3.3V	0	3 A	At CompactPCI connectors J1/J2
+12V	0	0.5 A	At CompactPCI connectors J1/J2
–12V	0	0	At CompactPCI connectors J1/J2
IPMB_PWR	0.25	0	At CompactPCI connector J1/A4

A.5 Mechanical Specifications

The Netra CP2500 board meets the mechanical specifications found in the CompactPCI specification PICMG 2.0 R3.0. FIGURE A-1 shows mechanical dimensions of the Netra CP2500 board panel, and FIGURE A-2 shows the mechanical dimensions of the board itself.

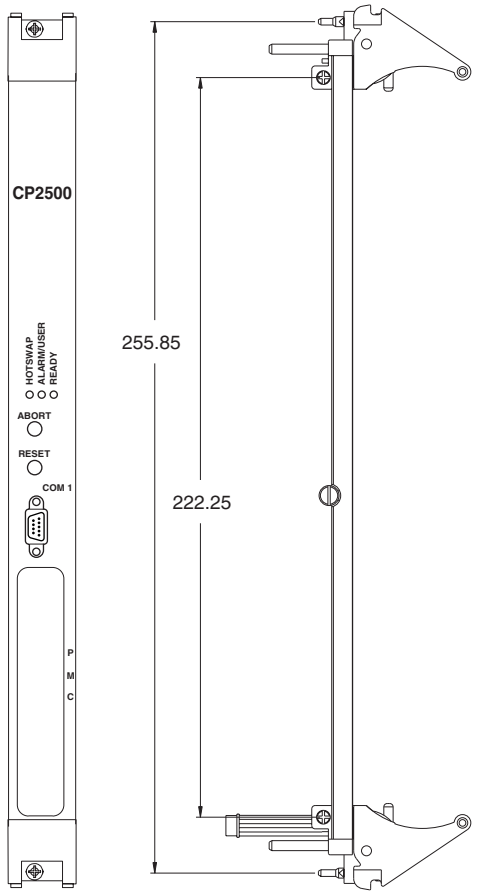

FIGURE A-1 Physical Dimensions of the Netra CP2500 Front Panel

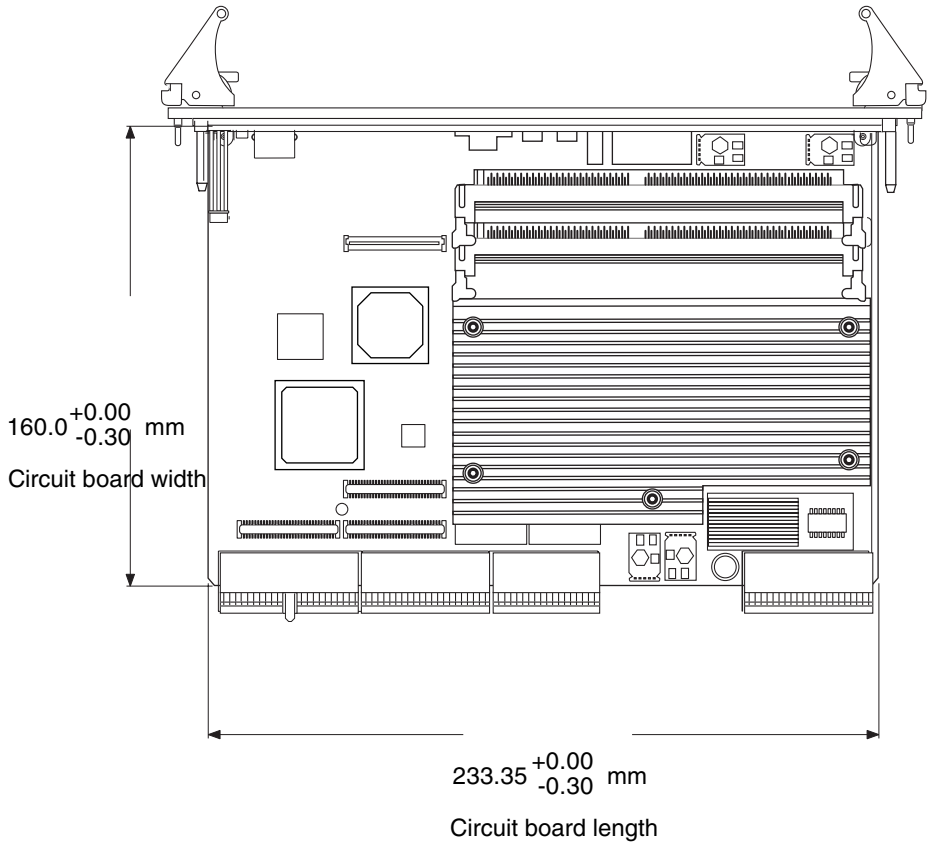

FIGURE A-2 Mechanical Dimensions of the Netra CP2500 Board

A.6 Environmental Specifications

TABLE A-4 Environmental Conditions and Limits

Ambient Conditions	Low Limit*	High Limit
Transportation and storage temperature	-40^0 C	+70^0 C
Transportation and storage humidity	5% RH\ noncondensing	95% RH noncondensing
Operating temperature	0^0 C (-5^0 C short term)	40^0 C (55^0 C short term)
Operating humidity	15% RH noncondensing	85% RH (90% RH short term) noncondensing
Shock and vibration	NEBS GR-63 CORE – Sections 4.3.1 and 4.3.2 for shock criteria and Section 4.4.3 for vibration criteria	
Electrostatic discharge	NEBS GR-1089 – Section 2	

* Short term, in this column, refers to a period of not more than 96 consecutive hours and a total of not more than 15 days in 1 year.

\ RH is relative humidity.

A.7 Cooling Requirements

The CPU diode temperature should not exceed 105^0 C when installed in the system. Refer to the *Netra CP2500 Board Programming Guide* (819-1749) for more information on thermal validation.

A.8 Reliability and Availability Specifications

Reliability, availability, and serviceability (RAS) specifications for the Netra CP2500 board are available through the Sun sales office under a nondisclosure agreement.

APPENDIX **B**

Connectors, Pinouts, and Switch Settings

This chapter contains the following sections:

Note – For pin assignments of the rear transition module connectors, refer to the *Netra CP2500 Rear Transition Module Installation and Technical Reference Manual* (819-1753).

B.1 PMC Connector

FIGURE B-1 and FIGURE B-2 show the location of PMC port connectors and pins. The following tables define contact allocations.

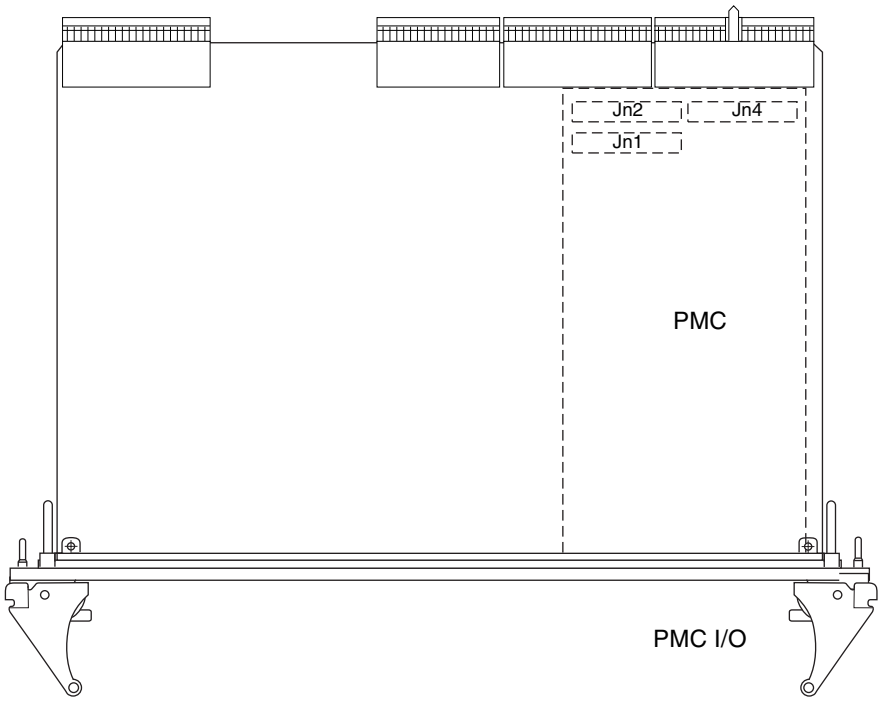

FIGURE B-1 Netra CP2500 Board PMC Port Connectors

Note – The P1386.1 standard reserves the Jn3 64-pin connector for PCI 64-bit extensions, so it is not fitted on the Netra CP2500 board.

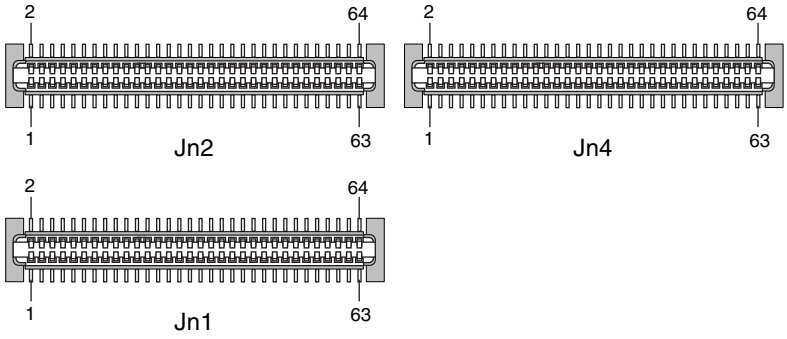

FIGURE B-2 PMC Connector Slot Connector Pins

B.1.1 PMC Connector Interfaces

Corresponding to the Common Mezzanine Card (CMC) specification, the PMC A slot is comprised of three PMC connectors – Jn1, Jn2, and Jn4. (The Jn3 connector is not fitted on the Netra CP2500 board.)

Note – Sun does not support installing a PIM device on either the RTM-S or the RTM-H.

The following tables list the PMC slot connector interfaces.

TABLE B-1 PMC Jn1 Connector Interface

Pin	Description	Pin	Description
1	Not connected	2	-12V
3	GND	4	PMC_A_INT_A_L
5	PMC_A_INT_B_L	6	PMC_A_INT_C_L
7	PMC_BUSMODE1_L*	8	VCC (5V)
9	PMC_A_INT_D_L	10	NC
11	GND	12	NC
13	PMC_CLK	14	GND
15	GND	16	PMC_GNT_L
17	PMC_REQ_L	18	VCC
19	LOCAL_VIO	20	PCI_B_AD<31>

TABLE B-1 PMC Jn1 Connector Interface *(Continued)*

Pin	Description	Pin	Description
21	PCI_B_AD<28>	22	PCI_B_AD<27>
23	PCI_B_AD<25>	24	GND
25	GND	26	PCI_B_CBE3_L
27	PCI_B_AD<22>	28	PCI_B_AD<21>
29	PCI_B_AD<19>	30	VCC
31	LOCAL_VIO	32	PCI_B_AD<17>
33	PCI_B_FRAME_L	34	GND
35	GND	36	PCI_B_IRDY_L
37	PCI_B_DEVSEL_L	38	VCC
39	GND	40	PCI_B_LOCK_L
41	PMC_SDONE	42	PMC_SB0_L
43	PCI_B_PAR	44	GND
45	LOCAL_VIO	46	PCI_B_AD<15>
47	PCI_B_AD<12>	48	PCI_B_AD<11>
49	PCI_B_AD<9>	50	VCC
51	GND	52	PCI_B_CBE_L<0>
53	PCI_B_AD<6>	54	PCI_B_AD<5>
55	PCI_B_AD<4>	56	GND
57	LOCAL_VIO	58	PCI_B_AD<3>
59	PCI_B_AD<2>	60	PCI_B_AD<1>
61	PCI_B_AD<0>	62	VCC
63	GND	64	PCI_B_REQ64_L

* BUSMODE signals require a pull-up.

TABLE B-2 PMC Jn2 Connector Interface

Pin	Description	Pin	Description
1	+12V	2	JTAG_PMC_RST_L
3	TMS	4	PMC_TDO
5	PMC_TDI	6	GND
7	GND	8	NC
9	NC	10	NC
11	PMC_BUSMODE2_L	12	VDD (3.3V)
13	PCI_B_RST_L	14	PMC_BUSMODE3_L
15	VDD	16	PMC_BUSMODE4_L
17	NC	18	GND
19	PCI_B_AD<30>	20	PCI_B_AD<29>
21	GND	22	PCI_B_AD<26>
23	PCI_B_AD<24>	24	VDD
25	PCI_B_IDSEL	26	PCI_B_AD<23>
27	VDD	28	PCI_B_AD<20>
29	PCI_B_AD<18>	30	GND
31	PCI_B_AD<16>	32	PCI_B_CBE_L<2>
33	GND	34	NC
35	PCI_B_TRDY_L	36	VDD
37	GND	38	PCI_B_STOP_L
39	PCI_B_PERR_L	40	GND
41	VDD	42	PCI_B_SERR_L
43	PCI_B_CBE_L<1>	44	GND
45	PCI_B_AD<14>	46	PCI_B_AD<13>
47	GND	48	PCI_B_AD<10>
49	PCI_B_AD<8>	50	VDD
51	PCI_B_AD<7>	52	NC
53	VDD	54	NC
55	NC	56	GND
57	NC	58	NC

TABLE B-2 PMC Jn2 Connector Interface *(Continued)*

Pin	Description	Pin	Description
59	GND	60	NC
61	PCI_B_ACK64_L	62	VDD
63	GND	64	NC

Note – The P1386.1 standard reserves the Jn3 64-pin connector for PCI 64-bit extensions. It is not fitted on these boards.

TABLE B-3 PMC Jn4 Connector Interface

Pin	Description	Pin	Description
1	Not connected	2	Not connected
3	Not connected	4	Not connected
5	Not connected	6	Not connected
7	Not connected	8	Not connected
9	Not connected	10	Not connected
11	Not connected	12	Not connected
13	Not connected	14	Not connected
15	Not connected	16	Not connected
17	Not connected	18	Not connected
19	Not connected	20	Not connected
21	Not connected	22	Not connected
23	Not connected	24	Not connected
25	Not connected	26	Not connected
27	Not connected	28	Not connected
29	Not connected	30	Not connected
31	Not connected	32	Not connected
33	PMC_A_IO_33	34	PMC_A_IO_34
35	PMC_A_IO_35	36	PMC_A_IO_36
37	PMC_A_IO_37	38	PMC_A_IO_38
39	PMC_A_IO_39	40	PMC_A_IO_40

TABLE B-3 PMC Jn4 Connector Interface *(Continued)*

Pin	Description	Pin	Description
41	PMC_A_IO_41	42	PMC_A_IO_42
43	PMC_A_IO_43	44	PMC_A_IO_44
45	PMC_A_IO_45	46	PMC_A_IO_46
47	PMC_A_IO_47	48	PMC_A_IO_48
49	Not connected	50	Not connected
51	Not connected	52	Not connected
53	Not connected	54	Not connected
55	Not connected	56	Not connected
57	Not connected	58	Not connected
59	Not connected	60	Not connected
61	Not connected	62	Not connected
63	Not connected	64	Not connected

B.2 Front Panel Serial Connector

This section contains the pin assignments for the front panel serial port connector.

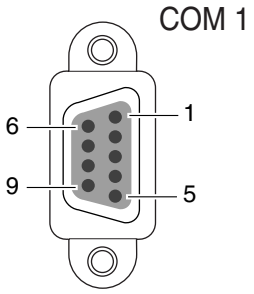

FIGURE B-3 Front Panel Serial Port Diagram

TABLE B-4 shows the serial port connector (TTYA) pin assignments.

TABLE B-4 Serial Micro DB9 Connector Pinouts

Pin	Signal Name	Pin	Signal Name
1	SER_DCD	6	SER_OSR
2	SER_RXD	7	SER_RTS
3	SER_TXD	8	SER_CTS
4	SER_DTR	9	SER_RI
5	SER_GND		

B.3 Backplane Connectors

FIGURE B-4 shows contact numbering as seen from the back of the Netra CP2500 board.

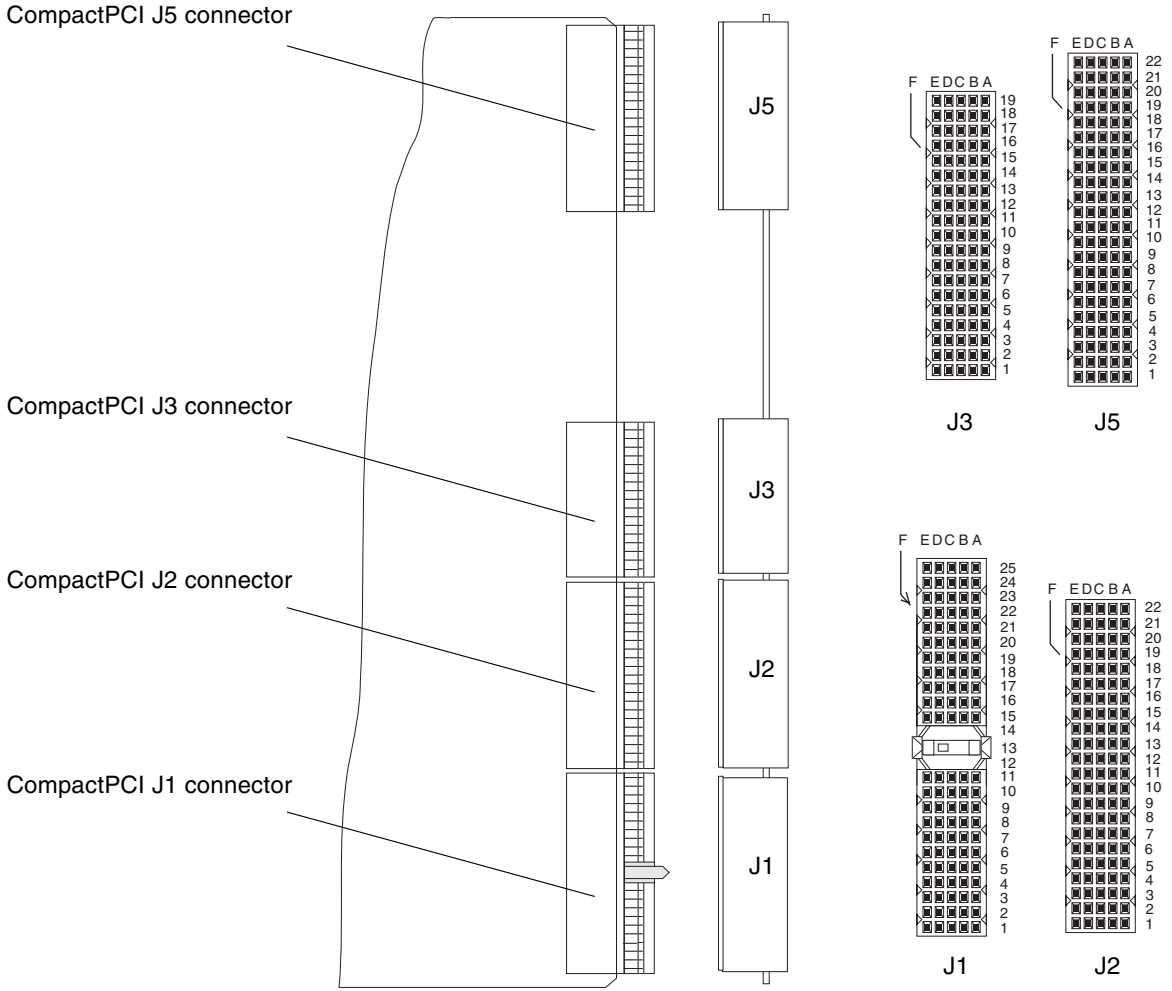

FIGURE B-4 Backplane Connector Contact Numbering

Note – The CompactPCI J4 connector is not populated on the Netra CP2500 board.

B.3.1 CompactPCI J1/P1 Connector Pinouts

TABLE B-5 lists the CompactPCI J1/P1 connector pin assignments.

TABLE B-5 CompactPCI J2/P2 Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
25	GND	+EP_5V	CPCI_REQ64#	CPCI_ENUM#	+EP_3.3V	+EP_5V	GND
24	GND	CPCI_AD[1]	+EP_5V	LP_VIO/unused	CPCI_AD[0]	CPCI_ACK64#	GND
23	GND	+EP_3.3V	CPCI_AD[4]	CPCI_AD[3]	LP_+EP_5V	CPCI_AD[2]	GND
22	GND	CPCI_AD[7]	GND	LP_+EP_3.3V	CPCI_AD[6]	CPCI_AD[5]	GND
21	GND	+EP_3.3V	CPCI_AD[9]	CPCI_AD[8]	m66en	CPCI_C/BE[0]#	GND
20	GND	CPCI_AD[12]	GND	VIO* (+EP_SV)	CPCI_AD[11]	CPCI_AD[10]	GND
19	GND	+EP_3.3V	CPCI_AD[15]	CPCI_AD[14]	LP_GND	CPCI_AD[13]	GND
18	GND	CPCI_SERR#	GND	+EP_3.3V	CPCI_PAR	CPCI_C/BE[1]#	GND
17	GND	+EP_3.3V	IPMB_SCL	IPMB_SDA	LP_GND	CPCI_PERR#	GND
16	GND	CPCI_DEVSL#	GND	VIO* (+EP_SV)	CPCI_STOP#	lock#	GND
15	GND	+EP_3.3V	CPCI_FRAME#	CPCI_IRDY#	CPCI_BD_SEL#	CPCI_TRDY#	GND
14	Key						Key
13	Key						Key
12	Key						Key
11	GND	CPCI_AD[18]	CPCI_AD[17]	CPCI_AD[16]	LP_GND	CPCI_C/BE[2]#	GND
10	GND	CPCI_AD[21]	GND	+EP_3.3V	CPCI_AD[20]	CPCI_AD[19]	GND
9	GND	CPCI_C/BE[3]#	CPCI_IDSEL	CPCI_AD[23]	LP_GND	CPCI_AD[22]	GND
8	GND	CPCI_AD[26]	GND	VIO* (+EP_SV)	CPCI_AD[25]	CPCI_AD[24]	GND
7	GND	CPCI_AD[30]	CPCI_AD[29]	CPCI_AD[28]	LP_GND	CPCI_AD[27]	GND
6	GND	CPCI_REQ0#	PCI_PRES#	LP_+EP_3.3V	CPCI_CLK0	CPCI_AD[31]	GND
5	GND	BRSVP	BRSVP	CPCI_RST#	LP_GND	CPCI_GNT0#	GND
4	GND	IPMB_PWR	HEALTHY#_out	LP_VIO/unused	intp	ints	GND
3	GND	CPCI_INTA#	CPCI_INTB#	CPCI_INTC#	LP_+EP_5V	CPCI_INTD#	GND
2	GND	tck	+EP_5V	tms	tdo	tdi	GND
1	GND	+EP_5V	-EP_12V	trst#	+EP_12V	+EP_5V	GND

* **Caution –** Backplane power (VIO) *must* be +EP_5V.

B.3.2 CompactPCI J1/P1 Signal Descriptions

Caution – Backplane power input (VIO) ***must*** be 5V.

TABLE B-6 CompactPCI J1/P1 Signal Descriptions

Signal Name	Description
+EP_5V	Backplane power input, EP_5V.
+EP_3.3V	Backplane power input, EP_3.3V.
+EP_12V	Backplane power input, EP_12V.
-EP_12V	Backplane power input, -EP_12V.
VIO	Backplane power input, which *must* be EP_5V.
LP_*	Long power pins. Refer to the PCIMG Hot Swap Spec R2.0, Section 4.2.1.
CPCI_RST#	cPCI reset.
CPCI_CLK[7..0]	cPCI clock. Provides timing for all cPCI transactions.
CPCI_AD[63..0]	cPCI bus Interface 64-bit multiplexed address and data.
CPCI_C/BE[7..0]#	cPCI bus command and byte enables; multiplexed on the same PCI signals.
CPCI_FRAME#	cPCI frame. Indicates the beginning of a PCI bus cycle.
CPCI_DEVSEL#	cPCI device select. Indicates PCI device response to selection.
CPCI_IRDY#	cPCI initiator ready. indicate bus master ability to complete the current data phase.
CPCI_TRDY#	cPCI target ready. Indicates target ability to complete the current data phase.
CPCI_STOP#	cPCI stop. Indicates initiator or target is requesting to stop the current transaction.
CPCI_IDSEL	cPCI initialization device select. Chip select during configuration read and write.
CPCI_REQ64#	cPCI request 64-bit transfer.
CPCI_ACK64#	cPCI Acknowledge 64-bit Transfer.
CPCI_PAR	cPCI parity bit. Calculated across AD[31..0] and C/BE[3..0].
CPCI_PERR#	Parity error.
CPCI_SERR#	cPCI system error.
CPCI_INT[A-D]	cPCI interrupts.
CPCI_REQ[7..0]#	cPCI request. Indicates to arbiter an agent desires use of the cPCI bus.
CPCI_GNT[7..0]#	cPCI grant. Indicates to agent access to the bus has been granted.
CPCI_BD_SEL#	PICMG 2.1 R1.0 hot-swap signal. Indicate board presence, SC drives to power on.
CPCI_ENUM#	PICMG 2.1 R1.0 hot-swap signal. Send or receive insertion or extraction event.

TABLE B-6 CompactPCI J1/P1 Signal Descriptions *(Continued)*

Signal Name	Description
HEALTHY#_out	PICMG 2.1 R1.0 hot-swap signal. Indicates health of the board, and signals to the SC that the board is suitable to be released from reset and enabled onto the bus.
IPMB_SCL	IPMI bus clock signal. Refer to the PCIMG 2.9 R1.0 cPCI System Management document.
IPMB_SDA	IPMI bus data signal. Refer to the PCIMG 2.9 R1.0 cPCI System Management document.
IPMB_PWR	Back-up power signal. Refer to the PCIMG 2.9 R1.0 cPCI System Management document.
PCI_PRES#	Indicates the backplane slot supports the cPCI interface.
m66en	66MHz cPCI bus speed enable; not supported.
lock#	cPCI Lock; not supported.
intp	Non-cPCI Interrupt; not supported.
ints	Non-cPCI Interrupt; not supported.
tck, tms, tdo, tdi	JTAG Signals; not supported, unconnected.
BRSVP	Backplane bused reserve pins, unconnected.

B.3.3 CompactPCI J2/P2 Connector Pinouts

TABLE B-7 lists the CompactPCI J2 connector pin assignments.

TABLE B-7 CompactPCI J2/P2 Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	CPCI_GA4	CPCI_GA3	CPCI_GA2	CPCI_GA1	CPCI_GA0	GND
21	GND	CPCI_CLK6	GND	RSV	RSV	rsv	GND
20	GND	CPCI_CLK5	GND	rsv	GND	rsv	GND
19	GND	GND	GND	rsv	rsv	rsv	GND
18	GND	BRSVP	BRSVP	BRSVP	GND	BRSVP	GND
17	GND	BRSVP	GND	BP_PB_RST#	CPCI_REQ6#	CPCI_GNT6#	GND
16	GND	BRSVP	BRSVP	DEG#	GND	BRSVP	GND
15	GND	BRSVP	GND	FAL#	CPCI_REQ5#	CPCI_GNT5#	GND
14	GND	CPCI_AD[35]	CPCI_AD[34]	CPCI_AD[33]	GND	CPCI_AD[32]	GND
13	GND	CPCI_AD[38]	GND	VIO/unused	CPCI_AD[37]	CPCI_AD[36]	GND
12	GND	CPCI_AD[42]	CPCI_AD[41]	CPCI_AD[40]	GND	CPCI_AD[39]	GND
11	GND	CPCI_AD[45]	GND	VIO/unused	CPCI_AD[44]	CPCI_AD[43]	GND
10	GND	CPCI_AD[49]	CPCI_AD[48]	CPCI_AD[47]	GND	CPCI_AD[46]	GND
9	GND	CPCI_AD[52]	GND	VIO* (+EP_5V)	CPCI_AD[51]	CPCI_AD[50]	GND
8	GND	CPCI_AD[56]	CPCI_AD[55]	CPCI_AD[54]	GND	CPCI_AD[53]	GND
7	GND	CPCI_AD[59]	GND	VIO* (+EP_5V)	CPCI_AD[58]	CPCI_AD[57]	GND
6	GND	CPCI_AD[63]	CPCI_AD[62]	CPCI_AD[61]	GND	CPCI_AD[60]	GND
5	GND	CPCI_C/BE[5]#	CPCI_64_EN#	VIO* (+EP_5V)	CPCI_C/BE[4]#	CPCI_PAR64	GND
4	GND	rsv	BRSVP	CPCI_C/BE[7]#	GND	CPCI_C/BE[6]#	GND
3	GND	CPCI_CLK4	GND	CPCI_GNT3#	CPCI_REQ4#	CPCI_GNT4#	GND
2	GND	CPCI_CLK2	CPCI_CLK3	CPCI_SYSEN#	CPCI_GNT2#	CPCI_REQ3#	GND
1	GND	CPCI_CLK1	GND	CPCI_REQ1#	CPCI_GNT1#	CPCI_REQ2#	GND

* **Caution –** Select VIO pins ***must*** be 5V, and *not* universal.

B.3.4 CompactPCI J2/P2 Signal Descriptions

Caution – Select VIO pins ***must*** be set to 5V, and *not* to universal.

TABLE B-8 CompactPCI J2/P2 Signal Descriptions

Signal Name	Description
CPCI_GA[4..0]	Geographical Address. Signals for unique slot identification.
BRSVP	Bused reserve pins.
PRST#	Backplane button reset input to SMC.
DEG#, FAL#	Power subsystem status signals input to SMC.
CPCI_64_EN#	PICMG hot-swap spec 2.1 R1.0 signal; designates 64-bit capability of backplane slot.
CPCI_PAR64	cPCI parity 64 bit; calculated across AD[63..32] and C/ BE[7..4]#.
CPCI_SYSEN#	System slot identification, grounded on the cPCI system slot.

B.3.5 CompactPCI J3/P3 Connector Pinouts

TABLE B-9 lists the CompactPCI J3 connector pin assignments.

TABLE B-9 CompactPCI J3/P3 Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
19	GND	RTM GND	RTM GND	RTM GND	RTM GND	RTM GND	GND
18	GND	PSB_A_TX_POS	PSB_A_TX_NEG	GND	GbE_A_TX_POS	GbE_A_TX_NEG	GND
17	GND	PSB_A_RX_POS	PSB_A_RX_NEG	GND	GbE_A_RX_POS	GbE_A_RX_NEG	GND
16	GND	PSB_B_TX_POS	PSB_B_TX_NEG	GND	GbE_B_TX_POS	GbE_B_TX_NEG	GND
15	GND	PSB_B_RX_POS	PSB_B_RX_NEG	GND	GbE_B_RX_POS	GbE_B_RX_NEG	GND
14	GND	RTM +3.3V	RTM +3.3V	RTM +3.3V	RTM +3.3V	RTM +3.3V	GND
13	GND	PCI A AD[31]	PCI A AD[30]	PCI A AD[29]	PCI A AD[28]	PCI A AD[27]	GND
12	GND	PCI A AD[26]	PCI A AD[25]	PCI A AD[24]	PCI A AD[23]	PCI A AD[22]	GND
11	GND	PCI A AD[21]	PCI A AD[20]	PCI A AD[19]	PCI A AD[18]	PCI A AD[17]	GND
10	GND	PCI A AD[16]	PCI A AD[15]	PCI A AD[14]	PCI A AD[13]	PCI A AD[12]	GND
9	GND	PCI A AD[11]	PCI A AD[10]	PCI A AD[9]	PCI A AD[8]	PCI A AD[7]	GND
8	GND	PCI A AD[6]	PCI A AD[5]	PCI A AD[4]	PCI A AD[3]	PCI A AD[2]	GND
7	GND	PCI A AD[1]	PCI A AD[0]	PCI A FRAM#	PCI A DVSL#	PCI A IRDY#	GND
6	GND	PCI A CBE0#	healthy_BP_RSV	PCI A CBE1#	PCI A TRDY#	PCI A STOP#	GND
5	GND	RTM SCA INT#	healthy_BP_RSV	RTM NTB INT#	PCI A PAR	PCI A CBE3#	GND
4	GND	RTM SCB INT#	healthy_BP_RSV	RTM NTA INT#	PCI A CBE2#	PCI A RTM CLKB	GND
3	GND	PCI A GNT 1#	healthy_BP_RSV	PCI A REQ1#	PCI A RST#	PCI A SERR#	GND
2	GND	PCI A GNT 2#	healthy_BP_RSV	PCI A REQ2#	SMC_3P3V	healthy_BP_RSV	GND
1	GND	Vdd 2.5V	healthy_BP_RSV	PCI A 66EN	PCI A RTM CLKA	PCI A PERR#	GND

B.3.6 CompactPCI J3/P3 Signal Descriptions

TABLE B-10 CompactPCI J3/P3 Signal Descriptions

Signal Name	Description
GbE/PSB_TX/RX_POS/NEG	PICMG 2.16 node board 10/100/1000 network signals.
32-bit PCI bus	32-bit PCI bus signaling and additional power pins to support SCSI controller on RTM-H. Optional.

B.3.7 CompactPCI J5/P5 Connector Pinouts

TABLE B-11 lists the CompactPCI J5 connector pin assignments.

TABLE B-11 CompactPCI J5/P5 Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	RSV	GND	No Connect	+5V	BP_XIR#	GND
21	GND	P1 LINKLED#	P1 ACTLED#	P2 LINKLED#	RTM I2C SCL	P2 ACTLED#	GND
20	GND	+5V	RSV	RSV	RTM I2C SDA	+12V	GND
19	GND	RSV	GND	VCC	SMC PWR	-12V	GND
18	GND	RSV	RSV	RSV	GND	+5V	GND
17	GND	RSV	RSV	RSV	RSV	RSV	GND
16	GND	RSV	RSV	RSV	RSV	RSV	GND
15	GND	RSV	RSV	RSV	RSV	RSV	GND
14	GND	RTSA	CTSA	RIA	GND	DTRA	GND
13	GND	DCDA	+5V	RXDA	DSRA	TXDA	GND
12	GND	RTSB	CTSB	RIB	+5V	DTRB	GND
11	GND	DCDB	GND	RXDB	DSRB	TXDB	GND
10	GND	PMC IO[36]	PMC IO[45]	PMC IO[47]	PMC IO[46]	PMC IO[48]	GND
9	GND	PMC IO[34]	PMC IO[41]	PMC IO[43]	PMC IO[42]	PMC IO[44]	GND
8	GND	PMC IO[35]	PMC IO[37]	PMC IO[39]	PMC IO[38]	PMC IO[40]	GND
7	GND	PMC IO[33]	RSV	RSV	RSV	RSV	GND
6	GND	RSV	GND	RSV	RSV	RSV	GND
5	GND	RSV	RSV	RSV	RSV	RSV	GND
4	GND	RSV	RSV	GND	RSV	RSV	GND
3	GND	RSV	RSV	RSV	RSV	RSV	GND
2	GND	RSV	RSV	RSV	RSV	RSV	GND
1	GND	RSV	RSV	RSV	RSV	RSV	GND

B.3.8 CompactPCI J5/P5 Signal Descriptions

TABLE B-12 lists the serial COM port (A and B) and RS232 level signal descriptions.

TABLE B-12 Serial COM Port and RS232 Level CompactPCI J5/P5 Signal Descriptions

Pin Signal	Description
CTS	Clear to send.
DCD	Data carrier detected.
DSR	Data set ready.
DTR	Data terminal ready.
RI	Ring indicator.
RTS	Request to send.
RXD	Serial receive data.
TXD	Serial transmit data.

FIGURE B-5 lists the miscellaneous signal descriptions.

TABLE B-13 Miscellaneous CompactPCI J5/P5 Signal Descriptions

Pin Signal	Description
BP_XIR_L	Button reset system input. Active low.

B.4 DIP Switch Settings

The Netra CP2500 board contains two DIP switches on one bank. The SW3301 DIP switch bank is located on the component side of the board between the front panel and heat sink (see FIGURE B-5). TABLE B-14 describes these switch settings.

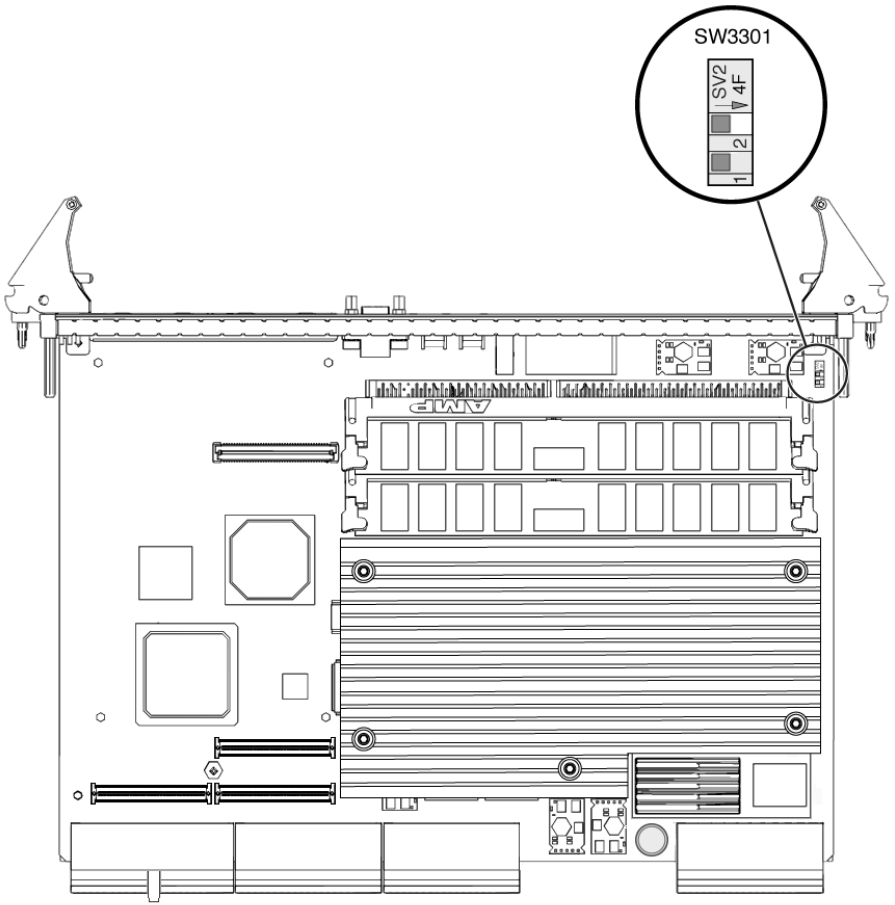

FIGURE B-5 SW3301 DIP Switch Location

Note – By default, the SW3301 DIP switches are both set in an *open* position, which means they are set in the opposite direction of the arrow. FIGURE B-5 shows the two switches in the default, open position.

TABLE B-14 SW3301 Switch Descriptions

Switch	Switch Setting	Description
1	Open	Boot the board from the main OpenBoot PROM image (default setting)
	Closed	Boot the board from the backup OpenBoot PROM image in the system flash (see FIGURE 4-2)
2	Open	Board is set to operate in a cPCI server (default setting)
	Closed	Board is set to operate in a cPSB chassis

Note – When switch 2 is set to the *closed* position (the cPSB chassis setting), the board's cPCI bridge will not be taken out of reset.

Note – The Netra CP2500 board is only supported in a Netra CT 410 server, Netra CT 810 server, or a third-party cPSB chassis. Sun does not support operating the Netra CP2500 board in a third-party cPCI server.

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