SPARCcenter 2000 System Board Manual

Sun Microsystems Computer Corporation
2550 Garcia Avenue
Mountain View, CA 94043
U.S.A.

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Preface

This manual is written for the trained service provider and contains service procedures for the Sun™ SPARCcenter™ 2000 and SPARCcenter™ 2000E system board.

When You Need Help with UNIX™ Commands

This manual does not include specific software commands or procedures. Refer to the operating system documentation when you need help with commands or procedures such as:

- Shutting down the system
- Booting the system
- Configuring devices
- Other software procedures

Depending on the operating system you are using, complete descriptions of commands and procedures can be found in:

- On-line AnswerBook™ documentation that comes with Solaris
- Other software documentation you received with your system

What Typographical Changes and Symbols Mean

Table P-1 describes the type changes and symbols used in this book.

Table P-1 Typographic Conventions

Typeface or Symbol	Meaning	Example
AaBbCc123	The names of commands, files, and directories; on-screen computer output	Edit your `.login` file. Use `ls -a` to list all files. system% You have mail.
AaBbCc123	What you type, contrasted with on-screen computer output	`system% su` `Password:`
AaBbCc123	Command-line placeholder: replace with a real name or value	To delete a file, type `rm` *filename*.
AaBbCc123	Book titles, new words or terms, or words to be emphasized	Read Chapter 6 in *User's Guide*. These are called *class* options. You *must* be root to do this.
Code samples are included in boxes and may display the following:		
%	UNIX C shell prompt	system%
$	UNIX Bourne and Korn shell prompt	system$
#	Superuser prompt, all shells	system#

Related Documentation

These documents contain reference information related to system board installation and testing.

Table P-2 Related Documents

Application	Name	Part Number
Safety	*Data Center Regulatory Compliance*	801-3051
Installation	*Deskside/Data Center SBus Install*	800-6366
	Memory Module Installation Guide	801-2030
	SuperSPARC Module Installation Guide	801-2035
Diagnostics	*SPARCcenter 2000 Post User's Guide*	800-7481
	Open Boot Command Reference	800-6076

Table P-2 Related Documents *(Continued)*

Application	Name	Part Number
User's Guides	*Writing FCODE Programs for SBus Cards*	800-5673
	System and Network Administration for the Sun Workstation	800-1323
Service	*SPARCcenter 2000 Service Manual*	800-2007

Notes, Cautions, and Warnings

Warning – The SuperSPARC module has a *hot surface.* Avoid contact. Surfaces are hot and may cause personal injury if touched.

Warning – This equipment contains lethal voltage. Accidental contact can result in serious injury or death.

Caution – Improper handling by unqualified personnel can cause serious damage to this equipment. Unqualified personnel who tamper with this equipment may be held liable for any resultant damage to the equipment.

Individuals who remove any outer panels or open covers to access this equipment must observe all safety precautions and ensure compliance with skill level requirements, certification, and all applicable local and national laws.

Procedures contained in this document must be performed by qualified service-trained maintenance providers.

Note – Before you begin, carefully read each of the procedures in this manual. If you have not performed similar operations on comparable equipment, *do not attempt* to perform these procedures.

Preparing for Installation or Service 1

This chapter discusses:

- Tools
- Safety precautions
- System boards
- Replacement parts

1.1 Required Tools

- Antistatic mat
- Grounding strap
- #1 Phillips screwdriver
- IC extraction tool

1.2 Safety Precautions

Caution – When working on the system board, use an antistatic mat which has at least 0.25" (6 mm) of cushioning. This cushioning will protect underside components and prevent harmful board flexing.

Caution – When the system power is turned off, the AC power cord must remain plugged in to ensure a proper ground.

Protect yourself and the equipment by observing the following precautions.

Table 1-1 Safety Precautions

Item	Problem	Precaution
Ac power cord	ESD (Electrostatic discharge)	The power cord provides a ground path for the cabinet. Do not unplug the cord, even if the power is turned off.
	Electric shock	Turn the cabinet circuit breaker OFF before opening the cabinet for service.
ESD mat & wrist or foot strap	ESD	Use a cushioned, antistatic mat and a grounding strap for these procedures.
System boards	ESD	Handle a system board by the edges only.Store boards in antistatic bags.
	Breakage	Parts on a board may break if the board is flexed. Keep the board vertical when out of the card cage. Place the board on a *cushioned* mat for service.
Springfingers	Personal injury	Springfingers have sharp edges, so handle springfinger-equipped screens and boards carefully.
	RFI leakage	The screens and panels used on the cabinet suppress radio frequency interference (RFI) and are required by law in many localities.
	Damaged springfingers	Replace any screen or board having broken or twisted springfingers with a new assembly.
Cover panels	System damage and overheating	Install all cover panels to keep out foreign objects and prevent overheating.
Filler panels	System damage and overheating	Install filler panels in all unused card cage slots. Open slots severely reduce the cooling capability of the system.

1.3 System Board Description

Figure 1-1 identifies the major components on the system board.

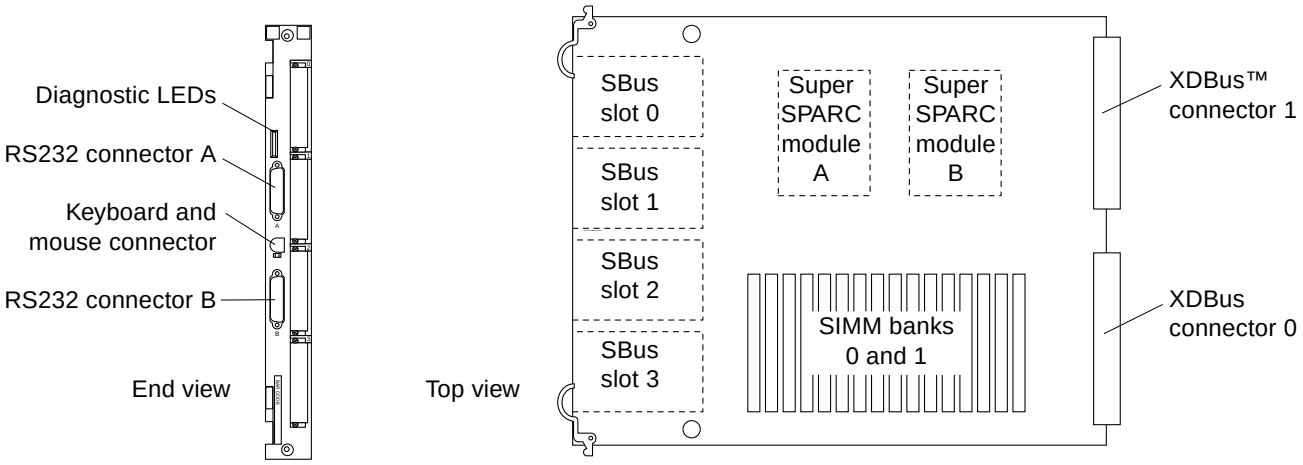

Figure 1-1 End and Side Views of the System Board

All system boards are basically the same. No jumper changes are necessary. A board can be moved to any slot in the card cage for troubleshooting.

However, the system architecture requires that one system board serve as the system master (being a major part of the bus arbitration system.) Also (in most cases), the OBP master is found on the system master board.

1.3.1 System Master Board

To determine which board is system master and for a list of system master requirements, Refer to Section D.1, “System Master Board.”

1.4 Replacement Parts

Table 1-2 lists part numbers for replacements. Replaceable parts are shown with dotted outlines in Figure 1-2, which shows their relative locations on the board. These items include SuperSPARC modules, SIMMs, SBus cards, the OpenBoot PROM and the system board itself.

System error messages may specify non-replaceable components by part name, but these components cannot be replaced in the field. If any non-replaceable component fails, replace system board.

Table 1-2 Replacement Part Numbers

Part	Part Number
SPARCcenter 2000 System board, 0 processors, 0 SIMMs	501-1866-xx
SPARCcenter 2000E System board, 0 processors, 0 SIMMs	501-2718-xx
SuperSPARC module	*
OpenBoot PROM	*
TOD / NVRAM	100-3528-xx
8 Mbyte SIMM (8Mx9 bits, 100ns): May be marked:MH1M72A,MH1M72BJ-8,ZA3080 (etch) or Z124SUN72	501-1817-xx
32 Mbyte SIMM (32Mx9 bits, 100ns): May be marked MH4M72J-8, Za3085 (in etch), or Z496SUN72	501-2196-xx
NVSIMM, 1Mx9 bits: The SIMM may be marked MH12872SN-70H	501-2197-xx
Filler panel, SBus slot cutout (Note: screw size is M2.5 for SBus cards)	340-2305-xx
Filler panel, card cage board slot	540-2114-xx

*-See your Sun representative for latest part number.

xx -Denotes revision level of an assembly; the factory ships the applicable revision level.

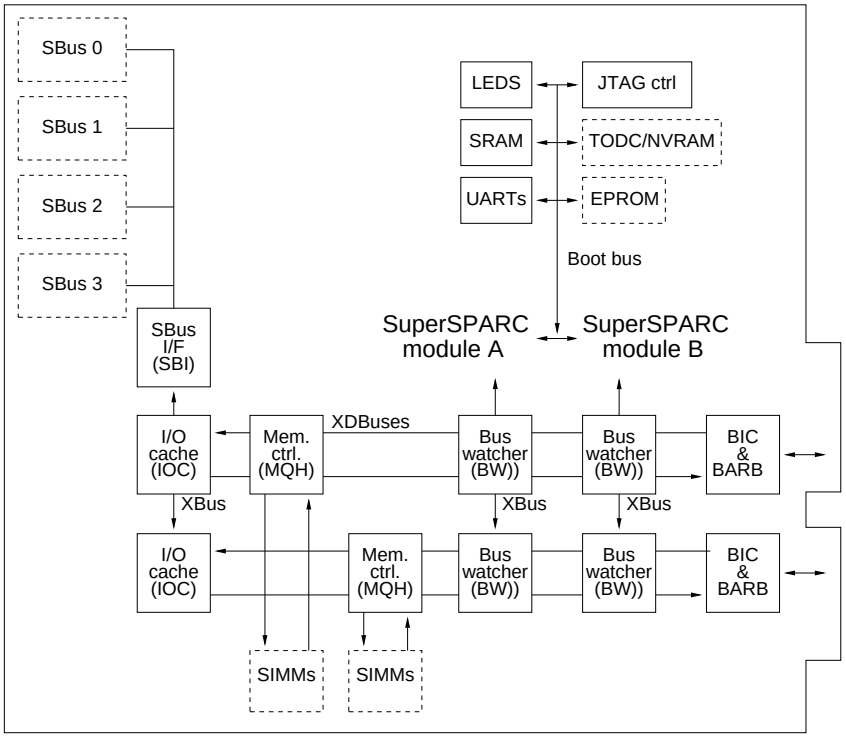

Figure 1-2 Replacement Part Locations

Removing and Replacing System Boards and Assemblies 2

This chapter provides the information on removing or replacing:

- System boards
- SuperSPARC modules
- SBus cards
- SIMMs and NVSIMMs
- OpenBoot PROMs
- TOD / NVRAM

2.1 Halting the System

To halt the system safely:

1. **Back up the system files and data, if necessary.**
2. **Halt the system using the appropriate commands.**
3. **Wait for the system-halted message and the boot monitor prompt.**
4. **Turn the key switch (on the front panel) to the Standby position.**
5. **Turn the AC power switch on the system back panel off.**

Caution – The system chassis power must be turned off, and the AC power cord must remain plugged in to ensure a proper ground.

2.2 Removing a System Board

Caution – Use a *cushioned* ESD mat for these procedures. There are breakable parts on the bottom of the system board.

1. **Take off the rear screen by removing two Phillips screws (seeFigure 2-1).** Grasp the rear screen carefully, the springfingers on the inner side of the rear screen have sharp edges.

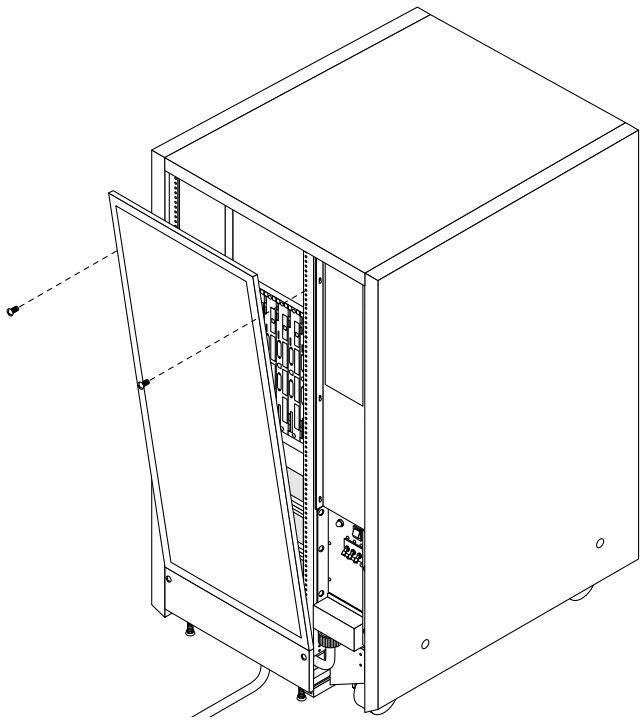

Figure 2-1 Rear Screen

2. **Disconnect and set aside any cables connected to the board backpanel.** Label the cables for ease of reconnection later.

3. **Remove the two screws that secure the board to the card cage.**

4. **Simultaneously, pull the curved ends of both ejector/injector levers outward to release the board from the backplane connectors.**
   Refer to Figure 2-2.
5. **Holding the board by both ejector/injector levers, gently slide the board out of the card cage.**
6. **Place the board on a cushioned ESD mat or in an antistatic bag.**

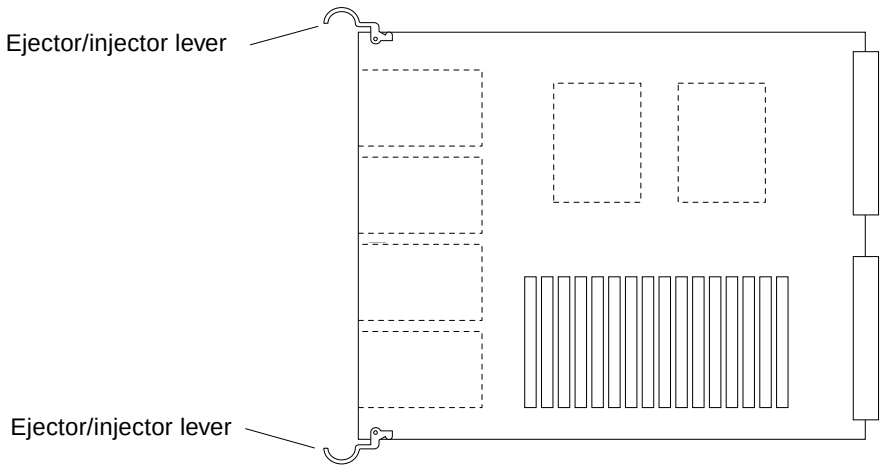

Figure 2-2 System Board Ejector/injector Levers in the Unlocked Position

2.3 Using Standoffs

Standoffs support and secure the SuperSPARC modules and SBus cards to the system board.

- To unlock a standoff, pull up the tip. Refer to Figure 2-3.
- To lock a standoff, first ensure that the module or card rests on the standoff flange, then press down the tip.

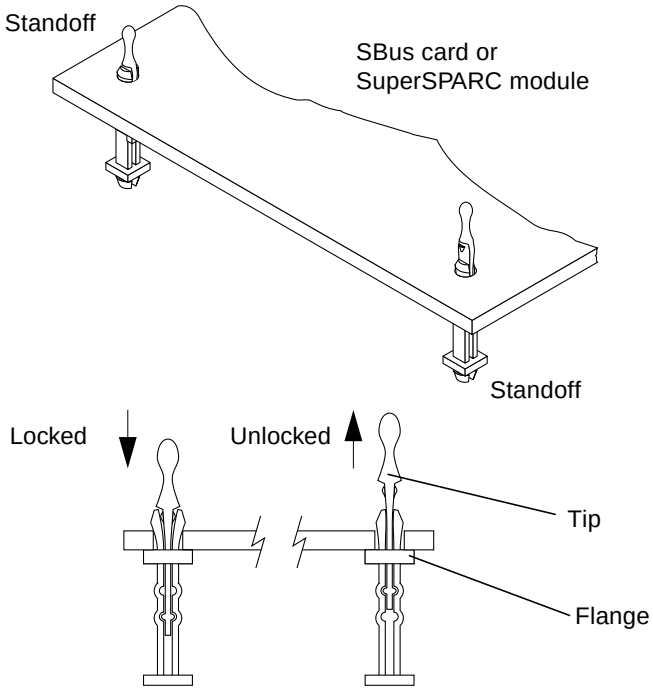

Figure 2-3 Locking and Unlocking Standoffs

2.4 SuperSPARC Modules

The system board can have zero, one, or two modules. Refer to Figure 2-4.

If you are adding SuperSPARC modules to a system, fill all A slots first, before filling the B slots. Start with the lowest-numbered system boards.

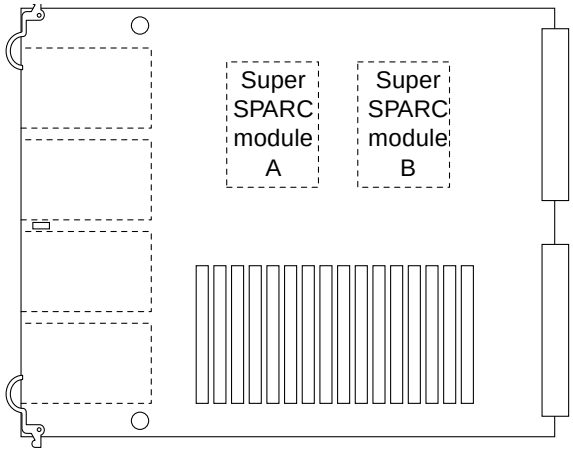

Figure 2-4 SuperSPARC Modules A and B

2.4.1 Removal

Warning – The heatsinks on the SuperSPARC modules may be hot. Use caution when removing or installing SuperSPARC modules and avoid contact with the heatsinks. Hold SuperSPARC modules only by the edges.

1. **Unlock the four standoffs that secure the module to the system board.** Pull up the tip of a standoff to unlock it. Refer to Figure 2-3.
2. **Hold the module by the edges near the connector and carefully rock the module back and forth to loosen the connector from the socket.**

Caution – The connector housing may break if the module is tilted too far.

3. **Place the module in an antistatic bag.**

2.4.2 Installation or Replacement

1. **Unlock the four standoffs for this slot if they are not already unlocked.** Pull up the tip of a standoff to unlock it, as shown in Figure 2-3.
2. **Take the SuperSPARC module out of the protective packaging, and inspect the connector for bent pins.**

3. **Rest the module lightly on the four standoffs and align the module connector with the system board socket.**
4. **Hold the module by the edges near the connector and firmly but gently press the module straight down until the connector is fully seated.** Do *not* press with a rocking motion; the plastic connector housing may break.
5. **Starting from the side opposite from the connector, press each corner of the module until the corner is seated on the flange of each standoff.**
6. **Press down on the tip of each standoff to lock the module in place.**

2.5 SBus Cards

Figure 2-5 shows the SBus slots on a board.

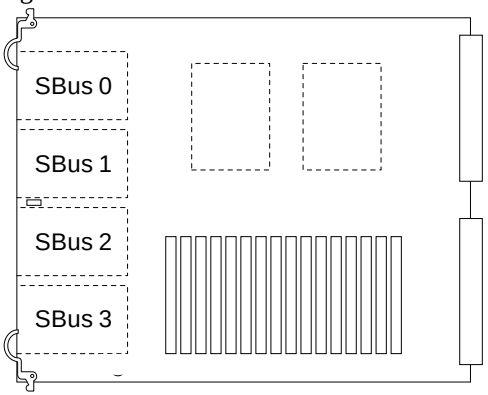

Figure 2-5 SBus Slot Locations

For help in selecting a location for a new SBus card, see Section D.4, “Selecting an SBus Module Location.”

2.5.1 Removal

1. **Remove the two screws that secure the SBus card to the back panel.**
2. **Unlock the SBus card by pulling up the tips of the two standoffs, as was shown in Figure 2-3.**

3. **Hold the card by the edges nearest to the connector, and gently rock the card back and forth to loosen it from the socket.**

Caution – The connector housing will break if the card is tilted too far.

4. **Lift the card at an angle while guiding the face plate out of the back panel opening and under the springfingers. Refer to Figure 2-6.**

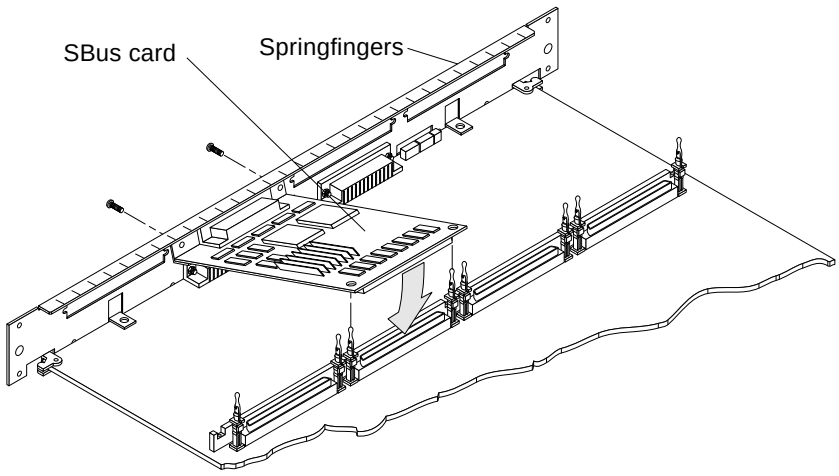

Figure 2-6 Removing or Installing an SBus Card

5. **Place the SBus card in an antistatic bag.**

6. **If a replacement card is not available, install a filler panel (P/N 340-2305) on the back panel opening of the system board. Secure the panel with the screws that were removed in step 1.**

Caution – Ensure the panel is right-side up. If the filler panel is installed upside down, a gap will be created, impairing system cooling.

2.5.2 Replacement

2.5.2.1 Preparing a New SBus Card

1. **Remove the black plastic card retainer shipped with the card.**
   Refer to Figure 2-7. Spread the ends of the retainer apart to remove it from the card. The retainer is not needed for this installation.

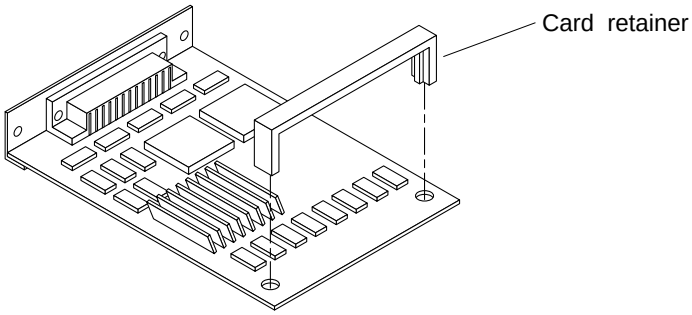

Figure 2-7 SBus Card Retainer

2. **Remove the adapter bracket from the SBus card rear panel.**
   Refer to Figure 2-8. Using a #0 Phillips screwdriver, remove two screws securing the adapter to the card rear panel. The adapter bracket and screws are not needed for this installation.

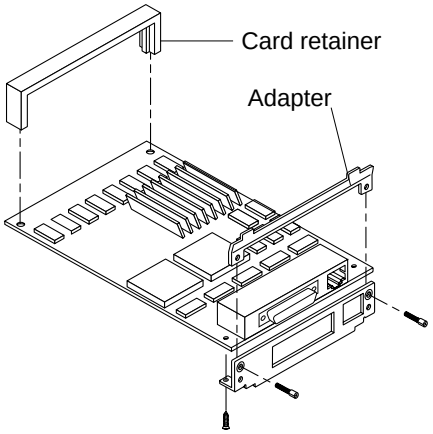

Figure 2-8 SBus Card Rear Panel with Adapter

3. **For DSBE/S and FSBE/S cards: remove the two outer retaining screws (refer to Figure 2-9), but do NOT remove the middle screw or the springfinger.**
   Use a #0 Phillips screwdriver and a 3/16 nut driver or socket wrench.

4. **For DSBE/S and FSBE/S cards, configure jumper J0302 for link integrity test functionality. Refer to**
   DSBE/S — Figure 2-9:

   FSBE/S — Figure 2-10

   a. **Put the shunt over both pins to** *disable* **the Link Integrity Test, as shown in Figure 2-11 “Disabled.”.**

   b. **Put the shunt in one pin to** *enable* **the Link Integrity Test, as shown in Figure 2-11 “Enabled.”.**

Caution – If the customer chooses to disable the test, it must be disabled both at the hub and at the SBus card. In the event of “loss of carrier” or “not responding” problems, check the status of the link enable on both the SBus card and the hub.

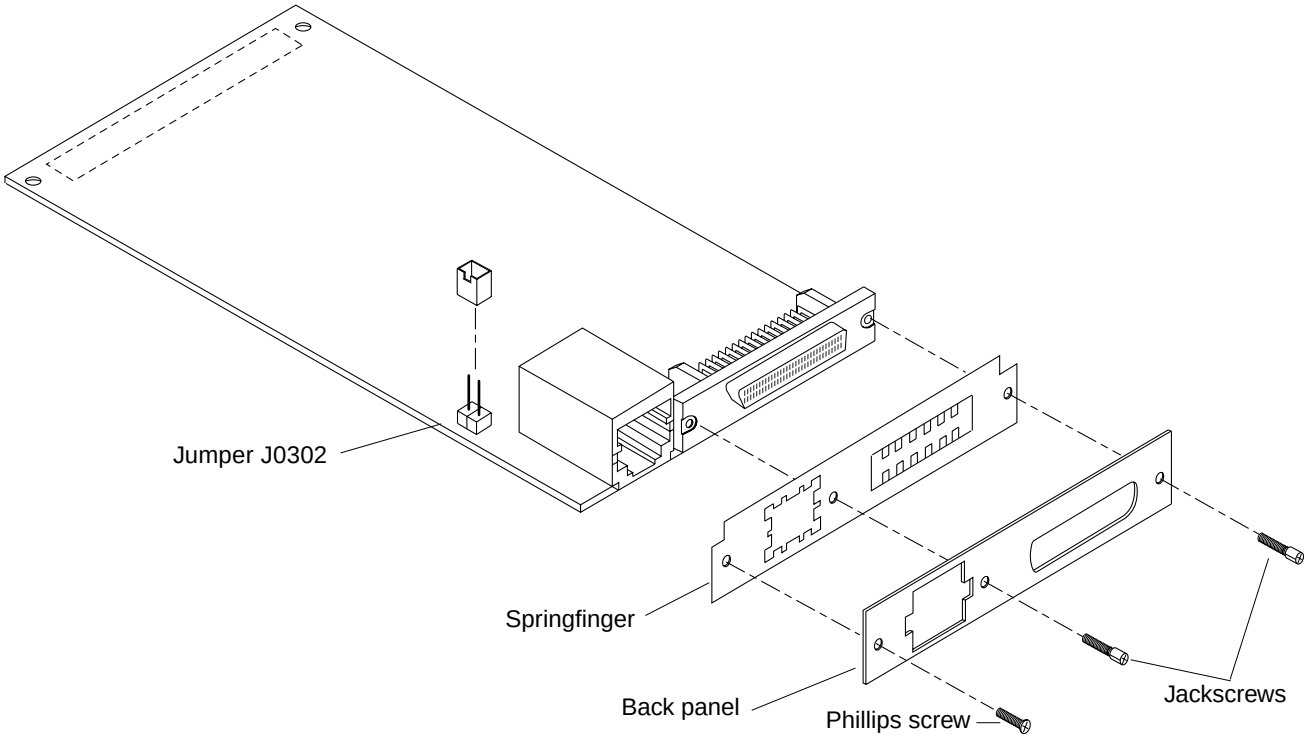

Figure 2-9 DSBE/S SBus Card

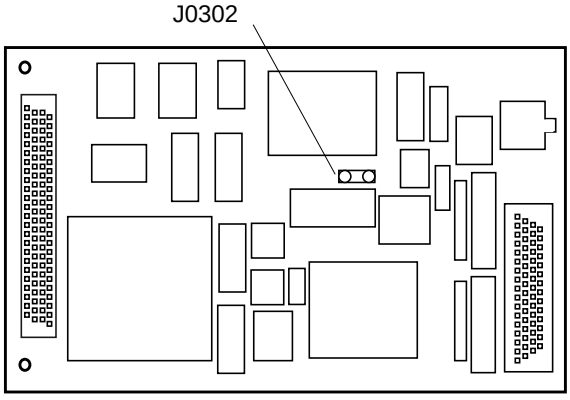

Figure 2-10 FSBE/S SBus Card

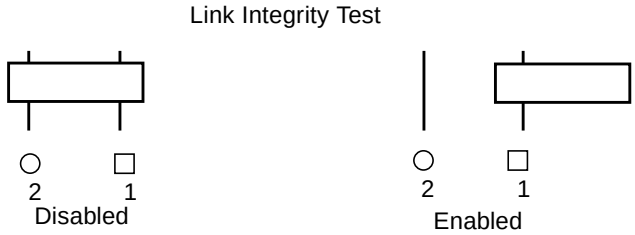

Figure 2-11 Disabling and Enabling the Link Integrity Test

2.5.2.2 Installation

1. **Remove the filler panel (if any) covering the SBus slot opening.**
   Retain the screws to attach the SBus card to the back panel, unless the card has a wide connector or connectors. See the SBus card installation manual to verify the specific connector type.

2. **Unlock the two standoffs for the slot.**
   Pull up the tip of a standoff to unlock it, as shown in Figure 2-3.

3. **Take the SBus card out of the protective packaging and inspect the SBus connector for damaged pins.**

4. **Guide the SBus card face plate under the springfingers and against the rear face of the back panel.**
   Refer back to Figure 2-6. The I/O connectors of the card should be visible through opening in the back panel.

5. **Hold the card by the edges nearest the SBus connector and rest the card lightly on the two standoffs.**

6. **Firmly but gently press the card straight down until the connector is fully seated. At the same time, align the connector and socket, pushing the card toward the system board back panel.**

Caution – Do not rock the card onto the socket; the SBus connector housing may break.

7. **Press down on each corner of the card to ensure that the corner rests fully on the flange of the standoff.**

8. **Press down on the tip of each standoff to lock the card in place.**

2.6 SIMMs and NVSIMMs

These devices were designed for the SPARCcenter 2000 and are not interchangeable with other types of SIMMs.

Do not mix SIMMS of different capacities.

Note – The 8 Mbyte and 32 Mbyte SIMMs may be almost identical when made by the same manufacturer, so do not rely on physical appearances. To verify the suitability of a replacement module, refer to Table 2-1 and Figure 2-12.

Table 2-1 SIMM Variations

Capacity	Type	Markings	Part Number	Outline in Figure 2-12
8 Mbyte	20-pin DRAMs	The SIMM may be variously marked MH1M72A, MH1M72BJ-8, ZA3080 (in etch), or Z124SUN72	501-1817	A or B
32 Mbyte	24-pin DRAMs	The SIMM may be variously marked MH4M72J-8, Za3085 (in etch), or Z496SUN72	501-2196	A or B
1Mbyte	Battery-backed NVSIMM	The NVSIMM may be marked MH12872SN-70H	501-2197	C

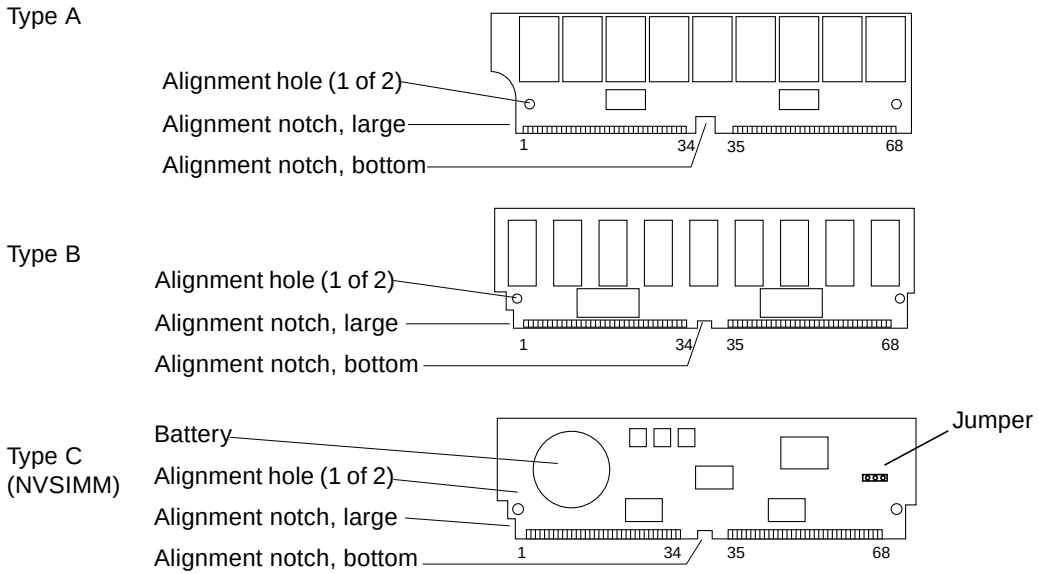

Figure 2-12 SIMM Types

2.6.1 Removal

If a SIMM or NVSIMM fails, the power-on self test (POST) will identify the location number (also known as the U-number or J-number) of the failing device. The socket number (J-number) is printed on the back of the board.

When replacing faulty SIMMs, refer to the location-numbers listed below.

1. **Locate a faulty SIMM by matching the location number noted in the POST message.**
2. **Orient the system board so that the XDBus™ connectors face you.**
3. **Unlock the SIMM by pressing the locking tabs toward the sides of the socket and then tilting the SIMM forward, as shown in Figure 2-14.**
4. **For most SIMM sockets, there is very little space for movement, so unlock two more SIMMs in front of the first SIMM, as shown in Figure 2-15.** This allows the faulty SIMM to tilt forward far enough to disengage the locking pins.
5. **Remove the SIMM from the socket and place it in an antistatic bag.**

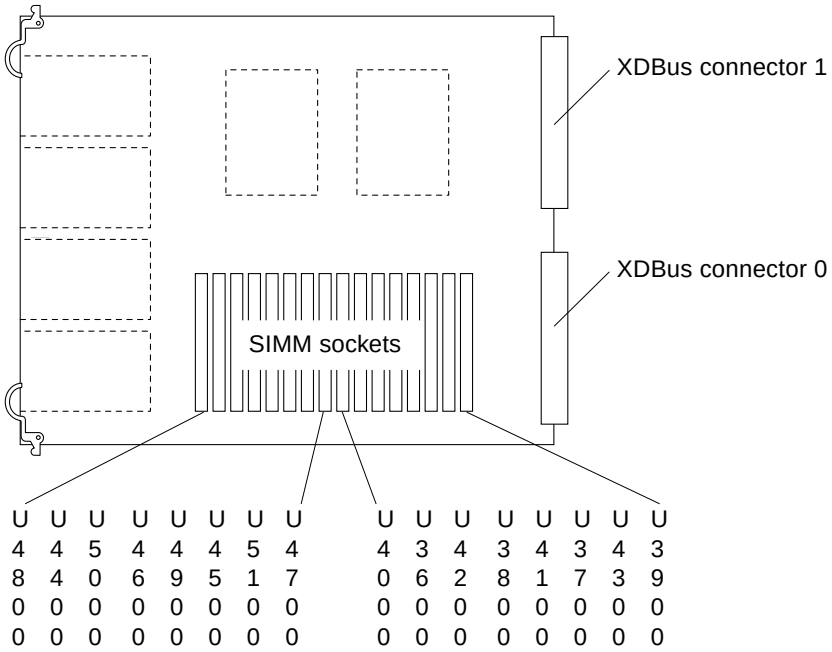

Figure 2-13 SIMM Location Numbers

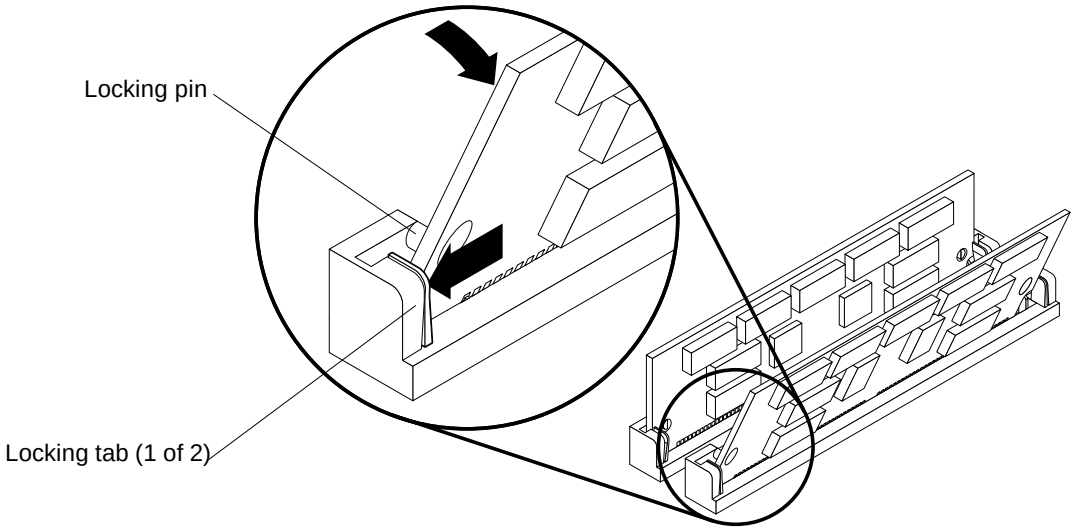

Figure 2-14 Unlocking a SIMM

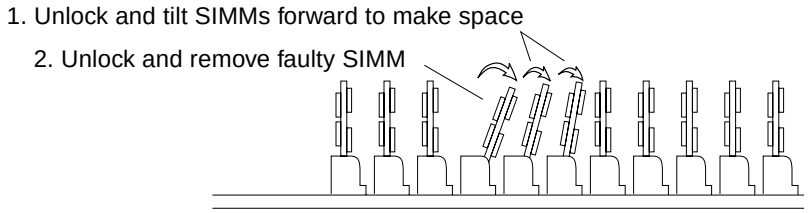

Figure 2-15 Creating Space to Remove a SIMM

2.6.2 Installation

Note – Do not mix SIMMs of different capacities.

Caution – If you are adding memory to a system (always in multiples of 8 SIMMs), see Section D.5, “Selecting SIMM or NVSIMM Locations” and Section D.6, “SIMM or NVSIMM Installation Rules” before proceeding.

1. **Orient the system board so that the XDBus connectors face you.**
2. **Remove the SIMM (or NVSIMM) from the antistatic package.**
3. **For NVSIMM only: if the battery is not already activated, move the jumper to the ON position, as shown in Figure 2-16. If the jumper is already in the On position, do not move it.**

Caution – Never move the jumper after the battery has been turned on, or data contained in the NVSIMM will be lost.

Note – It is not necessary to move jumpers on NVSIMMs that have been factory-installed in a new system. The system is delivered with the NVSIMM batteries activated.

4. **Hold the SIMM at the edges, with pin 1 to your left.**
   The large alignment notch or double notch (Figure 2-12) is at the left side.

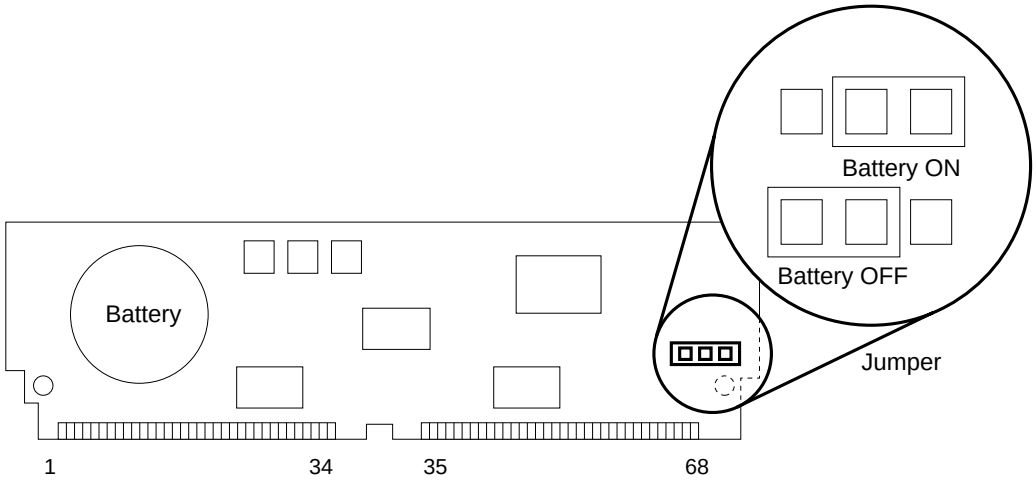

Figure 2-16 NVSIMM Jumper Locations

5. **Guide the SIMM into the slot so that the SIMM connector pads touch the bottom of the socket.**
   The bottom alignment notch on the SIMM must align with the tab in the center of the socket. The locking pins (refer to Figure 2-14) must align with the holes in the sides of the SIMM.

6. **Tilt the SIMM upright to lock it in place.**
   The locking tabs should automatically lock around the SIMM.

Note – The SIMM should require very little insertion force. If there are difficulties, or if the SIMM does not resemble the original SIMM, the replacement SIMM may be backward; check again that the alignment holes and the alignment notch align *exactly* with corresponding parts of the SIMM socket.

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7. **Lock back into place any SIMMs that were loosened in the SIMM removal steps.**

2.7 OpenBoot PROMs

Refer to Figure 2-17 for the PROM socket locations.

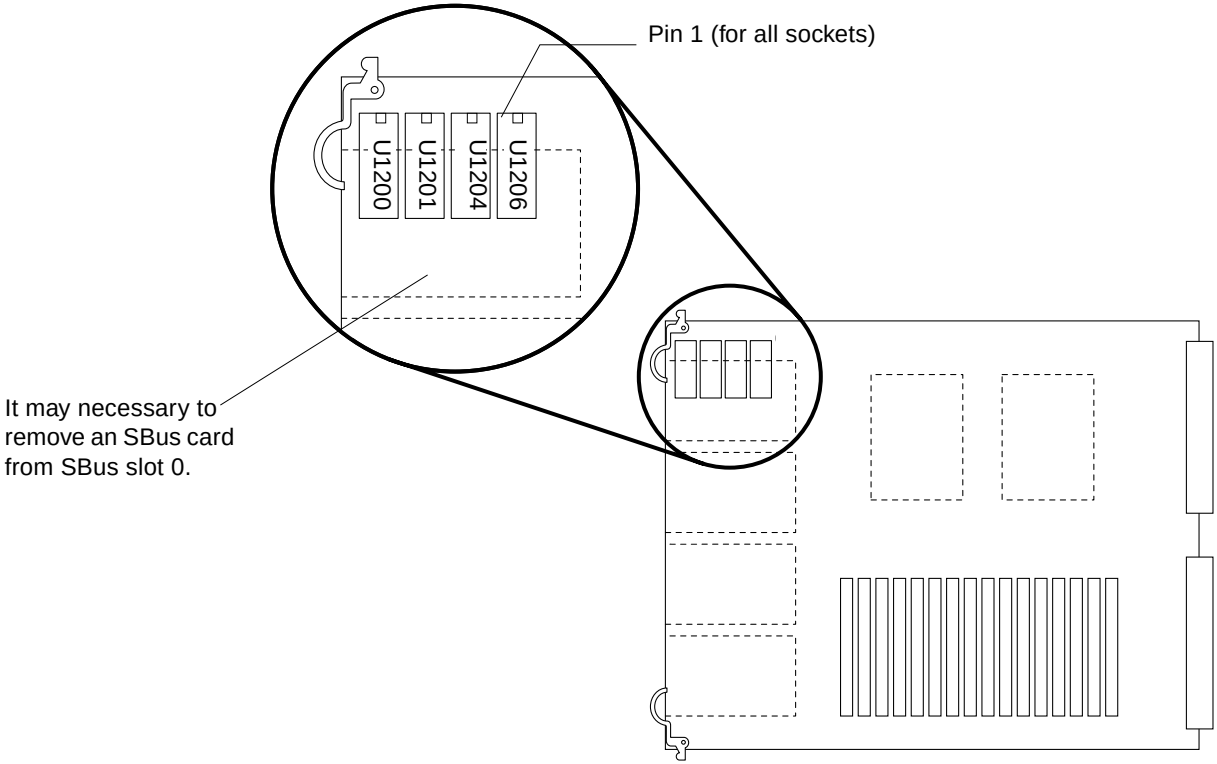


Figure 2-17 Open Boot PROM Locations

2.7.1 Removal

1. **To access the PROMs, remove the SBus card (if any) in SBus slot 0.**
2. **Use an IC extraction tool to remove the PROMs.**
3. **Place PROMs on antistatic foam plastic and store in an antistatic package.**

2.7.2 Replacement

1. **Verify the correct PROM location.**
   Correlate the part number on each PROM to the corresponding U-number as shown in Figure 2-17.

2. **Position the PROM carefully on the socket, and partially seat the PROM.** Orient the divice pin1 correctly as shown in Figure 2-17.

3. **Check for bent pins, then press firmly to seat the PROM in the socket.**

Caution – Use a cushioned ESD mat to prevent breakage of parts on the underside of the board.

4. **Install the remaining PROMs in the same manner.**

5. **Install any SBus card that was removed for this procedure.**

2.8 TOD/NVRAM

Refer to Figure 2-18 for the location of the TOD / NVRAM IC.

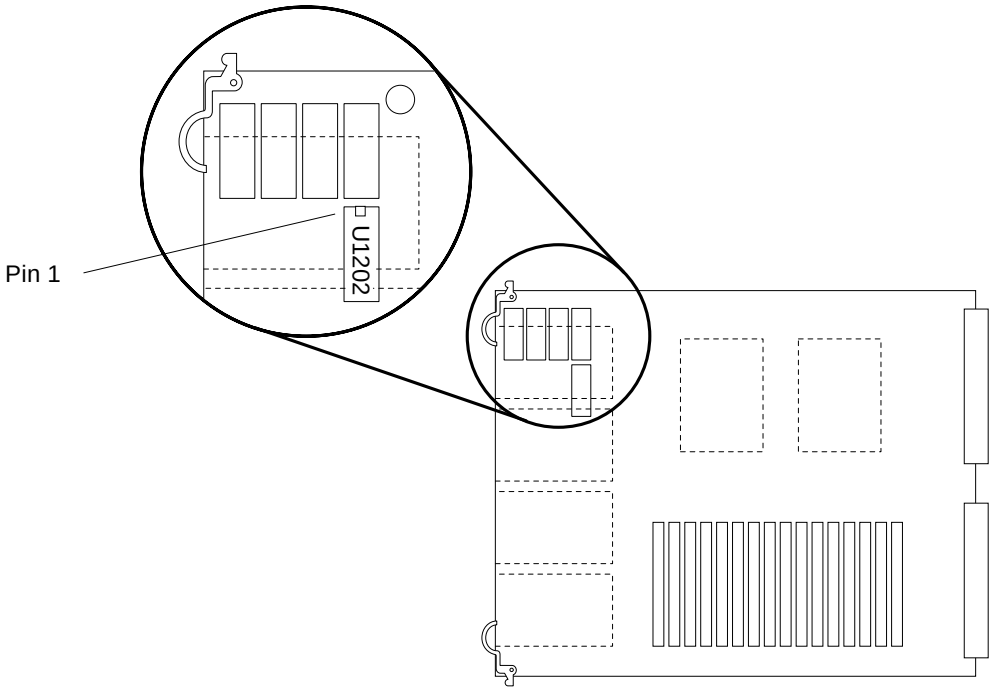


Figure 2-18 TOD / NVRAM Location

2.8.1 Removal

1. **To access the TOD/NVRAM, remove the SBus card (if any) in SBus slot 0.**
2. **Use an IC extraction tool to remove the the device.**
3. **Place the device on antistatic foam and store in antistatic packaging.**

2.8.2 Replacement

1. **Position the NVRAM carefully on the socket, and partially seat the device.**
   Orient the divice pin1 correctly as shown in Figure 2-18.
2. **Check for bent pins, then press firmly to seat the PROM in the socket.**

Caution – Use a cushioned ESD mat to prevent breakage of parts on the underside of the board.

3. **Install any SBus card that was removed for this procedure.**

2.9 Installing the System Board

Note – For help in selecting a card cage slot for a new system board, refer to Appendix D, “General Rules for System Configuration”.

1. **Carefully insert the board in the proper slot in the card cage, ensuring that the board does not slip out of the upper and lower card guides.**
   The component side of the board is to the right.

Caution – Do not force the board into the slot. Components on either side of the board may scrape against other boards. If the board binds, inspect the slot for obstructions. Inspect both the board and the backplane for bent pins or other damage.

2. **Ensure that both ejector/injector levers are in the outward position as you slide the board toward the backplane connectors. Refer to back Figure 2-2.**
   The board will not seat fully unless the levers are in this starting position.

3. **Use the ejector/injector levers to seat the board.**
   Simultaneously, swing both ejector/injector levers into the locked position. Do not press on board to seat it — doing so will damage the connector pins.
4. **Install two screws to secure the board to the card cage.**
5. **Connect any applicable interface cables to the system board backpanel.**

2.10 Replacing the Rear Screen

1. **Place the bottom of the panel on flanges near the bottom of the cabinet.**
   Refer back to Figure 2-1.
2. **Tilt the rear screen against the frame and install two screws to secure the screen in place.**

2.11 Restarting the System

To verify that the hardware has been installed properly, run the POST program.

1. **Turn on power to the monitor.**
   If the system lacks a monitor, connect an TTY terminal to serial port A on the system master board and configure the terminal software. Refer to the instruction manual shipped with the terminal for configuration instructions. The most commonly-used set-up is:

   - 9600 bps
   - 1 stop bit
   - 8 data bits
   - Parity off
   - Full duplex

   Refer to the instruction manual shipped with the terminal for configuration instructions.

Note – Parameters listed may differ from customer site settings. See the `set-defaults` & `printenv` commands in the manual, *OpenBoot Command Reference*.

---

2. **Turn the server key switch to the On position to run POST diagnostics.**
   Watch the diagnostics display for error messages. POST should finish in approximately 60 seconds.

3. **Watch the boot display to confirm that the newly installed or replaced hardware are recognized.**

Note – In the event of “loss of carrier” or “not responding” messages, refer to Section 2.5.2.1, “Preparing a New SBus Card“.

4. **After the system finishes booting, log in and resume normal operation.**

2.12 Selecting a System Master

OBP must select a new system master from among the system boards in the card cage in any of these situations:

- If the system master is replaced with a new system board
- If the NVRAM on the system master is replaced
- If two or more system master boards are in the card cage

A specific configuration and card cage slot position is required for the system master. Refer to Section D.1, “System Master Board.”

2.12.1 When a Terminal Is Present

If the terminal is connected to the correct system board (watch for one board with flashing LEDs during boot-up), the OBP prompt will appear approximately 20 seconds after the system begins to power up. The actual time depends on the amount of memory to be tested.

Caution – If the terminal is connected to the *wrong* board, the message will not appear. At this point the system may seem to be locked up, but OBP is only pausing, waiting for you to respond at a different board.

The following example for a three board system shows the prompt and the recommended responses (`0` and `y`).

```
ttya initialized
Need to select system master from the following boards:
Board#0 -- nvram slave, Prom Version nnnnnnnnn
Board#1 -- nvram slave, Prom Version nnnnnnnnn
Board#2 -- nvram slave, Prom Version nnnnnnnnn
Please enter the desired board#: 0
Are you sure? <y/n>: y
Resetting ...
```

If you enter an illegal board number, or select a board that has no SuperSPARC modules, OBP will prompt you for another selection.

2.12.2 *When a Terminal Is Not Present*

If only one system board is installed, OBP automatically selects this board as the new system master.

If there is no terminal on the system, remove all system boards except one from card cage slot 0 to force OBP to select this board as the new master.

Jumpers

Use this appendix to verify jumper settings on NVSIMMs, DSBE/S and FSBE/S SBus cards, and system boards.

A.1 NVSIMM Jumpers

Before installing NVSIMMs, activate the battery. Move the jumper to the battery ON position. Refer to Figure A-1.

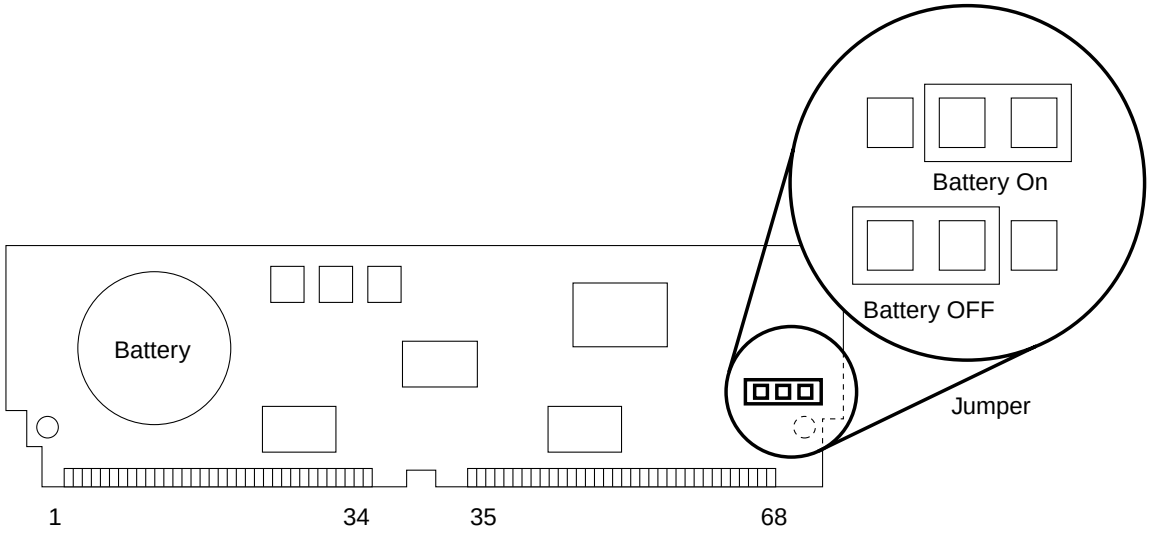


Figure A-1 NVSIMM Jumper Locations

Caution – Never move the jumper after the battery has been turned on, or data contained in the NVSIMM will be lost.

A.2 DSBE/S Link Integrity Test Jumper

Set the J0302 jumper (refer to Figure A-2) as required by 10BaseT Ethernet devices. Sun Microsystems ships the card with the Link Integrity Test enabled.

Note – If the customer chooses to disable the test, it should be disabled both at the hub and at the DSBE/S card. In the event of "loss of carrier" or "not responding" problems, check the status of the link enable on both the DSBE/S SBus card and the hub.

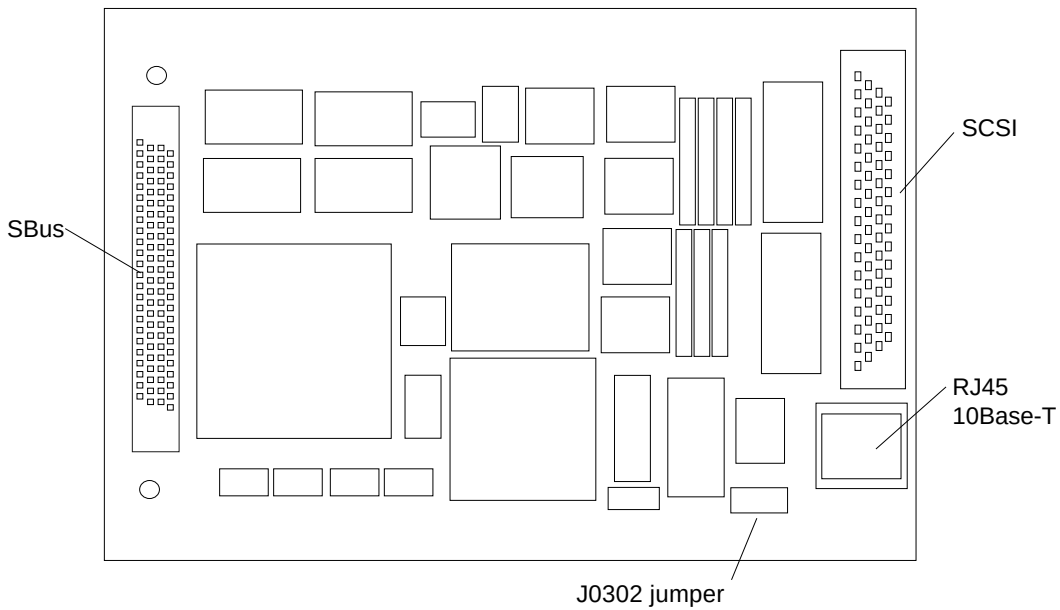


Figure A-2 DSBE/S SBus Card Jumper

To configure the Link Integrity Test jumper:

- Put the shunt over both pins on the jumper to *disable* the test.
- Put the shunt over only one pin of the jumper to *enable* the test.

A.2.1 FSBE/S Link Integrity Test Jumper

Set the J0202 jumper (refer to Figure A-3) as required by 10BaseT Ethernet devices. Sun Microsystems ships the card with the Link Integrity Test enabled.

Note – If the customer chooses to disable the test, it should be disabled both at the hub and at the FSBE/S card. In the event of "loss of carrier" or "not responding" problems, check the status of the link enable on both the FSBE/S SBus card and the hub.

Figure A-3 FSBE/S SBus Card Jumper

To configure the Link Integrity Test jumper:

- Put the shunt over both pins on the jumper to *disable* the test.
- Put the shunt over only one pin of the jumper to *enable* the test.

A.3 System Board Jumpers

Refer to Figure A-4 for the location of system board jumpers.

Note – Board jumpers are set at the factory and should not be changed except for use with factory diagnostic equipment and software.

Pin 1 of each location is identified by a square solder pad.

Table A-1 System Board Jumpers

Label	Jumper	Default Setting	Function
J1400	Pins 2, 3	In	Connects +12V to RS232 line driver. (Pin 1 = ground, pin 2 = line driver input, pin 3 = +12V supply.)
J1401	Pins 2, 3	In	Connects –12V to RS232 line driver. (Pin 1 = ground, pin 2 = line driver input, pin 3 = –12V supply.)
J1501	2, 3	In	Pins 1 and 2 are for factory or service depot use only. Pins 2 and 3 are connected if a service processor does not have a mouse.

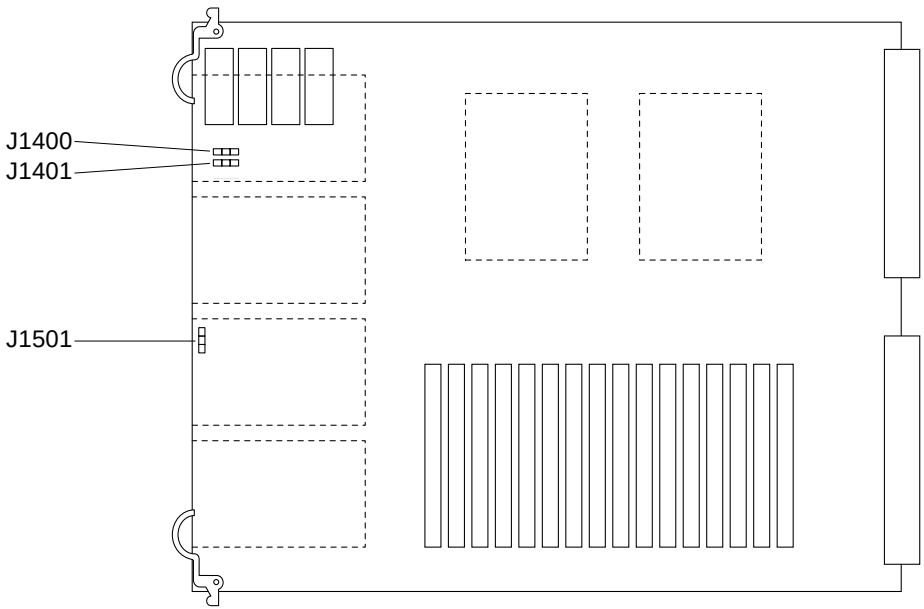


Figure A-4 Jumper Locations on the System Board

Connector Pinouts B

This appendix lists pinouts of connectors on the system board:

- Keyboard and mouse connector
- Serial port connectors A and B
- SBus slots 0, 1, 2, and 3
- XDBus connectors 0 and 1
- SuperSPARC module slots A and B

B.1 Connector Locations

Figure B-1 shows the end view and the side view of the system board.

The end panel has cable connectors for serial ports and a keyboard/mouse cable. The side of the board has connectors for SBus cards, SuperSPARC modules, and the XDBus connectors. These connectors are described in this appendix.

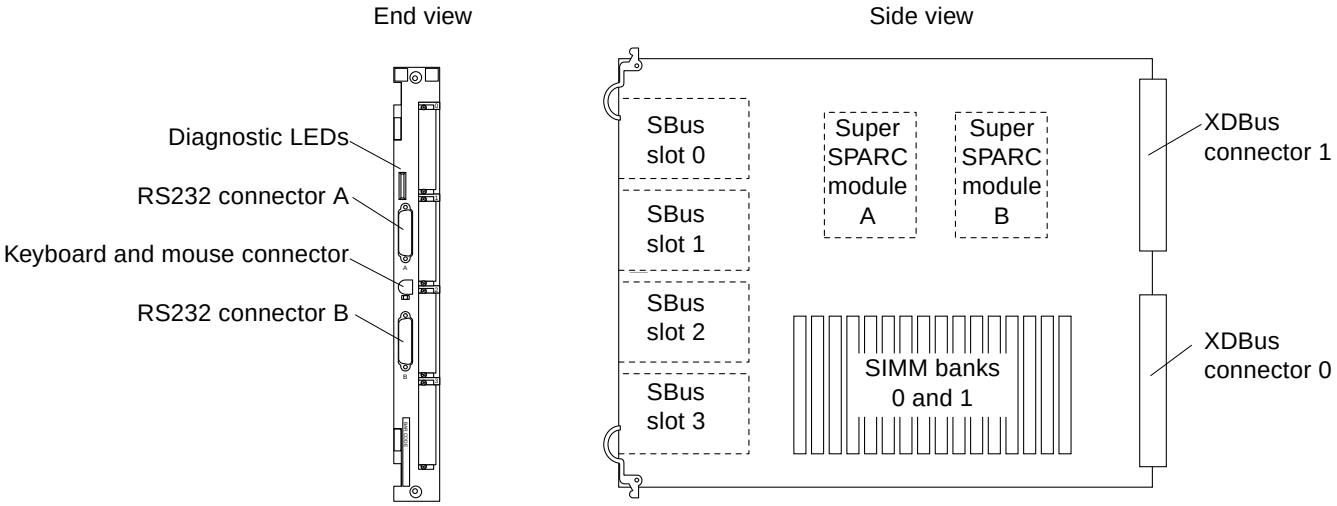


Figure B-1 End and Side Views of the System Board

B.2 Keyboard and Mouse Connector

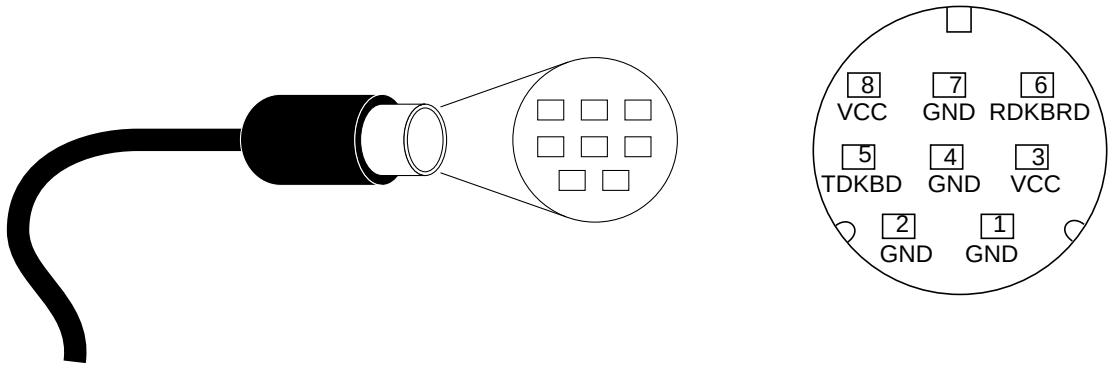


Figure B-2 Keyboard / Mouse Connector (DIN-8) Pinout

B.3 Serial Port Connectors

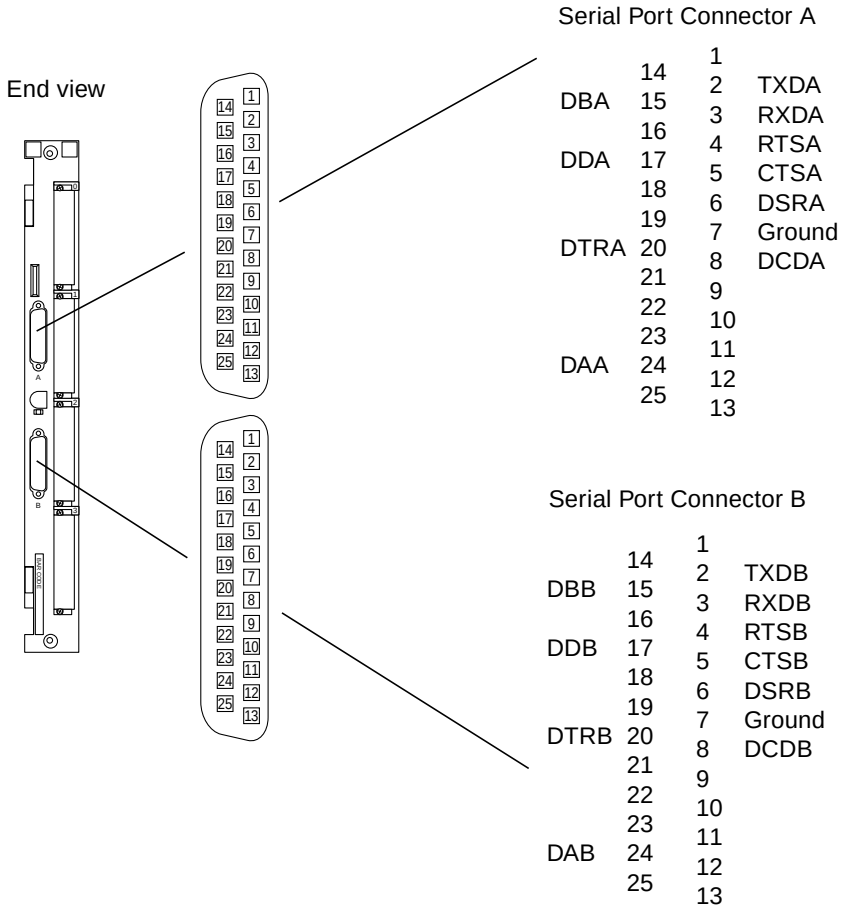


Figure B-3 Serial Port A and B Connector Pinouts

B.4 SBus Connectors

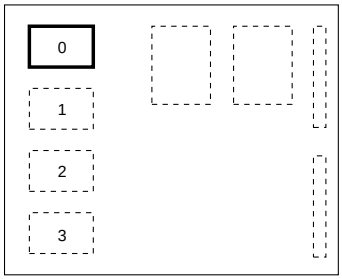


Table B-1 SBus Connector 0 (Connector J5700)

Section 1		Section 2		Section 3	
1	GND	33	SB_PA<6>	65	SB_D<18>
2	SB_BR_L<0>	34	SB_PA<8>	66	SB_D<20>
3	SB_Sel_L<0>	35	SB_PA<10>	67	SB_D<22>
4	SBIntR_L<0>	36	SB_Ack<0>	68	GND
5	SB_D<0>	37	SB_PA<12>	69	SB_D<24>
6	SB_D<2>	38	SB_PA<14>	70	SB_D<26>
7	SB_D<4>	39	SB_PA<16>	71	SB_D<28>
8	SBIntR_L<1>	40	SB_Ack<1>	72	VCC
9	SB_D<6>	41	SB_PA<18>	73	SB_D<30>
10	SB_D<8>	42	SB_PA<20>	74	SB_Siz<1>
11	SB_D<10>	43	SB_PA<22>	75	SB_Rd
12	SBIntR_L<2>	44	SB_Ack<2>	76	GND
13	SB_D<12>	45	SB_PA<24>	77	SB_PA<1>
14	SB_D<13>	46	SB_PA<26>	78	SB_PA<3>
15	SB_D<16>	47	SB_DPar	79	SB_PA<5>
16	SBIntR_L<3>	48	FS_VBB	80	VCC
17	SB_D<19>	49	SB_Clk<0>	81	SB_PA<7>
18	SB_D<21>	50	SB_SBG_L<0>	82	SB_PA<9>
19	SB_D<23>	51	SB_A._L	83	SB_PA<11>
20	SBIntR_L<4>	52	GND	84	GND
21	SB_D<25>	53	SB_D<1>	85	SB_PA<13>
22	SB_D<27>	54	SB_D<3>	86	SB_PA<15>
23	SB_D<29>	55	SB_D<5>	87	SB_PA<17>
24	SBIntR_L<5>	56	VCC	88	VCC
25	SB_D<31>	57	SB_D<7>	89	SB_PA<19>
26	SB_Siz<0>	58	SB_D<9>	90	SB_PA<21>
27	SB_Siz<2>	59	SB_D<11>	91	SB_PA<23>
28	SBIntR_L<6>	60	GND	92	GND
29	SB_PA<0>	61	SB_D<13>	93	SB_PA<25>
30	SB_PA<2>	62	SB_D<15>	94	SB_PA<27>
31	SB_PA<4>	63	SB_D<17>	95	SB_Rst_L<0>
32	SBLErr_L	64	VCC	96	FS_VDD

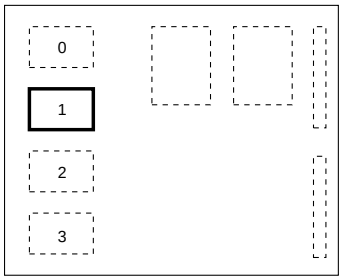


Table B-2 SBus Connector 1 (Connector J5701)

Section 1		Section 2		Section 3	
1	GND	33	SB_PA<6>	65	SB_D<18>
2	SB_BR_L<1>	34	SB_PA<8>	66	SB_D<20>
3	SB_Sel_L<1>	35	SB_PA<10>	67	SB_D<22>
4	SBIntR_L<7>	36	SB_Ack<0>	68	GND
5	SB_D<0>	37	SB_PA<12>	69	SB_D<24>
6	SB_D<2>	38	SB_PA<14>	70	SB_D<26>
7	SB_D<4>	39	SB_PA<16>	71	SB_D<28>
8	SBIntR_L<8>	40	SB_Ack<1>	72	VCC
9	SB_D<6>	41	SB_PA<18>	73	SB_D<30>
10	SB_D<8>	42	SB_PA<20>	74	SB_Siz<1>
11	SB_D<10>	43	SB_PA<22>	75	SB_Rd
12	SBIntR_L<9>	44	SB_Ack<2>	76	GND
13	SB_D<12>	45	SB_PA<24>	77	SB_PA<1>
14	SB_D<13>	46	SB_PA<26>	78	SB_PA<3>
15	SB_D<16>	47	SB_DPar	79	SB_PA<5>
16	SBIntR_L<10>	48	FS_VBB	80	VCC
17	SB_D<19>	49	SB_Clk<1>	81	SB_PA<7>
18	SB_D<21>	50	SB_SBG_L<0>	82	SB_PA<9>
19	SB_D<23>	51	SB_A._L	83	SB_PA<11>
20	SBIntR_L<11>	52	GND	84	GND
21	SB_D<25>	53	SB_D<1>	85	SB_PA<13>
22	SB_D<27>	54	SB_D<3>	86	SB_PA<15>
23	SB_D<29>	55	SB_D<5>	87	SB_PA<17>
24	SBIntR_L<12>	56	VCC	88	VCC
25	SB_D<31>	57	SB_D<7>	89	SB_PA<19>
26	SB_Siz<0>	58	SB_D<9>	90	SB_PA<21>
27	SB_Siz<2>	59	SB_D<11>	91	SB_PA<23>
28	SBIntR_L<13>	60	GND	92	GND
29	SB_PA<0>	61	SB_D<13>	93	SB_PA<25>
30	SB_PA<2>	62	SB_D<15>	94	SB_PA<27>
31	SB_PA<4>	63	SB_D<17>	95	SB_Rst_L<1>
32	SBLErr_L	64	VCC	96	FS_VDD

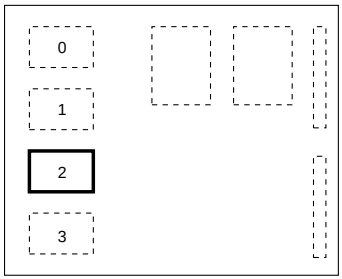


Table B-3 SBus Connector 2 (Connector J5702)

Section 1		Section 2		Section 3	
1	GND	33	SB_PA<6>	65	SB_D<18>
2	SB_BR_L<2>	34	SB_PA<8>	66	SB_D<20>
3	SB_Sel_L<2>	35	SB_PA<10>	67	SB_D<22>
4	SBIntR_L<4>	36	SB_Ack<0>	68	GND
5	SB_D<0>	37	SB_PA<12>	69	SB_D<24>
6	SB_D<2>	38	SB_PA<14>	70	SB_D<26>
7	SB_D<4>	39	SB_PA<16>	71	SB_D<28>
8	SBIntR_L<15>	40	SB_Ack<1>	72	VCC
9	SB_D<6>	41	SB_PA<18>	73	SB_D<30>
10	SB_D<8>	42	SB_PA<20>	74	SB_Siz<1>
11	SB_D<10>	43	SB_PA<22>	75	SB_Rd
12	SBIntR_L<16>	44	SB_Ack<2>	76	GND
13	SB_D<12>	45	SB_PA<24>	77	SB_PA<1>
14	SB_D<13>	46	SB_PA<26>	78	SB_PA<3>
15	SB_D<16>	47	SB_DPar	79	SB_PA<5>
16	SBIntR_L<17>	48	FS_VBB	80	VCC
17	SB_D<19>	49	SB_Clk<2>	81	SB_PA<7>
18	SB_D<21>	50	SB_SBG_L<2>	82	SB_PA<9>
19	SB_D<23>	51	SB_A._L	83	SB_PA<11>
20	SBIntR_L<18>	52	GND	84	GND
21	SB_D<25>	53	SB_D<1>	85	SB_PA<13>
22	SB_D<27>	54	SB_D<3>	86	SB_PA<15>
23	SB_D<29>	55	SB_D<5>	87	SB_PA<17>
24	SBIntR_L<19>	56	VCC	88	VCC
25	SB_D<31>	57	SB_D<7>	89	SB_PA<19>
26	SB_Siz<0>	58	SB_D<9>	90	SB_PA<21>
27	SB_Siz<2>	59	SB_D<11>	91	SB_PA<23>
28	SBIntR_L<20>	60	GND	92	GND
29	SB_PA<0>	61	SB_D<13>	93	SB_PA<25>
30	SB_PA<2>	62	SB_D<15>	94	SB_PA<27>
31	SB_PA<4>	63	SB_D<17>	95	SB_Rst_L<2>
32	SBLErr_L	64	VCC	96	FS_VDD

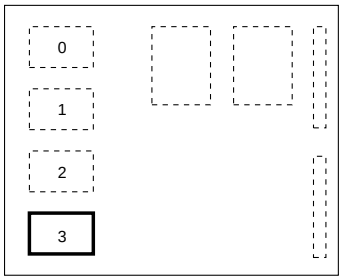


Table B-4 SBus Connector 3 (Connector J5703)

Section 1		Section 2		Section 3	
1	GND	33	SB_PA<6>	65	SB_D<18>
2	SB_BR_L<3>	34	SB_PA<8>	66	SB_D<20>
3	SB_Sel_L<3>	35	SB_PA<10>	67	SB_D<22>
4	SBIntR_L<21>	36	SB_Ack<0>	68	GND
5	SB_D<0>	37	SB_PA<12>	69	SB_D<24>
6	SB_D<2>	38	SB_PA<14>	70	SB_D<26>
7	SB_D<4>	39	SB_PA<16>	71	SB_D<28>
8	SBIntR_L<22>	40	SB_Ack<1>	72	VCC
9	SB_D<6>	41	SB_PA<18>	73	SB_D<30>
10	SB_D<8>	42	SB_PA<20>	74	SB_Siz<1>
11	SB_D<10>	43	SB_PA<22>	75	SB_Rd
12	SBIntR_L<23>	44	SB_Ack<2>	76	GND
13	SB_D<12>	45	SB_PA<24>	77	SB_PA<1>
14	SB_D<13>	46	SB_PA<26>	78	SB_PA<3>
15	SB_D<16>	47	SB_DPar	79	SB_PA<5>
16	SBIntR_L<24>	48	FS_VBB	80	VCC
17	SB_D<19>	49	SB_Clk<3>	81	SB_PA<7>
18	SB_D<21>	50	SB_SBG_L<3>	82	SB_PA<9>
19	SB_D<23>	51	SB_A._L	83	SB_PA<11>
20	SBIntR_L<25>	52	GND	84	GND
21	SB_D<25>	53	SB_D<1>	85	SB_PA<13>
22	SB_D<27>	54	SB_D<3>	86	SB_PA<15>
23	SB_D<29>	55	SB_D<5>	87	SB_PA<17>
24	SBIntR_L<26>	56	VCC	88	VCC
25	SB_D<31>	57	SB_D<7>	89	SB_PA<19>
26	SB_Siz<0>	58	SB_D<9>	90	SB_PA<21>
27	SB_Siz<2>	59	SB_D<11>	91	SB_PA<23>
28	SBIntR_L<27>	60	GND	92	GND
29	SB_PA<0>	61	SB_D<13>	93	SB_PA<25>
30	SB_PA<2>	62	SB_D<15>	94	SB_PA<27>
31	SB_PA<4>	63	SB_D<17>	95	SB_Rst_L<3>
32	SBLErr_L	64	VCC	96	FS_VDD

B.5 XDBus Backplane Connectors

There are two XDBus connectors on the system board.

B.5.1 XDBus Connector 0

Figure B-4 shows the location of XDBus connector 0 and Table B-5 lists pins in this connector.

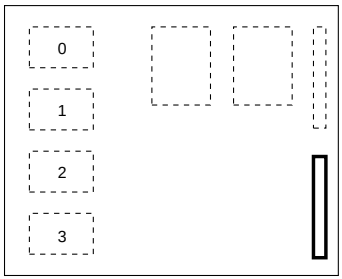


Figure B-4 Location of XDBus Connector 0

Table B-5 XDBus Connector 0 (Connector P0200) *(1 of 3)*

Section 1		Section 2		Section 3		Section 4	
A1	VTT	B1	GND	C1	GND	D1	SyPwrRst_L
A2	GND	B2	GND	C2	N.C.	D2	VCC
A3	VTT	B3	SYSECR	C3	GND	D3	N.C.
A4	SYRST_L	B4	AC_Fail	C4	SYSRST_L	D4	LEDGN_L
A5	LEDYEL_L	B5	LEDRED_L	C5	DIAGMODE	D5	Fan_Fail
A6	N.C	B6	GND	C6	DC_OK	D6	VCC
A7	VTT	B7	SY0RQ_L<1>	C7	GND	D7	SY0RQ_L<0>
A8	GND	B8	SY0RQS_L	C8	SY0RQ_L<2>	D8	VCC
A9	SyEClk	B9	GND	C9	SY0RQP_L	D9	SY0RQO_L
A10	SyEClk_L	B10	GND	C10	SY0GT_L	D10	VCC
A11	GND	B11	SY0GTT_L<3>	C11	GND	D11	SY0GTT_L<0>
A12	SY0GTS_L<2>	B12	GNDS	C12	SY0GTT_L<2>	D12	VCC
A13	GND	B13	SY0GTP_L	C13	GND	D13	SY0GTO_L

Table B-5 XDBus Connector 0 (Connector P0200) *(2 of 3)*

Section 1		Section 2		Section 3		Section 4	
A14	SY0D_L<1>	B14	GND	C14	SY0D_L<0>	D14	VCC
A15	VTT	B15	SY0D_L<3>	C15	GND	D15	SY0D_L<2>
A16	SY0D_L<5>	B16	GND	C16	SY0D_L<4>	D16	VCC
A17	GND	B17	SY0D_L<7>	C17	GND	D17	SY0D_L<6>
A18	SY0DP_L<8>	B18	GND	C18	SY0DP_L<0>	D18	VCC
A19	VTT	B19	SY0D_L<10>	C19	GND	D19	SY0D_L<9>
A20	SY0D_L<12>	B20	GND	C20	SY0D_L<11>	D20	VCC
A21	GND	B21	SY0D_L<14>	C21	GND	D21	SY0D_L<13>
A22	SY0DP_L<1>	B22	GND	C22	SY0D_L<15>	D22	VCC
A23	VTT	B23	N.C.	C23	GND	D23	N.C.
A24	N.C.	B24	GND	C24	N.C.	D24	VCC
A25	GND	B25	SY0D_L<17>	C25	GND	D25	SY0D_<16>
A26	SY0D_L<19>	B26	GND	C26	SY0D_L<18>	D26	VCC
A27	VTT	B27	SY0D_L<21>	C27	GND	D27	SY0D_L<20>
A28	SY0D_L<23>	B28	GND	C28	SY0D_L<22>	D28	VCC
A29	GND	B29	SY0D_L<24>	C29	GND	D29	SY0DP_L<2>
A30	SY0D_L<26>	B30	GND	C30	SY0D_L<25>	D30	VCC
A31	VTT	B31	SY0D_L<28>	C31	GND	D31	SY0D_L<27>
A32	SY0D_L<30>	B32	GND	C32	SY0D_L<29>	D32	VCC
A33	GND	B33	SY0DP_L<3>	C33	GND	D33	SY0D_L<31>
A34	N.C.	B34	GND	C34	N.C.	D34	VCC
A35	VTT	B35	N.C.	C35	GND	D35	N.C.
A36	SY0D_L<33>	B36	GND	C36	SY0D_L<32>	D36	VCC
A37	GND	B37	SY0D_L<35>	C37	GND	D37	SY0D_L<34>
A38	SY0D_L<37>	B38	GND	C38	SY0D_L<36>	D38	VCC
A39	VTT	B39	SY0D_L<39>	C39	GND	D39	SY0D_L<38>
A40	SY0DP_L<40>	B40	GND	C40	SY0DP_L<4>	D40	VCC

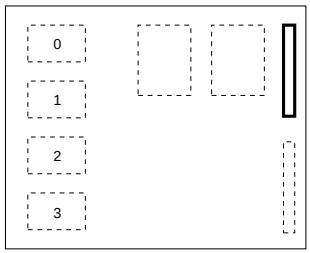
Table B-5 XDBus Connector 0 (Connector P0200) *(3 of 3)*

Section 1		Section 2		Section 3		Section 4	
A41	GND	B41	SY0D_L<42>	C41	GND	D41	SY0D_L<41>
A42	SY0D_L<44>	B42	GND	C42	SY0D_L<43>	D42	VCC
A43	VTT	B43	SY0D_L<46>	C43	GND	D43	SY0D_L<45>
A44	SY0DP_L<5>	B44	GND	C44	SY0D_L<47>	D44	VCC
A45	GND	B45	N.C.	C45	GND	D45	N.C.
A46	N.C.	B46	GND	C46	N.C.	D46	VCC
A47	VTT	B47	SY0D_L<49>	C47	GND	D47	SY0D_L<48>
A48	SY0D_L<51>	B48	GND	C48	SY0D_L<50>	D48	VCC
A49	GND	B49	SY0D_L<53>	C49	GND	D49	SY0DP_L<52>
A50	SY0D_L<55>	B50	GND	C50	SY0D_L<54>	D50	VCC
A51	VTT	B51	SY0D_L<56>	C51	GND	D51	SY0DP_L<6>
A52	SY0D_L<58>	B52	GND	C52	SY0D_L<57>	D52	VBB
A53	GND	B53	SY0D_L<60>	C53	GND	D53	SY0D_L<59>
A54	SY0D_L<62>	B54	GND	C54	SY0D_L<61>	D54	VBB
A55	VTT	B55	SY0DP_L<7>	C55	GND	D55	SY0D_L<63>

B.5.2 XDBus Connector 1

Table B-6 shows the location of XDBus connector 1 and lists connector pins.

Table B-6 XDBus Connector 1 (Connector P0300) *(1 of 2)*



	Section 1		Section 2		Section 3		Section 4	
	A1		B56		C56		D56	
	A1	GND	B1	Sy1D_L<0>	C1	GND	D1	SY1D_L<1>
	A2	SY1D_L<2>	B2	GND	C2	SY1D_L<3>	D2	VDD
	A3	VTT	B3	Sy1D_L<4>	C3	GND	D3	SY1D_L<5>
	A4	SY1D_L<6>	B4	GND	C4	SY1D_L<7>	D4	VDD
	A5	GND	B5	Sy1DP_L<0>	C5	GND	D5	SY1D_L<8>
	A6	SY1D_L<9>	B6	GND	C6	SY1D_L<10>	D6	VCC
	A7	VTT	B7	Sy1D_L<11>	C7	GND	D7	SY1D_L<12>
	A8	SY1D_L<13>	B8	GND	C8	SY1D_L<14>	D8	VCC
	A9	GND	B9	Sy1D_L<15>	C9	GND	D9	SY1DP_L<1>
	A10	N.C.	B10	GND	C10	N.C.	D10	VCC
	A11	VTT	B11	N.C.	C11	GND	D11	N.C.
	A12	SY1D_L<16>	B12	GND	C12	SY1D_L<17>	D12	VCC
	A13	GND	B13	Sy1D_L<13>	C13	GND	D13	SY1D_L<19>
	A14	SY1D_L<20>	B14	GND	C14	SY1D_L<21>	D14	VCC
	A15	VTT	B15	Sy1D_L<22>	C15	GND	D15	SY1D_L<23>
	A16	SY1DP_L<2>	B16	GND	C16	SY1D_L<24>	D16	VCC
	A17	GND	B17	Sy1D_L<25>	C17	GND	D17	SY1D_L<26>
	A18	SY1D_L<27>	B18	GND	C18	SY1D_L<28>	D18	VCC
	A19	VTT	B19	Sy1D_L<29>	C19	GND	D19	SY1D_L<30>
	A20	SY1D_L<31>	B20	GND	C20	SY1DP_L<3>	D20	VCC
	A21	GND	B21	N.C.	C21	GND	D21	N.C.
	A22	N.C.	B22	GND	C22	N.C.	D22	VCC
	A23	VTT	B23	Sy1D_L<32>	C23	GND	D23	SY1D_L<33>
	A24	SY1D_L<34>	B24	GND	C24	SY1D_L<35>	D24	VCC
	A25	GND	B25	Sy1D_L<36>	C25	GND	D25	SY1D_L<37>
	A26	SY1D_L<38>	B26	GND	C26	SY1D_L<39>	D26	VCC
	A27	VTT	B27	Sy1DP_L<4>	C27	GND	D27	SY1D_L<40>

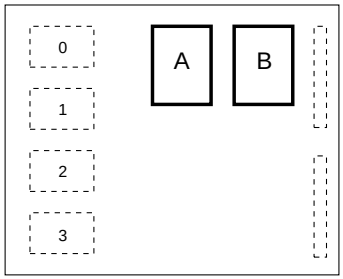
Table B-6 XDBus Connector 1 (Connector P0300) *(2 of 2)*

Section 1		Section 2		Section 3		Section 4	
A28	SY1D_L<41>	A28	GND	C28	SY1D_L<42>	D28	VCC
A29	GND	B29	Sy1D_L<43>	C29	GND	D29	SY1D_L<44>
A30	SY1D_L<45>	B30	GND	C30	SY1D_L<46>	D30	VCC
A31	VTT	B31	Sy1D_L<47>	C31	GND	D31	SY1DP_L<5>
A32	N.C.	B32	GND	C32	N.C.	D32	VCC
A33	GND	B33	N.C.	C33	GND	D33	N.C.
A34	SY1D_L<48>	B34	GND	C34	SY1D_L<49>	D34	VCC
A35	GND	B35	Sy1D_L<50>	C35	GND	D35	SY1D_L<51>
A36	SY1D_L<33>	B36	GND	C36	SY1D_L<53>	D36	VCC
A37	VTT	B37	Sy1D_L<54>	C37	GND	D37	SY1D_L<55>
A38	SY1DP_L<52>	B38	GND	C38	SY1D_L<56>	D38	VCC
A39	GND	B39	Sy1D_L<57>	C39	GND	D39	SY1D_L<58>
A40	SY1D_L<59>	B40	GND	C40	SY1D_L<60>	D40	VCC
A41	VTT	B41	Sy1D_L<61>	C41	GND	D41	SY1D_L<62>
A42	SY1D_L<63>	B42	GND	C42	SY1DP_L<7>	D42	VCC
A43	GND	B43	SY1RQ_L<1>	C43	GND	D43	SY1RQ_L<0>
A44	SysClk_L	B44	GND	C44	SY1RQ_L<2>	D44	VCC
A45	SyClk	B45	GND	C45	SY1RQO_L	D45	SY1RQS_L
A46	GND	B46	ST1GT_L	C46	SY1RP_L	D46	VCC
A47	N.C.	B47	ST1GTT_L	C47	GND	D47	SY1GTT_L<0>
A48	SY1GTS_L	B48	GND	C48	SY1GTT_L<2>	D48	VCC
A49	VTT	B49	SY1GTP_L	C49	GND	D49	SY1GTO_L
A50	N.C.	B50	GND	C50	N.C.	D50	VCC
A51	SYTDO	B51	MSTRPR_L	C51	N.C.	D51	N.C.
A52	SYTD1	B52	SYTCK	C52	SYTMS	D52	SYTAS
A53	GND	B53	BDID<1>	C53	GND	D53	BDID<0>
A54	VTT	B54	GND	C54	BDID<2>	D54	VCC
A55	GND	B55	VTT	C55	GND	D55	BDID<3>

B.6 SuperSPARC Module Connectors

SuperSPARC module connectors A and B have identical pinouts. Each connector has two rows of 50 pins, separated by blade-shaped power supply pins.

Table B-7 SuperSPARC Module Connectors (J2800 and J3100) *(1 of 2)*



	Name	Blade	Name
1	BW0Tdo		51 BdTms
2	BW1Tdo	Ground	52 BdPwrRst_L
3	BDTck		53 BootData<7>
4	BootData<6>	Ground	54 BootData<5>
5	BootData<4>		55 BtStrb_L
6	XData<0>	Ground	56 XData<1>
7	XData<2>		57 XData<3>
8	XData<4>	Ground	58 XData<5>
9	XData<6>		59 XData<7>
10	XData<8>		60 XData<9>
11	XData<10>		61 XData<11>
12	XData<12>	+5V	62 XData<13>
13	XData<14>		63 XData<15>
14	XData<16>	+5V	64 XData<17>
15	XData<18>		65 XData<19>
16	XData<20>	+5V	66 XData<21>
17	XData<22>		67 XData<23>
18	XData<24>	+5V	68 XData<25>
19	XData<26>		69 XData<27>
20	XData<28>		70 XData<29>
21	XData<30>		71 XData<31>
22	XGnt0_L	Ground	72 XReq1_L<1>
23	XDPar<3>		73 XReq1_L<0>

Table B-7 SuperSPARC Module Connectors (J2800 and J3100) *(2 of 2)*

	Name	Blade	Name
24	VikClk	Ground	74 XDPar<2>
25	CcClk		75 XDPar<1>
26	XGtyp_L	Ground	76 XDPar<0>
27	XCCAF_L		77 XReq0_L<1>
28	GND	Ground	78 XReq0_L<0>
29	VREF\G		79 Spare
30	XData<32>		80 XData<33>
31	XData<34>		81 XData<35>
32	XData<36>	+5V	82 XData<37>
33	XData<38>		83 XData<39>
34	XData<40>	+5V	84 XData<41>
35	XData<42>		85 XData<43>
36	XData<44>	+5V	86 XData<45>
37	XData<46>		87 XData<47>
38	XData<48>	+5V	88 XData<49>
39	XData<50>		89 XData<51>
40	XData<52>		90 XData<53>
41	XData<54>		91 XData<55>
42	XData<56>	Ground	92 XData<57>
43	XData<58>		93 XData<59>
44	XData<60>	Ground	94 XData<61>
45	XData<62>		95 XData<63>
46	BootCmd<2>	Ground	96 BootData<3>
47	BootData<2>		97 BootData<1>
48	BootData<0>	Ground	98 CCErr_L
49	BdRst_L		99 BootCmd<1>
50	BootCmd<0>		100 XGnt_L

Environmental Specifications C

C.1 Environmental Requirements

Table C-1 Temperature Limits

	Operating[1]		**Non-operating**	
	US	**Metric**	**US**	**Metric**
Recommended range	50°–104°F	10°–40°C	50°–140°F	10°–60°C
Minimum temperature	50°F at 20% RH	10°C at 20% RH	–4°F	–20°C
Maximum temperature	104°F at 20% RH	40°C at 20% RH	140°F	60°C
Maximum gradient	<27°F / hr, <30% RH / hr	<15°C / hr, <30% RH / hr	<27°F / hr, <30% RH / hr	<15°C / hr, <30% RH / hr
Dwells at extremes	8 hours	8 hours	24 hours	24 hours

1. The 1 / 2-inch front load tape drive has a maximum temperature limit of 86°F (30°C).

Table C-2 Humidity Limits

	Operating		Non-operating	
	US	**Metric**	**US**	**Metric**
Recommended range	20% to 80% RH at 104°F	20% to 80% RH at 40°C	95% RH at 104°F	95% RH at 40°C
Minimum humidity	20%	20%	10%	10%
Maximum humidity	80%	80%	95%	95%
Maximum gradient	<30% RH / hr, <27°F / hr	<30% RH / hr, <15°C / hr	<30% RH / hr, <18°F / hr	<30% RH / hr, <10°C / hr
Dwell at extremes	8 hours	8 hours	120 hours	120 hours

Table C-3 Altitude Limits

	Operating		Non-operating	
	US	**Metric**	**US**	**Metric**
Maximum altitude	10,000 ft	3 km	40,000 ft	12 km
Temperature range	50°–104°F	10°–40°C	32°F	0°C
Maximum gradient	<1.5kPa / min, <18°F / hr	<1.5kPa / min, <10°C / hr	<8kPa / min, <18°F / hr	<8kPa / min, <10°C / hr
Dwell at extremes	4 hours	4 hours	4 hours	4 hours

General Rules for System Configuration

D

This appendix lists recommended priorities and locations for:

- Selecting the proper system board slot
- Selecting a SuperSPARC module location
- Selecting an SBus module location
- Selecting SIMM locations
- Selecting a disk drive tray location
- Selecting drive identification numbers (IDs) in the SCSI tray
- Connecting SCSI cables
- Connecting DSBE/S cables
- Connecting Ethernet
- Connecting video cables

D.1 System Master Board

The system board slot numbers are marked on the card cage. Install system boards from the lowest card cage slot number (0) to the highest (9). Install filler panels in all empty slots.

A system board must be installed in card cage slot 0. If the system has a TTY console, connect it to port A of the system master. A TTY console is not normally required if the system is in auto-boot mode (see the OpenBoot Command Reference for instructions on enabling and disabling auto-boot).

D.1.1 Identifying the System Master

To determine which board is the system master, observe the LEDs on the system board rear panels during boot.

- On the system master the lower eight LEDs (yellow) cycle on and off in a repeated pattern.
- On other system boards the lower eight LEDs are lit in a solid pattern until boot completes.
- After boot ends, all LEDs (on boards with SuperSPARC® modules) will cycle.

The system master must meet a set of minimum hardware requirements, as described next.

D.1.2 Minimum Requirements for the System Master

The system master must have

- one or two SuperSPARC modules

  Two green LEDs, marked PA and PB, denote the presence of functional SuperSPARC modules in slots A and B when lit.

- DSBE/S or DWIS/S interface card in SBus slot 0

  The DSBE/S or DWIS/S card connects to the main network and to the root disk drive. DSBE/S can also connect to the main network.

- FSBE/S interface card in SBus slot 3.

  The FSBE/S card connects to the SCSI tray in the top of the cabinet, and possibly to the main network.

D.1.3 Selecting the System Master Board

Note – The system master board must have the highest-revision PROM set. Also, if your system has OBP patches stored in NVRAM, these must be erased before assigning a board having different revision PROM set as system master. This is required because OBP patches are PROM-version specific. Use the `set-default nvramrc` command at the OPB `ok` prompt to erase patches **before** powering down the system for board reassignment.

Determine which board is the candidate to become the system master. Before installing a given board:

1. **Determine the dash-revision level of Boot PROMs installed on the board. The level is expressed by the last two digits in the part number, as in: 525-xxxx-yy where "yy" conveys the dash-revision level.**
2. **Likewise, examine other system boards installed (or to be installed) in the card cage to determine the dash-revision level of PROMs on these boards.**
3. **Identify the board to be system master:**
   If a board has a higher dash-revision level Boot PROM than the others, it must be the system master.
   If two or three have higher levels, than one from that pool of boards must be the system master.
4. **Install the candidate-board into slot 0 as system master.**

Boot PROMs may be hidden because they reside beneath the SBus card in slot 0, if installed. See Figure D-1. Remove the SBus card as required to expose the OBP for examination to determine the OBP revision level.

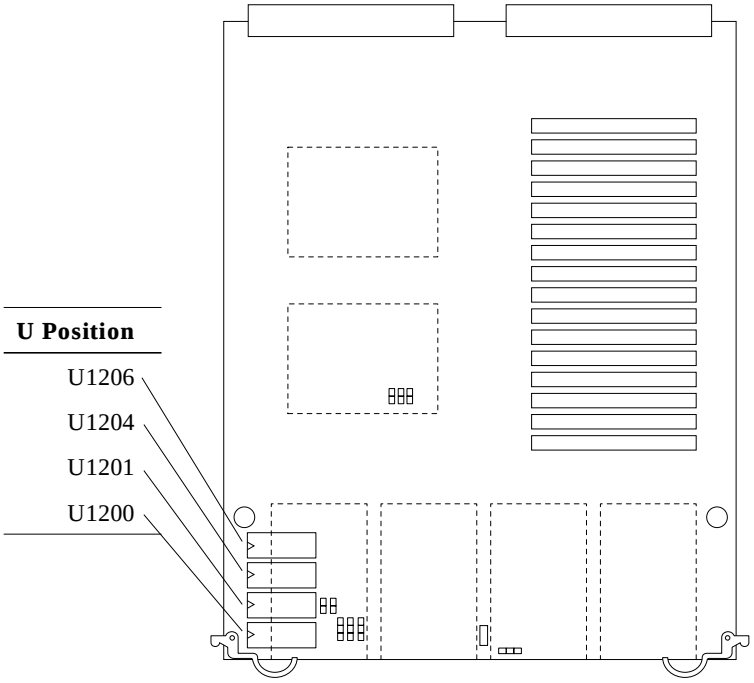


Figure D-1 Open Boot PROM Location

The OpenBoot PROM on the system master is usually the OBP master. This PROM controls the boot process. If the system master is replaced at the customer site by a new system board, the system master must be reassigned by the system. For information on identifying the system master, and on the schemes for selecting a new system master, refer to the *SPARCcenter 2000 Service Manual*, Appendix E.

D.1.3.1 Additional System Master Details

If a serial-interface TTY console is used, it must be connect to serial port A on the system master.

Note – The system master board must connect to a terminal, or you will not see the OBP message. If the terminal is connected to the *wrong* board, the message will not appear. At this point the system may seem to be locked up, but OBP is only pausing, waiting for you to respond.

If a color monitor is used, a color-graphics interface card must be installed in SBus slot 1. Only one color-graphics interface is allowed in the system.

D.2 System Slave Boards

The remaining system boards are “slave boards,” because the master board exercises control during portions of boot and other system operations.

For uniformity of configuration and ease of service, install and equip slave system boards according to the guidelines below. (These guidelines are not required by system architecture, but are strongly recommended, to maintain consistency between systems and to simplify service procedures.)

Install slave boards in the lowest card cage slot numbers, following the system master.

Installing SuperSPARC modules strictly according to the guidelines presented in Section D.3.

Install SIMM devices strictly according to the guidelines presented in Section D.6.

D.3 Selecting a SuperSPARC Module Location

When installing or replacing a SuperSPARC module, use the following guidelines to verify that the location you have selected is correct.

Each system board has two SuperSPARC module connectors, marked A and B. Refer to Figure D-2. Modules should first be installed in the A connectors, in consecutive card cage slots starting from card cage slot 0. After all of the A connectors have been filled, begin filling the B connectors, starting from slot 0.

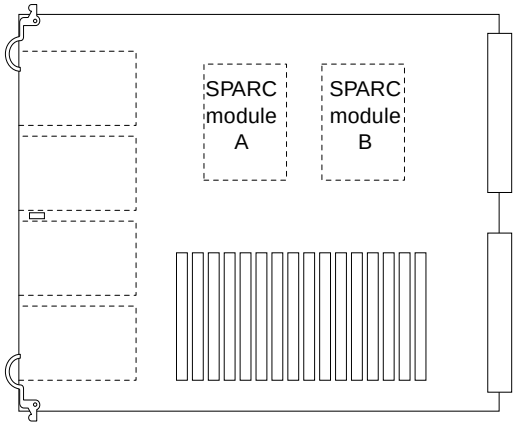


Figure D-2 SuperSPARC Module Locations

The example in Table D-1 shows how to distribute seven SuperSPARC modules on five system boards. (Board slots 5–9 are empty in this example.

Table D-1 Example of Connector and Slot Priorities

Board Slot	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Board present	No	No	No	No	No	Yes	Yes	Yes	Yes	Yes
SuperSPARC Module A	—	—	—	—	—	A	A	A	A	A
SuperSPARC Module B	—	—	—	—	—	—	—	—	B	B

D.4 Selecting an SBus Module Location

Each system board has four SBus slots. Refer to Figure D-3.

The system master is the only system board that has a minimum configuration requirement for SBus cards. Refer to Table D-2. Populate all other system board SBus slots for load balance.

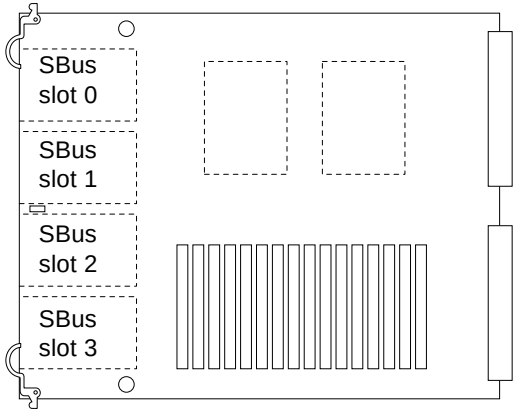


Figure D-3 SBus Card Locations

Table D-2 SBus Slot Requirements for the System Master

Slot	SBus Card	Comments
SBus 0	DSBE/S or DWIS	Interface to root disk and, if DSBE/S, to twisted-pair Ethernet Interface
SBus 1	CGSIX	CGSIX is present if a monitor is part of machine configuration, otherwise the slot is used as general SBus connector
SBus 2	Available	General SBus connector
SBus 3	FSBE/S	To SCSI box

The example in Table D-1 shows how five DSBE/S cards and two FSBE/S cards might be distributed on three system boards. (Board slots 3–9 are empty in this example. D=DSBE/S, F=FSBE/S.)

Table D-3 Example of SBus Card Distribution

	Board Slot Number									
	9	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Board present?	No	No	No	No	No	No	No	Yes	Yes	Yes
SBus slot 0	—	—	—	—	—	—	—	D	D	D

Table D-3 Example of SBus Card Distribution

	Board Slot Number									
	9	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SBus slot 1	—	—	—	—	—	—	—	—	D	D
SBus slot 2	—	—	—	—	—	—	—	—	—	—
SBus slot 3	—	—	—	—	—	—	—	—	F	F

D.5 Selecting SIMM or NVSIMM Locations

The SPARCcenter 2000 system board has two buses, as shown in Figure D-4.

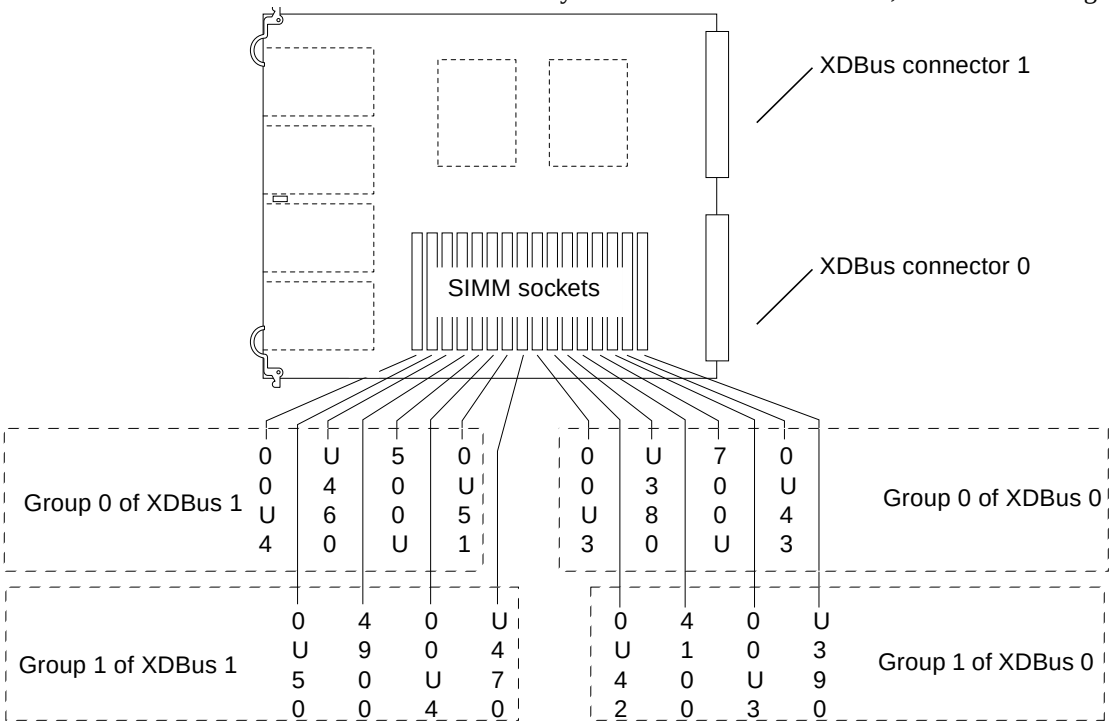


Figure D-4 SIMM Slot Locations and U-numbers

The SIMM slots on each board are divided into four groups of four slots each, and two groups (0 and 1) are attached to each bus.

D.6 SIMM or NVSIMM Installation Rules

Information in this section applies to SIMMs and NVSIMMs. On SPARCcenter 2000 boards (having two buses), install eight SIMMs at a time, four in group x (where x = 0 or 1) on bus 0 and four in the same group number on bus 1.

Note – Fill the lowest -numbered SIMM groups first. For multiple-board configurations, fill group 0 on each board before filling group 1 (but see following for rules for optimizing system performance.)

Note – These devices were designed for the SPARCcenter 2000 and SPARCcenter 2000 and are not interchangeable with other types of SIMMs.

The rules for installing SIMMS in the system board are:

- Always install eight SIMMs at a time, in two groups of four.
- Install one group on bus 0, and the second group in the matching group number on the other bus. For example, fill group 0 on bus 0 and group 0 on bus 1. (Although it is not mandatory that both groups must be on the same board, to avoid confusion it is best to put both groups on the same board.)
- Install SIMMs in both group 0 locations on every board (in groups of two or four boards), before adding SIMMs to any group 1 location.
- A minor exception to the above rule is that to optimize memory performance, you should keep the numbers of memory groups balanced across multiples of two or four boards. (This allows the system to interleave memory across two or four boards.)
- For example, if a system has five boards, and group 0 is filled on all five boards, performance will not be optimal. Memory addresses will be interleaved across the first four boards, but not across the fifth. If this memory is accessed often, performance will suffer.
- Ideally (for the case of five boards), populate group 0 across four boards, then populate group 1 across four boards. The next most optimal case would be to populate group 0 across four boards, then populate group 1 across *two* boards. Both cases allow for interleaving across group 0 memory and separate interleaving across group 1 memory.
- Do not mix SIMM sizes within the two groups of four SIMMs.

D.7 Identifying SIMM or NVSIMM Types

Do not mix SIMMs of different memory capacities in a bank. (SIMMs from different manufacturers can be mixed, so long as the memory capacities are equal. SIMM speeds are limited by the speed of the slowest SIMM.) The system board has various SIMM options:

- The 8 Mbyte SIMMs are shown as Type A and Type B in Figure D-5.
- The 32 Mbyte SIMMs are also shown as Type A and Type B in Figure D-5.

Note – Because the SIMM outline varies by the manufacturer, identify the 8 Mbyte and 32 SIMM capacities by the number of pins on each DRAM: DRAMs on 8 Mbyte SIMMs have 20 pins. DRAMs on 32 Mbyte SIMMs have 24 pins.

- The 1 Mbyte NVSIMM is identified by the presence of a battery. Refer to Type C in Figure D-5.

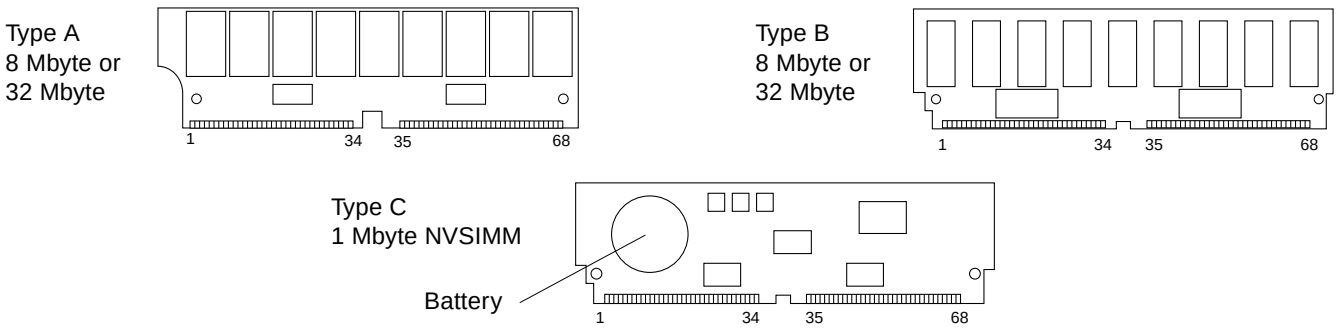


Figure D-5 SIMM Variations

D.8 Locating a Disk Drive Tray

The system cabinet can hold up to three disk drive trays. Install the trays from the bottom up. For identification purposes, the trays will be numbered 1 (bottom), 2 (middle), and 3 (top). The tray numbering for an expansion cabinet also starts from the bottom position. Individual disk drive numbers range from SCSI ID 0 to ID 5 in a drive tray.

D.9 Selecting Drive ID Numbers in the SCSI Box

The SunCD ID number is 6. The first 150 Mbyte 1/4-inch tape drive ID is 5. If there are more 1/4-inch tape drives, the ID numbers must be higher than any 8 mm tape drive. That is, the SunCD has a higher ID number than 1/4-inch tape drives, which have higher ID numbers than 8 mm tape drives.

In addition, if a 1/2-inch front load tape drive is used, the drive ID should be the highest in the string (ID 6).

The example in Table D-4 shows how to number five drives in a SCSI tray.

Table D-4 Example of ID Numbering in a SCSI Tray

Device	ID
SunCD	6
1/4-inch tape drive	5
8 mm tape drive	4
8 mm tape drive	1
8 mm tape drive	0

D.10 Connecting SCSI Cables

The SCSI tray I/O harness terminates at the card cage bottom, near the cabinet rear. One harness connector must connect to the FSBE/S card in SBus slot 3 of the master system. Install a SCSI terminator on the second harness connector.

D.11 Connecting DSBE/S or DWIS Cables

Disk tray 1 in the main cabinet should be connected to the DSBE/S or DWIS card in SBus slot 0 on the system master board. Disk tray 1 usually contains the root disk (although this location is not a physical requirement.) Disk trays 2 and 3 should be connected to the next two lowest DSBE/S or DWIS/S cards. Disk trays in the expansion cabinets should be connected to higher-numbered DWIS/S or DSBE/S cards in the system cabinet card cage.

D.12 Connecting Ethernet

The main network cable may be connected to an Ethernet port of the DSBE/S, FSBE/S or QED/S card. The SPARCcenter 2000 system supports only 10Base-T twisted-pair Ethernet.

D.13 Connecting Video Cables

A maximum of one CG6 color frame buffer is allowed per system. It must be installed in SBus slot 1 of the system master board. The color monitor keyboard must be plugged into the keyboard connector of the system master.

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Revision History

Revision	Dash	Date	Comments
800-6993-13	A	October 1994	Included SPARC module warning
800-6993-11	A	May 1993	
800-6993-10	A	December 1992	First customer shipment

Reader Comments

We welcome your comments and suggestions to help improve the *SPARCcenter 2000 System Board Manual*, part number *800-6993-13*. Please take time to let us know what you think about this manual.

■ The tasks were well documented and easy to follow.

Strongly Agree	Agree	Disagree	Strongly Disagree	Not Applicable
❑	❑	❑	❑	❑

Comments _____

■ The information provided in *SPARCcenter 2000 System Board Manual* was complete.

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Comments _____

■ The information I needed was easy to find.

Strongly Agree	Agree	Disagree	Strongly Disagree	Not Applicable
❑	❑	❑	❑	❑

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Strongly Agree	Agree	Disagree	Strongly Disagree	Not Applicable
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