APPENDIX **A**

Functional Description

This appendix provides an overview of the hardware and software of the Netra t 1400/1405 system. It provides information about the hardware of the system and of the hardware resources visible to the software.

A.1 System

The system is an UltraSPARC port architecture (UPA) based machine that uses peripheral component interconnect (PCI) as the I/O expansion bus. The CPU modules and UPA-to-PCI bridge (U2P) ASIC communicate with each other using the UPA protocol. The CPU modules and the U2P ASIC are UPA master-slave devices. The QSC ASIC routes UPA requests packets through the UPA address bus and controls the flow of data using the XB9++ ASIC and the CBT switching network.

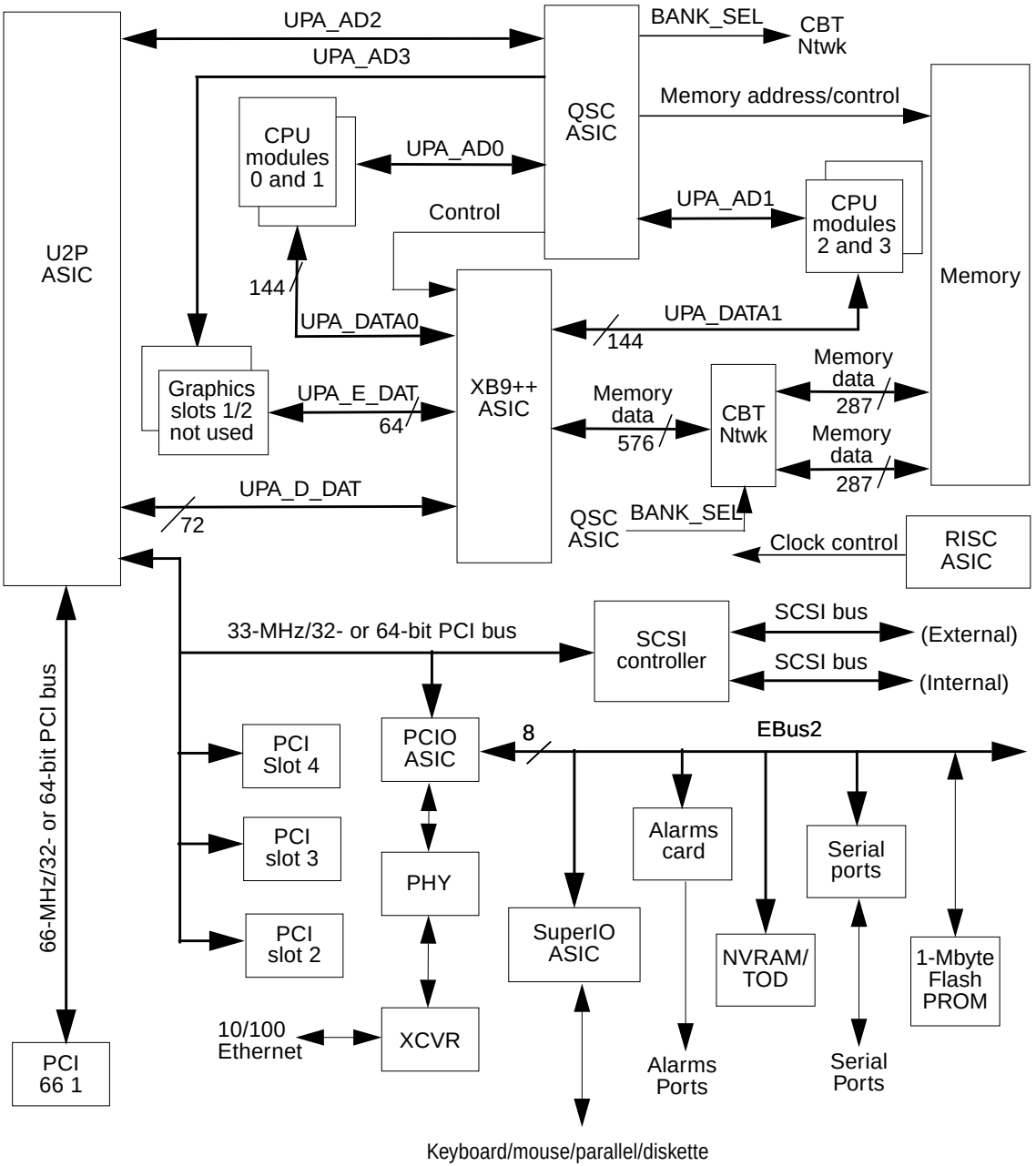


FIGURE A-1 Block Diagram of the Netra t 1400 / 1405 System

A.1.1 UltraSPARC Port Architecture

The UPA provides a packet-based interconnection between the UPA clients, that is, the CPU modules and U2P ASIC. Electrical interconnection is provided through four address buses and four data buses.

TABLE A-1 UPA Interconnects

Bus Name	Bus Designation	Function
UPA address bus 0	UPA_AD0	A full 36-bit bidirectional bus that connects the QSC ASIC to CPU modules 0 and 1
UPA address bus 1	UPA_AD1	A full 36-bit bidirectional bus that connects the QSC ASIC to CPU modules 2 and 3
UPA address bus 2	UPA_AD2	A full 36-bit bidirectional bus that connects the QSC ASIC to the U2P ASIC
UPA address bus 3	UPA_AD3	Not used
UPA data bus 0	UPA_DATA0	A bidirectional 144-bit data bus (128 bits of data and 16 bits of ECC) that connects CPU modules 0 and 1 to the XB9++ ASIC
UPA data bus 1	UPA_DATA1	A bidirectional 144-bit data bus (128 bits of data and 16 bits of ECC) that connects CPU modules 2 and 3 to the XB9++ ASIC
UPA data bus 2	UPA_D_DAT	A bidirectional 72-bit data bus (64 bits of data and 8 bits of ECC) that connects the U2P ASIC to the XB9++ ASIC
UPA data bus 3	UPA_E_DAT	Not used

TABLE A-1 lists the interconnections between the UPA and UPA clients, TABLE A-2 lists the UPA port identification assignments, and FIGURE A-2 illustrates how the UPA address and data buses are connected between the UPA and the UPA clients.

TABLE A-2 UPA Port Identification Assignments

UPA Slot Number	UPA Port ID <4:0>
CPU module slot 0	0x0
CPU module slot 1	0x1
CPU module slot 2	0x2
CPU module slot 3	03
U2P ASIC	0x1F

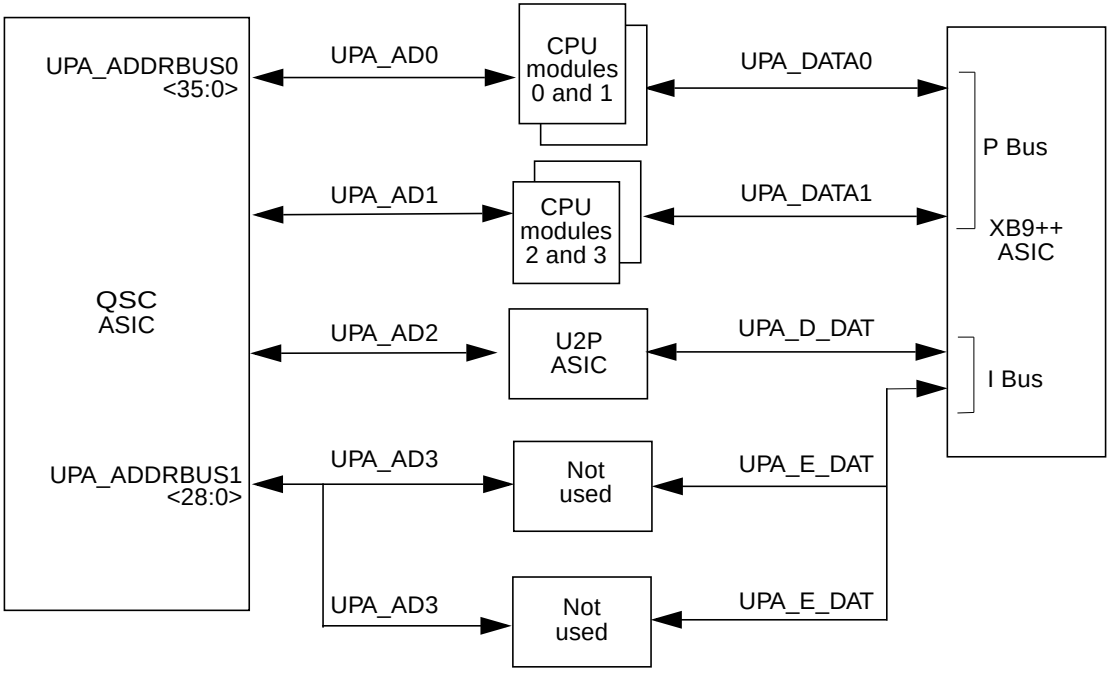


FIGURE A-2 UPA Address and Data Buses Functional Block Diagram

A.1.2 PCI Bus

The PCI bus is a high-performance 32-bit or 64-bit bus with multiplexed address and data lines. The PCI bus provides electrical interconnection between highly integrated peripheral controller components, peripheral add-on devices, and the processor–memory system.

There are two PCI buses (FIGURE A-1):

- a one-slot, 3.3Vdc, 64-bit or 32-bit, 66MHz or 33MHz bus
- a three-slot, 5.0Vcd, 64-bit or 32-bit, 33MHz bus (one slot is 32-bit only)

Both buses are controlled by the U2P ASIC. There are also two on-board controllers, the Symbios 53C876 SCSI controller and the PCI to Ebus/Ethernet controller (PCIO) ASIC, on the 33MHz PCI bus.

A.1.2.1 PCI Cards

PCI cards have a variety of configurations. Not all cards will fit or operate in all PCI slots, so it is important to know the specifications of your PCI cards and the types of cards supported by each PCI slot in the system.

PCI cards can be as short as 6.875in. (17.46cm) in length and are designated as *short*. The maximum length of PCI card that can be accommodated is 12.28in. (31.19cm) and cards of this type are designated *long*. Each PCI slot can accommodate either a short or long card.

Older PCI cards communicate over 32-bit PCI buses, while many newer cards communicate over wider, 64-bit buses. PCI slot 1 accepts 32-bit PCI cards only and PCI slots 2, 3 and 4 accept either 32-bit or 64-bit cards.

Older PCI cards operate at 5VDC while newer cards operate at 3.3VDC. These cards must be used in slots that are designed to operate at the correct voltage. In addition, PCI cards designated as *universal* will operate at either 3.3V or 5V and so can be used in either type of slot. The system provides three slots for 5-volt cards and one slot for a 3.3-volt card. All four PCI slots accept universal. cards.

Most PCI operate a clock speeds of 33MHz, while some newer cards operate at 66MHz. All four PCI slots will accept 33MHz cards, A 66MHz card can be used only in PCI slot 4.

TABLE A-3 lists the mapping of the PCI slots to the two PCI buses, and the types of PCI cards supported in each slot.

TABLE A-3 PCI Slot-to-Bus Mapping

	PCI 4	PCI 3	PCI 2	PCI 66 1
PCI Bus	0	0	0	1
Slot Width (bits)	32	64	64	64
Card Type (bits)	32	32 or 64	32 or 64	32 or 64
Clock Rates (MHz)	33	33	33	66
DC Voltage (VDC)	5.0[1]	5.0[1]	5.0[1]	3.3[1]
Card Size	Short or Long	Short or Long	Short or Long	Short or Long

1. A universal PCI card can be used in any slot.

A.1.2.2 UPA-to-PCI Bridge ASIC

The U2P ASIC controls the PCI buses. It forms the bridge from the UPA bus to the PCI buses. For a brief description of the U2P ASIC, see Section A.10.4 “U2P” on page A-29.

A.1.3 SCSI Controller

The SCSI controller provides electrical connection between the mother board and separate internal and external SCSI buses. The controller also provides the SCSI bus control.

SCSI channel A is used to interface to internal devices. SCSI channel B is used to interface to external devices.

A.1.4 PCI-to-EBus/Ethernet Controller ASIC

The PCIO ASIC connects the PCI bus to the EBus. This enables communication between the PCI bus and all miscellaneous I/O functions, as well as the connection to slower, on-board functions. The PCIO ASIC also embeds the Ethernet controller. For a brief description of the PCIO ASIC, see Section A.10.3 “PCIO” on page A-29.

A.2 UltraSPARC II Processor

The UltraSPARC II processor is a high-performance, highly-integrated super-scalar processor implementing the SPARC-V9 64-bit RISC architecture. The UltraSPARC II processor is capable of sustaining the execution of up to four instructions per cycle even in the presence of conditional branches and cache misses. This sustained performance is supported by a decoupled prefetch and dispatch unit with instruction buffer.

The UltraSPARC II processor module provides 4Mbyte Ecache.

UltraSPARC II processor characteristics and associated features include:

- SPARC-V9 architecture compliance
- Binary compatibility with all SPARC application code:
- Multi-processing support
- Snooping or directory-based protocol support
- Four-way superscalar design with nine execution units
- Four integer execution units
- Three floating-point execution units
- 64-bit address pointers
- 16-Kbyte non-blocking data cache
- 16-Kbyte instruction cache
- Single cycle branch following
- Power management
- Software prefetch instruction support
- Multiple outstanding requests

A.3 Memory System

The system's motherboard provides sixteen slots for high-capacity, dual inline memory modules (DIMMs). Eight of the sixteen slots are located on the motherboard and the other eight are located on the memory riser assembly. The system supports standard 168-pin, 5-volt, 60-nanosecond DIMMs of 64 and 256-Mbyte capacities. Total system memory capacity ranges from 256 Mbytes to 4 Gbytes.

Memory slots are organized into four banks (bank 0 through bank 3), with each bank comprising four slots. Each bank is divided between the motherboard and the memory riser assembly. Consequently, the DIMMs must be installed in groups of four (bank), with two DIMMs being installed in a motherboard bank and two DIMMs being installed in the associated memory riser assembly bank. Individual DIMMs within a bank should be of equal capacity. The system reads from, or writes to, all four DIMMs in a bank simultaneously.

Caution – Failure to populate a DIMM bank with DIMMs of equal capacity will result in inefficient use of memory resource or system failure.

The memory system (FIGURE A-3) consists of four components:

- QSC ASIC
- XB9++ ASIC
- CBT switching network
- Memory module

The QSC ASIC generates memory addresses and control signals to the memory module. The QSC ASIC also coordinates the two 288-bit wide data bus (MEM_DATA0 and MEM_DATA1) data transfers between the XB9++ and the memory module. Co-ordination is provided by the BANK_SEL control signal to the CBT switching network.

The XB9++ ASIC exchanges

- 144-bit wide bus data with the two CPU data buses, UPA_DATA0 and UPA_DATA1
- 72-bit wide bus data (UPA_D_DAT) with the U2P ASIC

This data is placed on a 576-bit wide bus and exchanged with the CBT switching network where it is divided onto two 276-bit wide data buses and exchanged with the memory module.

FIGURE A-3 is a functional block diagram of the memory system. FIGURE A-4 illustrates the memory module arranged in four banks, 0, 1, 2 and 3. FIGURE A-5 shows the motherboard DIMM slot mapping, and FIGURE A-6 shows the riser board DIMM slot mapping.

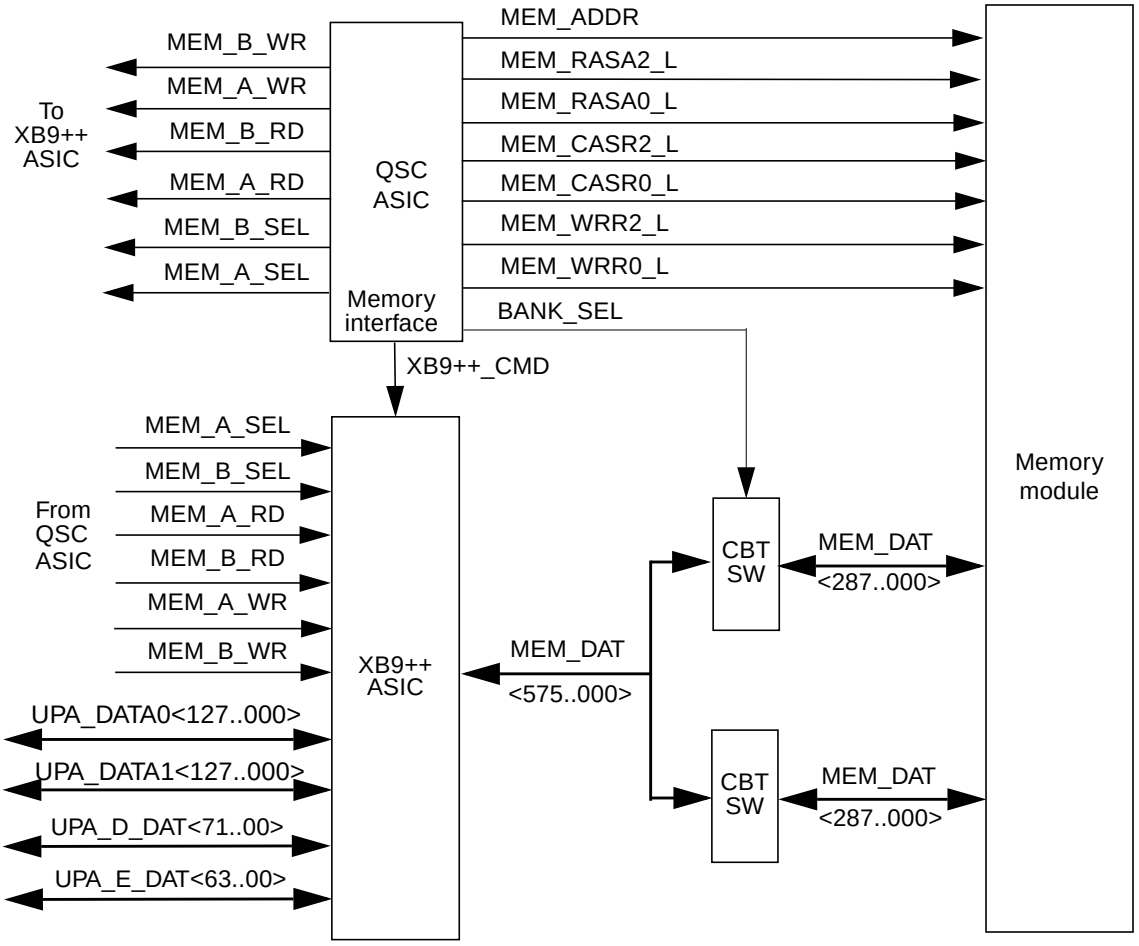


FIGURE A-3 Memory System Functional Block Diagram

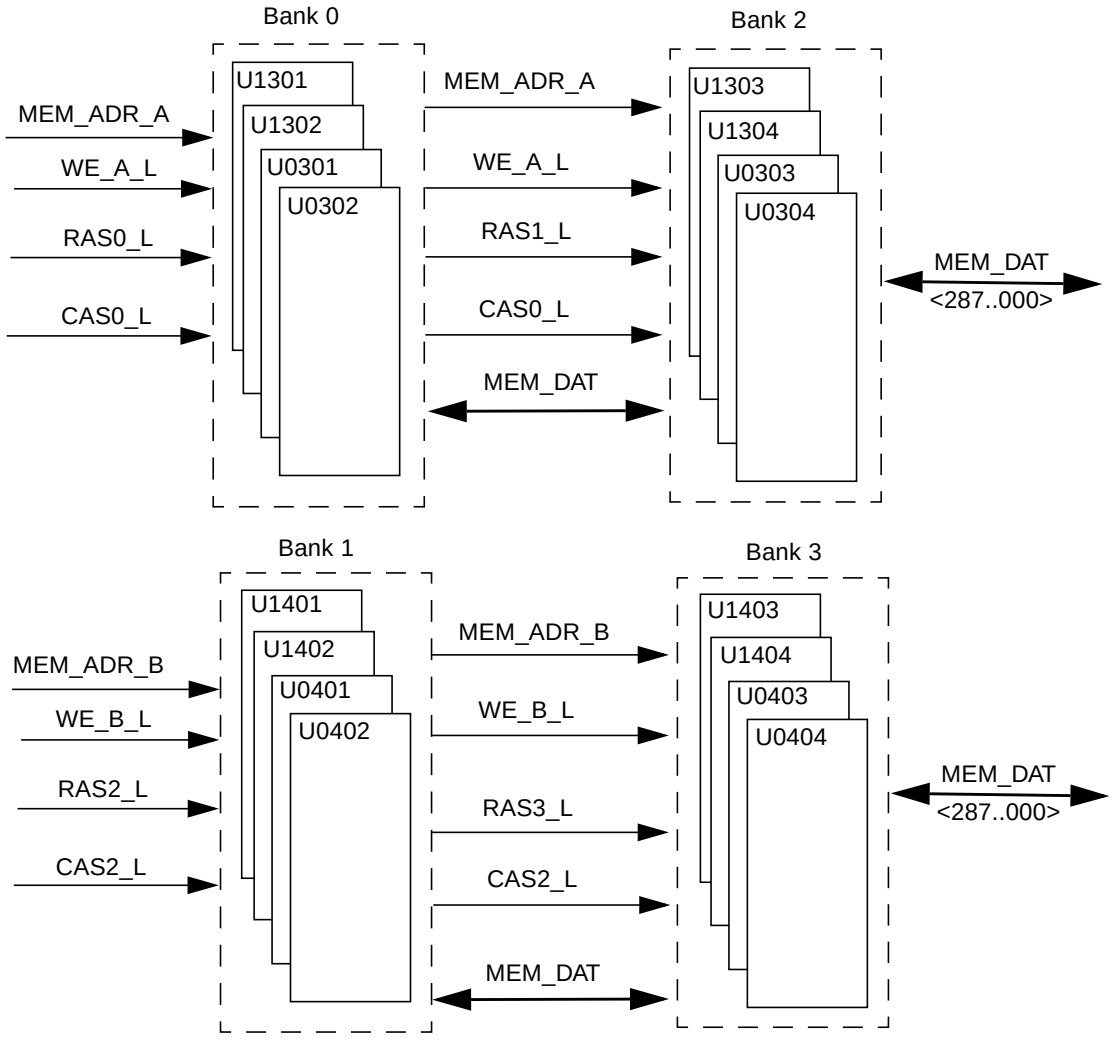


FIGURE A-4 Memory Module Functional Block Diagram

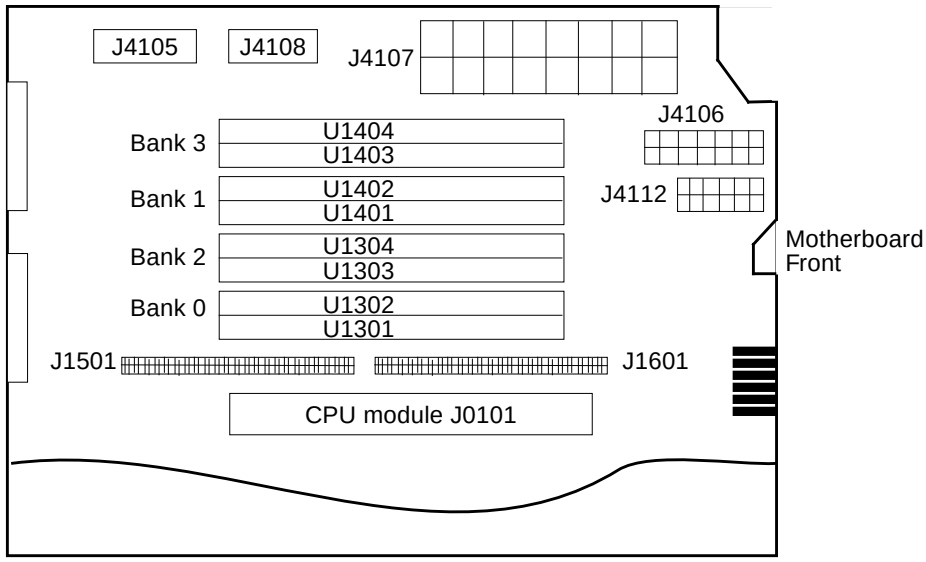


FIGURE A-5 DIMM Mapping (Motherboard)

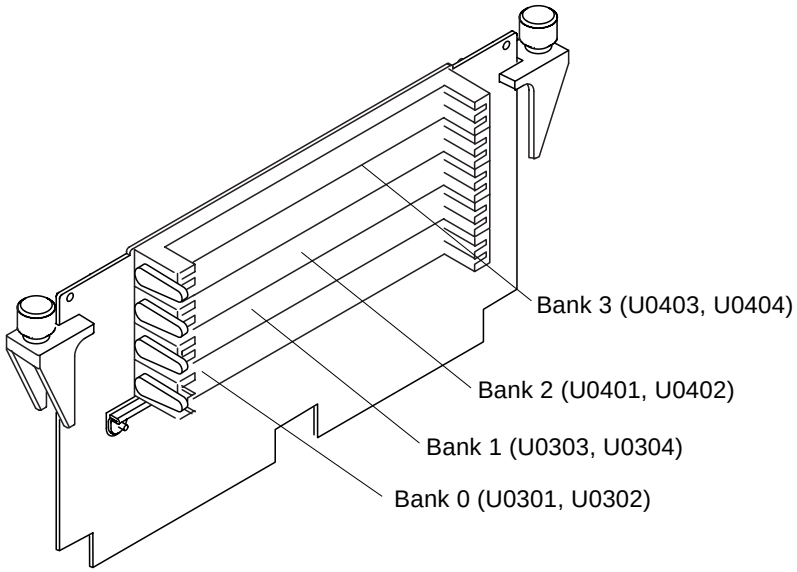


FIGURE A-6 DIMM Mapping (Memory Riser Assembly)

A.3.1 DIMM

The memory module is a 60ns, fast-page-mode DIMM. Two DIMM densities are supported in the system: 64- and 256-Mbyte. The minimum memory capacity is 256Mbyte (four 64-Mbyte DIMMs) and the maximum memory capacity is 4Gbytes (sixteen 256-Mbyte DIMMs).

A block of data (64bytes) always comes from one bank of DIMMs. An error code, containing the address of where a failure occurred as well as the associated syndrome, is logged when an ECC error occurs.

There are a total of four DIMM banks in the system. TABLE A-4 matches DIMM banks to DIMM U numbers. FIGURE A-5 on page A-11 and FIGURE A-6 on page A-11 illustrate the bank numbering schemes for the motherboard and riser card, respectively.

TABLE A-4 DIMM Bank-to-U-Number Mapping

Bank	U Number (Motherboard)	U Number (Riser Card)
0	U1301 and U1302	U0301 and U0302
2	U1303 and U1304	U0303 and U0304
1	U1401 and U1402	U0401 and U0402
3	U1403 and U1404	U0403 and U0404

TABLE A-5 Memory Addressing

DIMM Size/Quantity	Memory Bank	Addressing
64 Mbyte/4	0	0 x 0000.0000 to 0 x 3fff.ff00
64 Mbyte/4	1	0 x 0000.0040 to 0 x 3fff.ff40
64 Mbyte/4	2	0 x 0000.0080 to 0 x 3fff.ff80
64 Mbyte/4	3	0 x 0000.00c0 to 0 x 3fff.ffc0
256 Mbyte/4	0	0 x 0000.0000 to 0 x ffff.ff00
256 Mbyte/4	1	0 x 0000.0040 to 0 x ffff.ff40
256 Mbyte/4	2	0 x 0000.0080 to 0 x ffff.ff80
256 Mbyte/4	3	0 x 000.00c0 to 0 x ffff.ffc0

A.3.1.1 Memory System Timing

The QSC ASIC generates the memory address and control signals to the memory system. The UPA clock is the clock source for the QSC ASIC and operates at up to 120MH.z

A.4 Peripherals

The following peripherals are supported by the system:

- Hard Disk Drive
- CD-ROM Drive (optional)
- Tape Drive (optional)

The system unit supports up to four fixed disk drives. An optional CD-ROM drive and 4mm tape drive are also supported.

A.4.1 Hard Disk Drives

The system unit supports four UltraSCSI disk drives with a capacity of 18 Gbyte.

All disk drives have a 3.5in form factor and a single connector configuration.

A spud bracket is used to mount the drive in its own dedicated slot in the front of the system. TABLE A-6 lists the supported disk drives.

- The *18Gb Disk Drive Specifications* (part number 806-1057-10), provides installation instructions, power requirements and performance data for the 18Gbyte disk drive.

TABLE A-6 Supported Disk Drive

Form Factor Dimension	Disk Drive Capacity	Wide	RPM	Seek Time
3.5in (88.9mm)	18Gbyte	Yes	10,000	8.5ms

A.4.2 Optional CD-ROM Drive

The CD-ROM drive is a standard device with multimedia features. This includes multi-session capability and fast access (32x) for image and video data. The CD-ROM drive dimensions are 149.5mm (5.94in.) x 196mm (7.78in.) x 43mm (1.71in.) and the drive slot is a standard 1.6-in (40.64-mm) bay that uses industry standard bezels.

A.4.3 Optional 4mm Tape Drive

The 4mm tape drive is equipped with a single-ended SCSI controller and a 1Mbyte on-drive buffer. The DDS-3 *Tape Drive Specifications*, part number 802-7791, provides cleaning, jumper setting and tape cartridge instructions for the 4mm DDS-3 tape drive.

A.5 Parallel Port

The parallel port is supported by an IEEE 1284-compatible parallel port controller located on the SuperIO ASIC. The parallel port controller is an industry standard controller that supports the ECP protocol and achieves a 2Mbps data transfer rate. The parallel port controller interface also supports:

- **Centronics** – Provides a widely accepted parallel port interface
- **Compatibility** – Provides an asynchronous, byte-wide forward (host to peripheral) channel with data and status lines used according to their original definitions
- **Nibble mode** – Provides an asynchronous, reverse (peripheral-to-host) channel, under control of the host. Data bytes are transmitted as two sequential, four-bit nibbles using four peripheral-to-host status lines

A.5.1 Parallel Port Cables

The parallel port cable is IEEE1284 compliant and consists of 18 pairs of signal wires that are double shielded with braid and foil. The maximum length of the parallel port cable is 2meters.

A.5.2 Electrical Characteristics

Drivers operate at a nominal 5VDC transistor-transistor logic (TTL) levels. The maximum open circuit voltage is 5.5VDC and the minimum is –0.5VDC. A logic high-level signal is at least 2.4VDC at a source current of 0.32mA and a logic low-level signal is no more than 0.4VDC at a sink current of 14mA.

Receivers also operate at a nominal –5VDC TTL levels and can withstand peak voltage transients between –2VDC and 7VDC without damage or improper operation. The high-level threshold is less than or equal to 2.0VDC and the low-level threshold is at least 0.8VDC. Sink current is less than or equal to 0.32mA at 2.0VDC and source current is less than or equal to 12mA at 0.8VDC.

A.6 Serial Ports

The system unit incorporates two serial ports, each of which is synchronous and asynchronous with full modem controls. All serial port functions are controlled by a serial port controller that is electrically connected to the system through the EBus. Line drivers and line receivers control the serial port signal levels and provide RS232 and RS423 compatibility. Each serial port interfaces through its own DB-25 connector.

The major features of each serial port include:

- Two fully-functional synchronous and asynchronous serial ports
- DB-25 connectors
- Increased baud (to 384Kbaud synchronous, 460.8Kbaud asynchronous)
- Variable edge rate for greater performance
- EBus interface

FIGURE A-7 shows a functional block diagram of the serial ports.

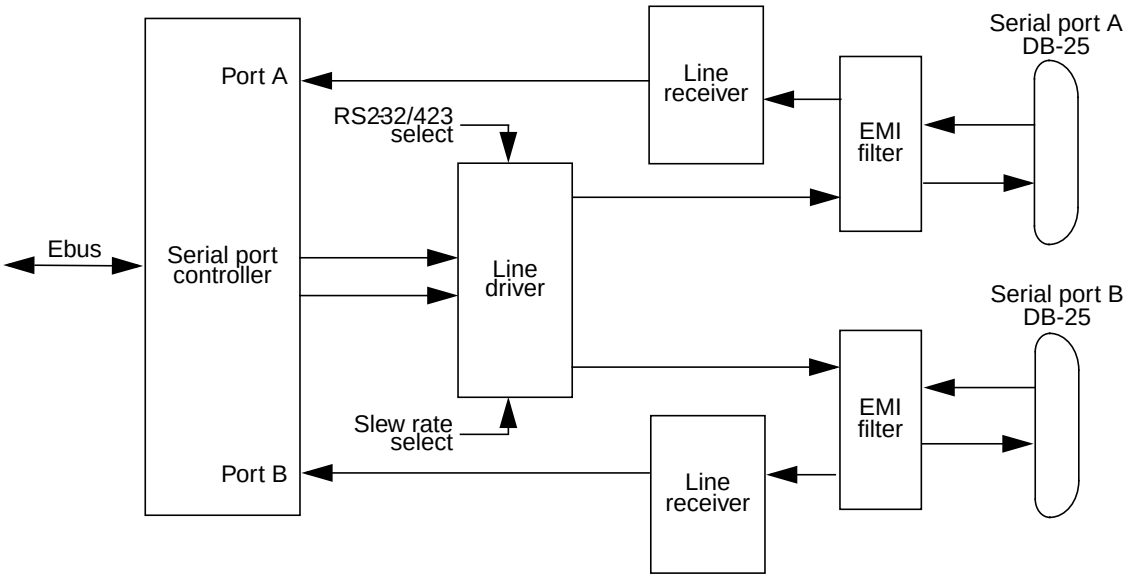


FIGURE A-7 Serial Port Functional Block Diagram

A.6.1 Serial Port Components

Serial port components include a serial port controller, line drivers and the line receivers.

The serial port controller contains 64-byte buffers on both the input and output. This enables the serial port to require less CPU bandwidth. Interrupts are generated when the buffer reaches 32 bytes or half full. The serial port controller contains its own crystal oscillator that supports up to 921.6Kbaud.

The line drivers and line receivers are compatible with both RS232 and RS423. Two system board jumpers are used to set the line drivers and line receivers to either RS232 or RS423 protocols. The line driver slew rate is also programmable. At 100Kbaud or more, the slew rate is set to 10VDC/µs. At less than 100Kbaud, the slew rate is set to 5VDC/µs.

A.6.2 Serial Port Functions

The serial port provides a variety of functions. Modem connection to the serial port enables access to the internet. Synchronous X.25 modems are used for telecommunications in Europe. An ASCII text window is accessible through the serial port on non-graphic systems.

Low speed printers, buttonboxes (for CAD/CAM applications), and devices that function like a mouse are also accessible through the serial port.

The additional speed of the serial port can be used to execute communications with a CSU/DSU for a partial T1 line to the internet at 384Kbaud.

A.6.3 EIA Levels

Each serial port supports both RS-232 and RS-423 protocols. RS-232 signaling levels are between –3VDC and –15VDC and +3VDC and +15VDC. A binary 1 (001_2) is anything greater than +3VDC and a binary 0 (000_2) is anything less than –3VDC. The signal is undefined in the transition area between –3VDC and +3VDC. The line driver switches at –10VDC and +10VDC with a maximum of –12VDC and +12VDC in RS-232 mode.

RS-423 is similar except that signaling levels are between –4VDC and –6VDC and +4VDC and +6VDC. The line driver switches at –5.3VDC and +5.3VDC with a maximum of –6VDC and +6VDC.

Switching from RS-232 to RS-423 protocol is accomplished by changing jumpers J2604 and J2605. Jumper positions 1 and 2 are for RS-232 and jumper positions 2 and 3 are for RS-423 (see Chapter 12 “Motherboard Jumpers”).

The preferred signaling protocol is RS-423. The higher voltages of RS-232 make it difficult to switch at the higher baud rate. The maximum rate for RS232 is approximately 64Kbaud while the maximum rate for RS423 is 460.8Kbaud.

The system default is set to RS-232.

A.6.3.1 Synchronous Rates

The serial synchronous ports operate between 50Kbaud and 256Kbaud when the clock is generated from the serial port controller. When the clock is generated from an external source, the synchronous ports operate at up to 384Kbaud. Clock generation is accurate within 1 percent for any rate that is generated between 50Kbaud and 256Kbaud.

A.6.3.2 Asynchronous Rates

The serial asynchronous ports support twenty rates that are all exact divisors of the crystal frequency (with exception of 110, which is off by less than 1 percent). Rates include 50, 75, 110, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200, 38400, 57600, 76800, 115200, 153600, 230400, 307200 and 460800 baud.

A.6.3.3 Slew Rate and Cable Length

The maximum RS-423 cable length is 118 feet (30 meters) and the maximum RS-232 cable length is 50 feet (15.24 meters). The slew rate changes depending on the speed. For speeds less than 100 Kbaud, the slew rate is set at 5 VDC/µs. For speeds greater than 100 Kbaud, the slew rate is increased to 10 VDC/µs. This allows maximum performance for the greater baud rate and better signal quality at the lesser baud rate.

A.7 Ethernet

The system unit supports 10 Mbps, 10BASE-T, twisted-pair Ethernet and 100 Mbps, 100BASE-T. Twisted-pair Ethernet is provided through an 8-pin RJ45 connector.

The Ethernet circuitry design is based on a Quality Semiconductor PHY.

The PHY chip integrates a 100BASE-T physical coding sub-layer (PCS) and a complete 10BASE-T module in a single chip.

The 100BASE-X portion of the PHY IC consists of the following functional blocks:

- Transmitter
- Receiver
- Clock generation module
- Clock recovery module

The 10BASE-T section of the PHY IC consists of the 10Mbps transceiver module with filters.

The 100BASE-X and 10BASE-T sections share the following functional characteristics:

- PCS control
- IEEE 802.3u auto negotiation

The following sections provide brief descriptions of the following:

- Automatic negotiation
- Connectors

A.7.1 Automatic Negotiation

Automatic negotiation controls the cable when a connection is established to a network device. It detects the various modes that exist in the linked partner and advertises its own abilities to configure automatically the highest performance mode of inter-operation, namely, 10BASE-T, 100BASE-TX, or 100BASE-T4 in half- and full-duplex modes.

The Ethernet port supports automatic negotiation. At power up, an on-board transceiver advertises 100BASE-TX in half-duplex mode, which is configured by the automatic negotiation to the highest common denominator based on the linked partner.

A.7.1.1 External Cables

The RJ45 Ethernet port supports a Category 5 UTP cable for the 100BASE-T, and a Category 3, 4, or 5 UTP cable for the 10BASE-T operation.

Note – The maximum cable segment lengths for the 100BASE-TX and 10BASE-TX are 109 yards (100 meters) and 1094 yards (1000 meters), respectively.

A.8 Alarms Subsystem

The Alarms subsystem comprises:

- Alarms Card, incorporating a LOMlite lights out management module
- LED printed circuit board

A.8.1 Alarms Functionality

The Alarms Card interfaces with the motherboard through an EBus edge connector slot. A PCI-style bracket attached to one edge provides the external interfaces at the rear of the chassis. Internal interfaces provide connections to the power supply assembly and to the LED pcb on the front panel.

The alarms subsystem provides the following functionality:

- Serial interface
- Host watchdog
- Status inputs
  Power inlet and output rail monitoring for three PSUs
- Front panel indicators
  - Front panel fault indicator
  - Three configurable alarm relays with front panel indicators
  - Two power inlet front panel indicators
- Power control
  On and standby outputs
- Fan monitors
  Speed monitoring of four fans

A.8.1.1 Light-Out Management Module

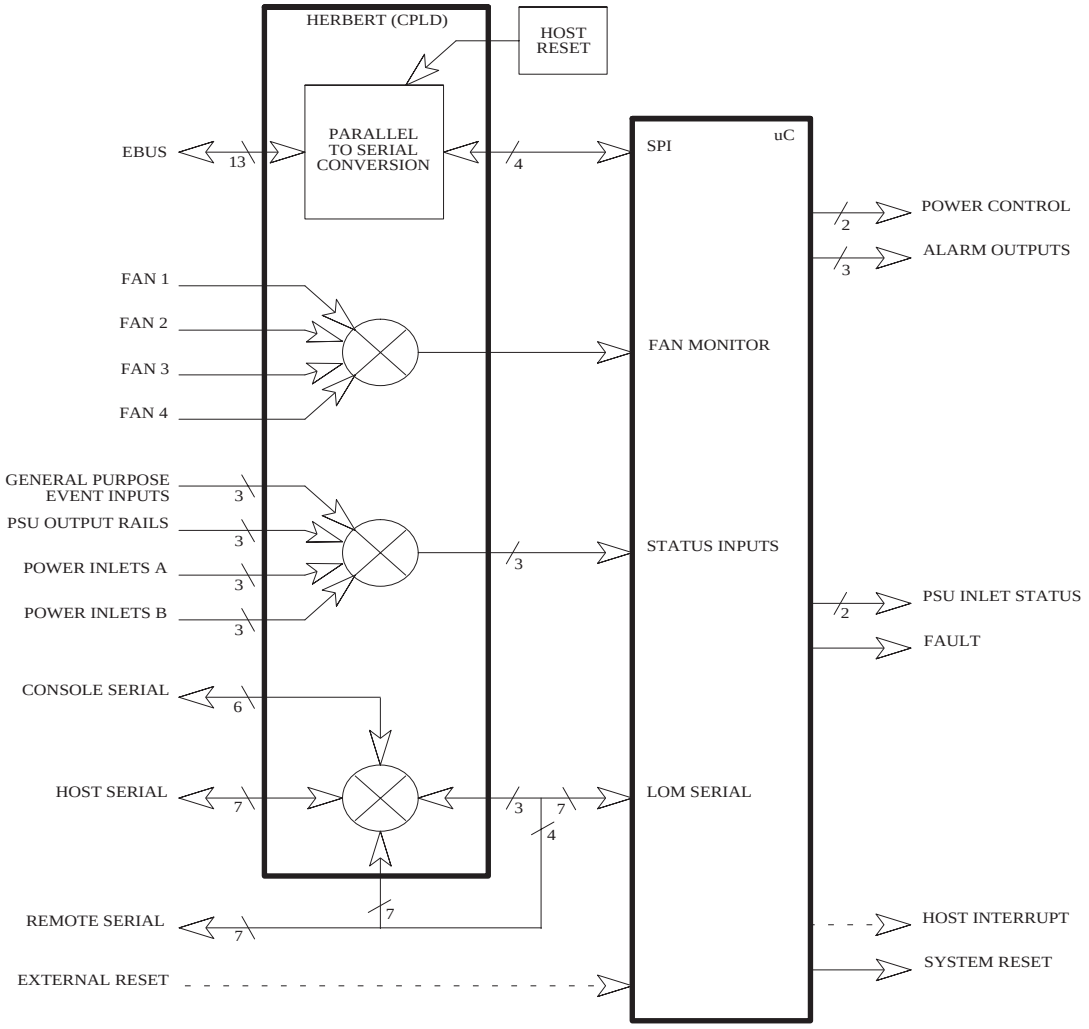


FIGURE A-8 LOMlite Functional Block Diagram

A.8.1.2 EBus Connector

The Alarms Card interfaces with the motherboard through an EBus edge connector (AMP Connector Assembly, Dual Position, 0.050 Series, Standard Edge. Amp Part No. 650090-7). TABLE A-7 lists the Ebus Connector pinout.

TABLE A-7 Ebus Connector Pinout

Pin	Signal Name	I/O	Description
1	GND		0V return
2	GND		0V return
3-5			Not used
6	GND		0V return
7	GND		Ground
8-11			Not used
12	GND		Ground
13			Not used
14	GND		0V return
15	EB_ADR6	Input	EBus address bit 6
16	EB_ADR7	Input	EBus address bit 7
17	GND		0V return
18	EB_ADR5	Input	EBus address bit 5
19	EB_ADR4	Input	EBus address bit 4
20	EB_ADR3	Input	EBus address bit 3
21	EB_ADR2	Input	EBus address bit 2
22	EB_ADR1	Input	EBus address bit 1
23	EB_ADR0	Input	EBus address bit 0
24	VCC		Host + 5V supply rail
25	PROM_CS	Input	EBus Fcode PROM chip select
26			Not used
27	LOM_CS	Input	EBus LOM chip select
28			Not used
29	GND		0V return
30	EB_WR	Input	EBus write strobe
31	EB_DAT6	Bidirectional	EBus data bit 6

TABLE A-7 Ebus Connector Pinout *(Continued)*

Pin	Signal Name	I/O	Description
32	EB_RD	Input	EBus read strobe
33	EB_DAT4	Bidirectional	EBus data bit 4
34	EB_DAT7	Bidirectional	EBus data bit 7
35	EB_DA‘T2	Bidirectional	EBus data bit 2
36	EB_DAT5	Bidirectional	EBus data bit 5
37	EB_DAT0	Bidirectional	EBus data bit 0
38	EB_DAT3	Bidirectional	EBus data bit 3
39	GND		0V return
40	EB_DAT1	Bidirectional	EBus data bit 1
41			Not used
42	GND		0V return
43			Not used
44	CFRQ		Not used (grounded)
45			Not used
46	PDRQ		Not used (grounded)

A.8.1.3 Power Supply Interface

The power supply interface supplies the Alarms Card with the standby supply rail together with power supply status information, system fan monitoring signals and access to power control signals. TABLE A-8 lists the connector pinout:

TABLE A-8 Power Supply Interface Connector Pinout

Pin	Signal Name	I/O	Description
1	FAN1	Input	Fan1 tacho
2	FAN2	Input	Fan2 tacho
3	FAN3	Input	Fan3 tacho
4	FAN4	Input	Fan4 tacho
5	INA3	Input	PSU 3 inlet A present
6	INB3	Input	PSU 3 inlet A present
7	OUT3	Input	PSU 3 outputs present

TABLE A-8 Power Supply Interface Connector Pinout *(Continued)*

Pin	Signal Name	I/O	Description
8	INA2	Input	PSU 2 inlet A present
9	INB2	Input	PSU 2 inlet A present
10	OUT2	Input	PSU 2 outputs present
11	INA1	Input	PSU 1 inlet A present
12	INB1	Input	PSU 1 inlet A present
13	OUT1	Input	PSU 1 outputs present
14	AVCC		Standby +5V supply rail
15	GND		0V return
16	RST	Bidirectional	PSU/system reset
17	STBY	Bidirectional	Host power-down
18	ON	Bidirectional	Host power-up

A.8.1.4 LED Card Interface

The Alarms Card provides the system interface to the LED card which comprises outputs to front panel indicators and inputs from the front panel switch. TABLE A-9 lists the pinout.

TABLE A-9 LED Card Interface Connector Pinout

Pins	Signal Name	I/O	Description
1	VCC		Host +5V supply rail
2	FAULT	Output	Fault output
3	LED1	Output	Alarm 1 indicator
4	LED3	Output	System alarm indicator
5	LED2	Output	Alarm 2 indicator
6	GND		0V return
7	SUPA	Output	Supply active indicator
8	STBY	Bidirectional	Host power-down
9	SUPB	Output	Supply B active indicator
10	ON	Bidirectional	Host power-up

A.8.1.5 External Ports

For details of the pinout for the external LOM serial port and the alarms service port, see Section 10.6 “Alarms Ports” on page 10-10.

A.9 SCSI

The system unit implements a small computer system interface (SCSI) UltraSCSI (Fast-20) parallel interface bus. The UltraSCSI is based on the SCSI-3 parallel interface and provides the following:

- Efficient peer-to-peer I/O bus devices
- Definition of the mechanical, electrical, and timing specification to support transfer rates of 20, 40, or 80 Mbyte/s corresponding to the data path width of an 8-, 16-, or 32-bit bus, respectively
- Peak bandwidth of 40 Mbyte/s (with implemented 16-bit bus width)

UltraSCSI is also called Fast-20 SCSI and the two names are used synonymously.

The SCSI subsystem is based upon single-ended UltraSCSI using a 16-bit-wide bus. UltraSCSI, having an implemented 16-bit bus width, supports a peak bandwidth of 40 Mbps.

The maximum cumulative signal path length between terminators is 3 meters when connecting up to four external devices (one host initiator and three targets). The maximum cumulative signal path length between terminators is 1.5 meters when using from five to eight external devices (one host initiator and four to seven targets).

The system incorporates a dual-channel host adapter. One channel is used exclusively to provide an internal SCSI bus, and the second provides the external SCSI bus. The internal bus is terminated at one end on the motherboard and at the other on the CD-ROM adapter. The external bus is terminated at the host adapter and at the 68-pin external connector. Connecting an external device disables the on-board terminators near the 68-pin connector to extend the bus and allowing the last external device to provide the termination. FIGURE A-9 shows the SCSI bus configuration.

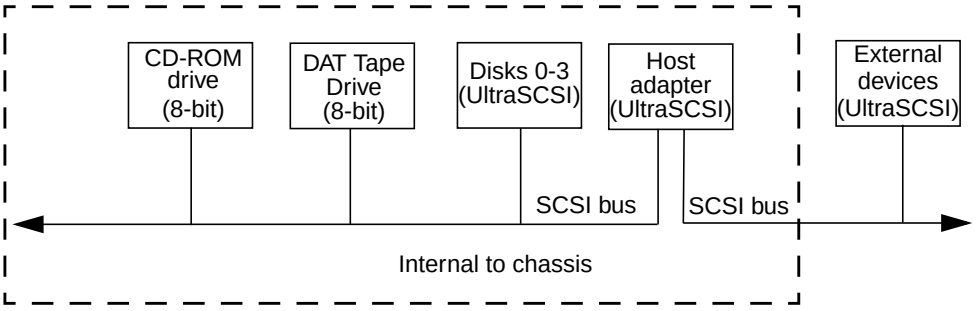


FIGURE A-9 Configuration of the SCSI Bus

A.9.1 Host Adapter

The host adapter is a dual-channel Symbios 53C876 PCI-SCSI I/O processor IC. The host adapter and all target devices comply with the UltraSCSI single-ended drivers and receivers characteristics. The electrical characteristics of the output buffers include:

- V_{OL} (output low) equals 0 to 0.5VDC with Iol at 48mA (signal asserted)
- V_{OH} (output high) equals 2.5 to 3.7VDC (signal negated)
- t_{rise} (rising slew rate) equals 520 mV/nanosecond maximum (0.7 to 2.3VDC)
- t_{fall} (falling slew rate) equals 520mV/nanosecond maximum (2.3 to 0.7VDC).

The UltraSCSI electrical characteristics for the host adapter and target device include:

- V_{IL} (input low) equals 1.0VDC maximum (signal true)
- V_{IH} (input high) equals 1.9VDC minimum (signal false)
- I_{IL} (input low current) equals ±20µA at V_i equals 0.5VDC
- I_{IH} (input high current) equals ±20µA at V_i equals 2.7VDC
- Minimum input hysteresis equals 0.3VDC

A.9.2 Supported Target Devices

The SCSI subsystem supports a maximum of four internal devices, including the host adapter. A unipack with one drive or a six-pack, accommodating six drives, can be used as external devices.

A.9.3 External Cables

External UltraSCSI compliant SCSI cables are an extension of the existing shielded cables but have a impedance of 90Ω (±6Ω). UltraSCSI requires that the total SCSI bus length be limited to 3 meters for less than five devices and 1.5 meters for five to eight devices.

A.9.4 Internal SCSI Subassembly

The internal SCSI subassembly consists of two cable assemblies and two SCSI cards. The SCSI subassembly is attached to the motherboard using an insulation displacement connector (IDC) receptacle attached to an 80-conductor cable. The IDC receptacle mates with a right angle plug mounted on the motherboard in close proximity to the test edge connector.

The other end of the 80-conductor cable is hard-wired to the SCSI backplane. The SCSI backplane incorporates four SCA-2 connectors for mounting the hard drives and a four-circuit power connector to supply 5VDC and 12VDC power to the hard drives.

A 68-conductor cable exits the SCSI backplane carrying 27 SCSI signals and the Termpower to the internal SCSI adaptor card. The upper nine bits are terminated at the SCSI adapter and the lower 18 bits are carried to the CD-ROM and DAT Tape drives. The signals then return to the SCSI adaptor where the lower 9 bits and 9 control bits are terminated.

A.9.5 SCSI ID Selection

The SCSI devices are allocated ID addresses according to the following table:

TABLE A-10 SCSI ID Allocation

SCSI Device	ID
Controller	7
Disk 0	0
Disk 1	1
Disk 2	2
Disk 3	3
Tape	4
CD-ROM	6

A.10 ASICs

The system unit achieves a high level of integration through application-specific integrated circuits (ASICs). All ASICs are 1149.1 (JTAG) compliant. The ASICs are:

- QSC
- XB9++
- PCI-to Ebus/Ethernet controller (PCIO)
- UPA-to-PCI bridge (U2P)
- Reset, interrupt, scan and clock (RISC)

Also included in this section is a brief discussions of the SuperIO component.

A.10.1 QSC

The QSC ASIC provides system control. It controls the UPA interconnect between the major system unit components and main memory. The QSC ASIC provides the following:

- Interconnect packet receive
- Memory arbiter
- Non-cached arbiter
- Memory controller
- Snoop interface
- Coherence controller
- S_register dispatcher
- Internet packet send
- Datapatch scheduler
- EBus interface

A.10.2 XB9++

The XB9++ ASIC is a buffered memory crossbar device that acts as the bridge between the six system unit buses. The six system unit buses include two processor buses, a memory data bus and two I/O buses. The XB9++ ASIC provides the following:

Note – Referred data formats are as follows: a byte is 8bits, a halfword is 16bits, a word is 32bits, and a doubleword is 64bits.

- Six-port crossbar
- Decoupled memory port; loading and unloading of memory data can take place in parallel with other operations
- Burst transfers operate on a doubleword of data per slice
- A total of eight two-entry first-in-first-out (FIFO) devices for read data storage
- Power-up safe buses (tristated)

A.10.3 PCIO

The PCI-to-Ebus/Ethernet controller (PCIO) ASIC performs dual roles: PCI bus-to-Ebus bridging and Ethernet control. The PCIO ASIC provides the electrical connection between the PCI bus and all other I/O functions. In addition, the PCIO ASIC also contains an embedded Ethernet controller that manages Ethernet transactions and provides the electrical connection to slower on-board functions, such as the Flash PROM and the alarms module.

A.10.4 U2P

The UPA-to-PCI bridge (U2P) ASIC provides an I/O connection between the UPA bus and the two PCI buses. The U2P ASIC features include:

- Full master and slave port connection to the high-speed UPA interconnect. The UPA is a split address/data packet-switched bus that has a potential data throughput rate greater than 1Gbyte per second. UPA data is ECC protected.
- Two physically separate PCI bus segments with full master and slave support:
  - 66MHz PCI bus segment (PCI bus A): 3.3VDC signalling, 64-bit data bus, compatible with the PCI 66MHz extensions, support for up to four master devices (at 33MHz only)
  - 33MHz PCI bus segment (PCI bus B): 5.0VDC signaling, 64-bit data bus, support for up to six master devices
- Two separate 16-entry streaming caches, one for each bus segment, for accelerating some kinds of PCI DVMA activity. Single IOMMU with 16-entry TLB for mapping DVMA addresses for both bus (IOMMU used to translate 32- or 64-bit PCI addresses into 41-bit UPA addresses)
- A mono-vector dispatch unit for delivering interrupt requests to the CPU module, including support for PCI interrupts from up to six slots, as well as interrupts from on-board I/O devices

A.10.5 RISC

The reset, interrupt, scan, and clock (RISC) ASIC implements those four functions. Generation and stretching of the reset pulse is performed in this ASIC. Interrupt logic concentrates 42 different interrupt sources into a 6-bit code that communicates with the U2P ASIC. It also integrates a JTAG controller.

The RISC ASIC features include:

- Determination of system clock frequency
- Control of reset generation
- Provision of JTAG
- Performance of PCI bus and miscellaneous interrupt concentration for U2P
- Control of flash PROM programming, frequency margining and lab console operation
- 33-MHz operation
- 160-pin MQFP package
- 3.3VDC and 5VDC supply voltage

A.10.6 SuperIO

The SuperIO is a commercial off-the-shelf component that contains two serial port controllers for keyboard and mouse, an IEEE 1284 parallel port interface and an IDE disk interface (not used). The SuperIO drives the various ports directly with some EMI filtering on the keyboard and parallel port signals. Support for mixed voltage modes and power management features are also included.

A.11 Power Subsystem

The Power subsystem comprises the three (n+1 redundancy) Power Supply Units (PSU) and the Power Distribution Assembly (PDA).

The PDA consists of a cage that houses the PSUs and the Power Distribution Board (PDB).

A.11.1 Netra t 1400

The Netra t 1400 uses 330W DC-DC power supplies that operate in the range –40VDC to –75VDC. The maximum input current at –40VDC is 17.1A and the inrush current is limited to $20 A_{peak}$.

Each PSU has dual dc inputs and current is shared between the two inputs via a diode commoning arrangement

The power supply continues to regulate all outputs for approximately 5ms after removal of the dc input. Power supply output voltages are listed in TABLE A-11.

TABLE A-11 DC PSU Power Supply Output Voltages

Output	Voltage (VDC)	Max. Current (A)	Regulation Band
1	3.3	49.5	3.23 to 3.43
2	5.0	38.5	4.85 to 5.25
3	12	6.6	11.65 to 12.60
4	–12	0.4	–12.6 to –11.4
5	5.0	1.0	4.75 to 5.25

Note – The combined power of output 1 and output 2 does not exceed 300 W.

A.11.2 Netra t 1405

The Netra t 1405 uses 330W AC-DC power supplies that operate within the following input voltage and frequency range:

TABLE A-12 AC PSU Operating Voltage and Frequency Range

	Minimum	Maximum
Voltage	90 V_{rms}	264 V_{rms}
Frequency	47 Hz	63 Hz

The maximum inrush current is limited to 80 A_{peak} on restart or after the power has been removed for 60s or longer.

The power supply continues to regulate all outputs for approximately 10ms after ac power is removed. Power supply output voltages are listed in TABLE A-13.

TABLE A-13 AC PSU Power Supply Output Voltages

Output	Voltage (VDC)	Max. Current (A)	Regulation Band
1	3.3	49.5	3.23 to 3.43
2	5.0	38.5	4.85 to 5.25
3	12	6.6	11.65 to 12.60
4	–12	0.4	–12.6 to –11.4
5	5.0	0.25	4.75 to 5.25

Note – The combined power of output 1 and output 2 does not exceed 300 W.

A.11.3 Power Distribution Board

The power distribution board (PDB) distributes power between the power supplies and the rest of the system and enables hot-plugging of the PSUs.

A.11.3.1 PDB Connectors

TABLE A-14 to TABLE A-19 give the pinout for the PDB connectors.

TABLE A-14 PDB Interface Connector (P1, P2 and P3) Pinout

Pin	Signal	Pin	Signal
1	3.3V	25	
2	3.3V	26	
3	3.3V	27	5V share
4	3.3V	28	
5	3.3V	29	3.3V share
6	RTN	30	+12V
7	RTN	31	+12V
8	RTN	32	+12V
9	RTN	33	12V

TABLE A-14 PDB Interface Connector (P1, P2 and P3) Pinout *(Continued)*

Pin	Signal	Pin	Signal
10	RTN	34	
11	RTN	35	5V sbs
12	RTN	36	5V sense
13	RTN	37	PSU*n*[1] ON/L
14	RTN	38	12V
15	+5V	39	PSU*n*[1] OK
16	RTN	40	Reset /L
17	+5V	41	IN A*n*[1] OK
18	+5V	42	Fault/
19	+5V	43	12V share
20	+5V	44	IN B*n*[1] OK
21	3.3V sen RTN	45	
22	PSU *n*Con[1]	46	
23	3.3V sense	47	
24	5V sen RTN		

1. *n* = 1, 2 or 3, corresponding to P1, P2 or P3.

TABLE A-15 Motherboard Power Services Interface Connector (J4) Pinout

Pin	Signal	Pin	Signal
1	ON	8	POR/L
2	-12V	9	
3	+5V sen rtn	10	+5V sen
4	+3.3V sen rtn	11	+3.3V sen
5	RTN	12	+12V
6	RTN	13	+12V
7	not used	14	+5V sbs

TABLE A-16 Motherboard Power Supply Interface Connector (J5) Pinout

Pin	Signal	Pin	Signal
1	+3.3V	8	+3.3V RTN
2	+3.3V	9	+3.3V RTN
3	+3.3V	10	+3.3V RTN
4	+3.3V	11	+3.3V RTN
5	+5V	12	+5V RTN
6	+5V	13	+5V RTN
7	+5V	14	+5V RTN

TABLE A-17 Alarms Card Interface Connector (J6) Pinout

Pin	Signal	I/O	Description
1	FAN1	Output	Fan 1 tacho
2	FAN2	Output	Fan 2 tacho
3	FAN3	Output	Fan 3 tacho
4	FAN4	Output	Fan 4 tacho
5	INA3	Output	PSU 3 input A present
6	INB3	Output	PSU 3 input B present
7	OUT3	Output	PSU 3 outputs present
8	INA2	Output	PSU 2 input A present
9	INB2	Output	PSU 2 input B present
10	OUT2	Output	PSU 2 outputs present
11	INA1	Output	PSU 1 input A present
12	INB1	Output	PSU 1 input B present
13	OUT1	Output	PSU 1 outputs present
14	AVCC		Standby +5V supply rail
15	GND		0V return
16	RST	Bidirectional	PSU/system reset
17	STBY	Bidirectional	Host power-down
18	ON	Bidirectional	Host power-up

TABLE A-18 SCSI Subassembly Interface Connector (J10) Pinout

Pin	Signal	Pin	Signal
1	+12V	3	RTN
2	RTN	4	+5V

TABLE A-19 Fans Control Board Interface Connector (J11) Pinout

Pin	Signal	Pin	Signal
1	+12V	5	Fan T1
2	+12V	6	Fan T3
3	RTN	7	Fan T2
4	RTN	8	Fan T4

APPENDIX **B**

Illustrated Parts List

This appendix lists the authorized replaceable parts for the Netra t 1400/1405 system unit. FIGURE B-1is an exploded view of the system unit with numerical references correlating to the replaceable components listed in TABLE B-1 and TABLE B-2. A brief description of each listed component is also given.

The part numbers listed in TABLE B-1 and TABLE B-2 are correct at the time of publication of this manual, but are subject to change without notice. Consult your authorized Sun sales representative or service provider to confirm a part number before ordering the replacement part.

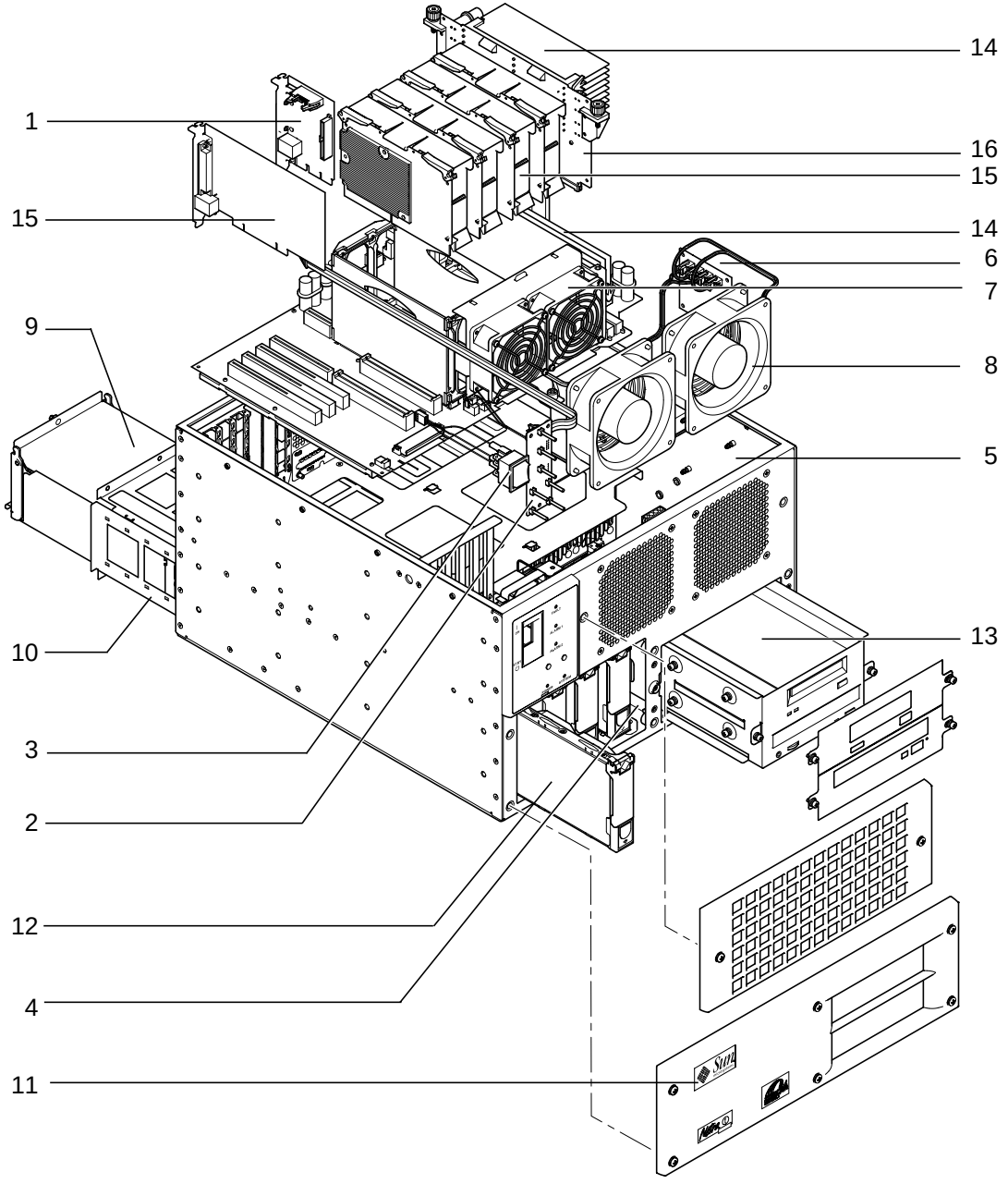


FIGURE B-1 Exploded View of the Netra t 1400/1405 System Unit

TABLE B-1 Netra t 1400/1405 Field Replaceable Components

Ref	FRU Number	Description
1	F501-5437	Alarms card
2	F501-5560	LED card with alarms card and motherboard cables
3	F530-2514	Switch and integral cable
4	F540-4311	Disk-bay assembly with SCSI backplane, cables and screws
5	F501-5125	SCSI adapter for removable media bay, with power and SCSI cables
6	F501-5561	Fan control board
7	F540-4262	CPU fan assembly with integral cables
8	F370-3976	Front system fan with integral cable (two required)
9	F300-1434	AC PSU for Netra t 1405
9	F300-1435	DC PSU for Netra t 1400
10	F370-3920	Power subframe and power distribution board assembly
	F565-1639	Set of five cables
16	F501-5218	Memory riser card
	F501-5168	Motherboard
	F300-1407	DC-to-DC Converter

TABLE B-2 Netra t 1400/1405 Optional Components

Ref	Component Number	Description
11	X7076A	Fascia kit for Netra t 1400/1405, including AC and DC badges
12	X-5237A	18GByte 10K hard disk drive
13	X-6911A	32x CD-ROM drive (lower)
13	X6912A	DDS-3 tape drive (upper)
14	X-7003A	Memory (2 x 64Mbyte DIMM)
14	X-7005A	Memory (2 x 256Mbyte DIMM)
15	X-1197A	440MHz CPU
	X7075A	Air filter pack for Netra t 1400/1405
	X7077A	LOMlite CD with alarms driver, utilities and VTS extension

TABLE B-2 Netra t 1400 / 1405 Optional Components *(Continued)*

Ref	Component Number	Description
	X7071A	19-in. rack mounting kit comprising four flanges (340-5904), two handles and screws
	X7072A	23-in. rack mounting kit four flanges (340-5905), two handles and screws
	X7073A	24-in. rack mounting kit comprising four flanges (340-5906), two handles and screws
	X7074A	600-mm rack mounting kit comprising four flanges (340-5907), two handles and screws
	X6914A	Rack mount slide adapter kit comprising two slides, adapter for use in Sun rack and screws
	X949A	Pack of 10 Wago connectors and strain reliefs

APPENDIX **C**

Product Specifications

This appendix provides information concerning the physical and electrical requirements for installing the Netra t 1400 and Netra t 1405 systems.

C.1 Physical Specifications

C.1.1 Dimensions

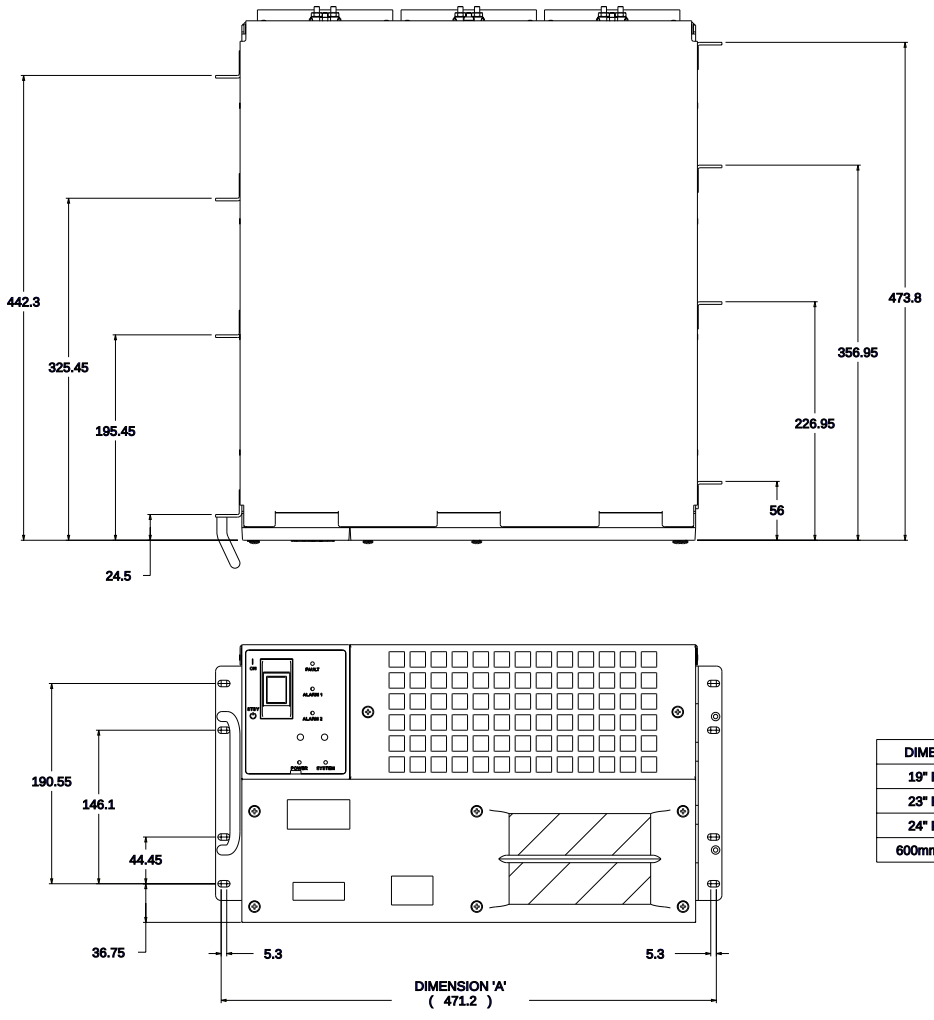
- Height: 264 mm (10.39 in.) 6U nominal
- Width: 431.8 mm (17.00 in.)
- Depth: 477.3 mm (18.79 in.)
- Weight (unpackaged): maximum 38 kg (84 lb.)

Flanges can be fitted to accommodate the equipment in 19-inch, 23-inch, 24 inch and 600-mm racks (see FIGURE C-1 on page C-2).

Caution – The Netra t 1400/1405 system, when fully loaded, can weigh up to 38 kg (84 lb.); hence mechanical assistance may be required if installing a fully-loaded unit.

C.1.2 Mounting Flanges

The Netra t 1400/1405 chassis has been designed for a wide variety of mounting options and rack sizes. One set of 19-inch flanges (four) and handles (two) is included with each system. Mounting flanges to suit 23-inch, 24-inch or 600-mm nominal frame widths can be ordered as required:



DIMENSION 'A'	
19" FLANGES	471.2
23" FLANGES	572.1
24" FLANGES	596.6
600mm FLANGES	519

FIGURE C-1 Netra t 1400/1405 Flange Options and Dimensions

Optional Components

TABLE C-1 Optional Mounting Flange Kits

Mounting Option	Part Number
19-inch configuration	X7071A
23-inch configuration	X7072A
24-inch configuration	X7073A
600-mm configuration	X7074A

FIGURE C-2 on page C-4 shows how to connect the Flange Mount assembly to the Netra t 1400/1405 system.

The system can also be mounted on telescopic slides.

An adaptor kit (part number X6914A) is available for mounting the system in a Sun 72-inch rack.

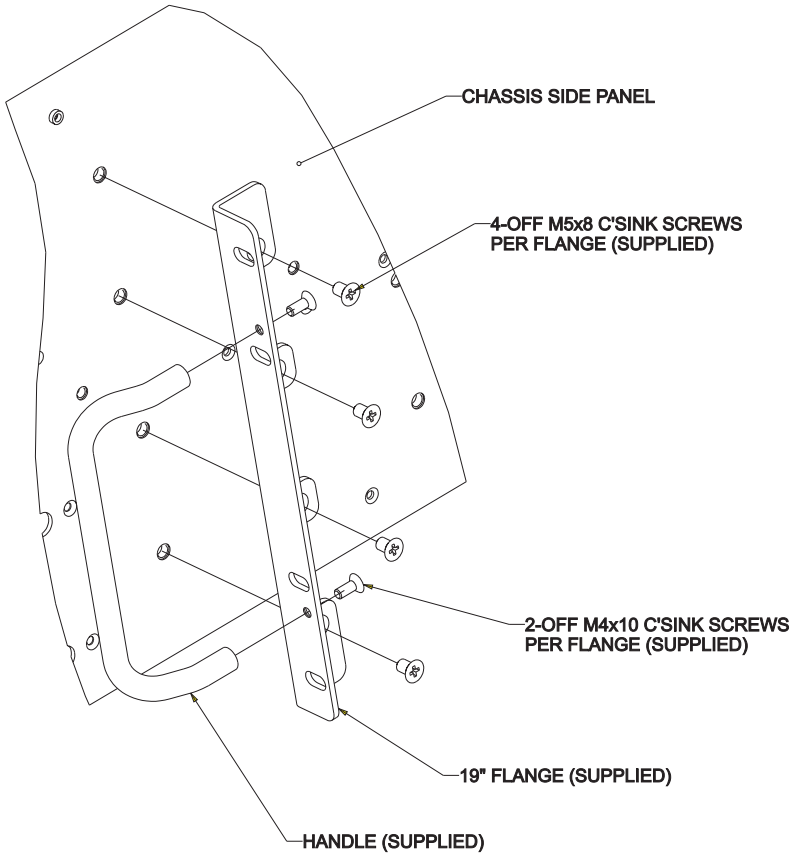


FIGURE C-2 Flange Mount Assembly

The chassis must be secured within the rack frame using screws suitable for the equipment frame. They must be a minimum size of M5 (10/32) depending on the frame requirement. All screws must be fitted; there are positions provided for a total of 16 screws (four per flange). The recommended tightening torque value for M5 recess head screws is 4.0Nm (3.0lbf-ft).

Caution – For flange mounted installations, always fit four flanges.

C.2 Electrical Specifications

This section provides information about electrical supply installation.

Note – All supply connections, wiring, wire protection, and wire routing must be made in accordance with applicable sections and requirements of national electrical code and local electrical authorities.

C.2.1 Netra t 1400 DC Source Site Requirements

TABLE C-2 DC Power Requirements[1]

Electrical Element	Requirement
Voltage	-48VDC / -60VDC
Max. operating current	10A @ -48VDC / 12A @ -60VDC
Max. inrush current	24A @ -48VDC / 30A @ -60VDC

1. The DC power supply range is -40VDC to -75VDC.

The DC source must be:

- –48VDC or –60VDC nominal centralized DC power system
- electrically isolated from any AC power source
- reliably connected to earth (that is, the battery room positive bus is connected to the grounding electrode)
- capable of providing up to 15W of continuous power per feed pair

---

Note – The DC version of your system must be installed in a *restricted access location*. Per the intent of the National Electrical Code, a restricted access location, is an area intended for qualified or trained personnel only and has access controlled by a locking mechanism, such as a key lock or an access card system.

C.2.2 Overcurrent Protection Requirements

- Overcurrent protection devices must be provided as part of each host equipment rack.
- Circuit breakers must be located between the DC power source and the Netra t 1400 system.
  - Two 15 A maximum single-pole fast trip DC rated circuit breakers (one per ungrounded supply conductor) in the negative supply conductor.
- Circuit breakers must not trip when presented with inrush current of 20 A lasting 500 ms.

Note – Overcurrent devices must meet applicable national and local electrical safety codes and be approved for the intended application.

C.2.3 Required Connection Materials

C.2.3.1 DC Branch Circuits

- Two Wago 3-position connectors with strain relief housings, one per feed pair with strain relief housings, are supplied in the shipkit with each system.

C.2.3.2 Grounding

- One Thomas & Betts two-hole lug (part number: 54204-UB) suitable for 8AWG conductor or UL / CSA approved equivalent having 5 / 8-inch pitch. Torque value: 3.5 Nm maximum. Two M5 studs and cupwasher nuts are supplied on the rear of the chassis for connection.
- A Thomas & Betts crimping tool (part number: TBM 5-S), or approved equivalent is required to secure the lug on to the cable.
- An earthing bus bar that is near the equipment and easily accessible.

Caution – External filtering and / or surge suppression devices may be required on the power feeds where branch circuit electromagnetic characteristics are unknown.

C.2.3.3 DC Supply and Ground Conductor

The requirements are:

- suitable conductor material: tinned copper only
- conductors: 14 AWG maximum (between the Netra t 1400 and circuit breaker). There are three conductors:
  - -48 VDC / -60 VDC Supply (pin 1)
  - Ground connection to power supply (pin 2)
  - -48VDC / -60 VDC Return (pin 3)
- system ground conductor: 8 AWG
- cable insulation rating: minimum 75°C, low smoke fume (LSF), flame retardant
- cable must conform to GR63CORE fire resistance requirements
- branch circuit cable insulation color: per applicable National Electrical Codes
- grounding cable insulation color: green / yellow

C.2.4 Netra t 1405 AC Source Requirements

Note – As part of the installation, overcurrent devices meeting applicable national and local electrical safety codes shall be provided.

The disconnect device for servicing is defined as any one of the following:

- the appliance inlet on the rear of the system
- the circuit breakers in the rack in which the system is mounted
- the mains plug

It must be ensured that these remain accessible after installation.

Caution – External filtering and / or surge suppression devices may be required on the power feeds where branch circuit electromagnetic characteristics are unknown.

C.2.4.1 Chassis Enclosure Grounding

- One Thomas & Betts two-hole lug (part number: 54204-UB) suitable for 8 AWG conductor or UL / CSA approved equivalent having 5 / 8-inch pitch. Torque value: 3.5Nm maximum. Two M5 studs and cupwasher nuts are supplied on the rear of the chassis for connection.
- A Thomas & Betts crimping tool (part number: TBM 5-S), or approved equivalent is required to secure the lug on to the cable.
- An earthing bus bar that is near the equipment and easily accessible.

The safety earth path is established by the connection of the grounding conductor within the AC power cord to a *reliably* earthed socket outlet located near the equipment.

C.3 Environmental Requirements

The system can be installed in an environment with the following specific parameter ranges:

- Ambient temperature
  - operating: 5˚ to 40˚C
  - exceptional operating limit: –5˚ to 55˚C[1, 2]
  - storage: –40˚ to 70˚C
- Relative humidity
  - operating: 5 to 85% non-condensing[3]
  - storage: 10 to 95% non-condensing
- Elevation
  - operating: –300 to +3000 m
  - storage: –300 to +12000 m

C.3.1 Forced Air Cooling Requirements

1. Adequate airflow through the host equipment frame must be ensured.
2. The air is drawn through the front of the Netra t 1400/1405 enclosure and expelled from the rear of the enclosure.
3. The inlet and exhaust ventilation areas must be a minimum of 200 sq. cm each.

1. Error-free operation of the removable media devices is from 0° to 40°C.
2. No more than 96 hours duration at extremes and at elevations less than 1800 m.
3. Subject to a maximum absolute humidity of 0.024 kg of water per kg of dry air.

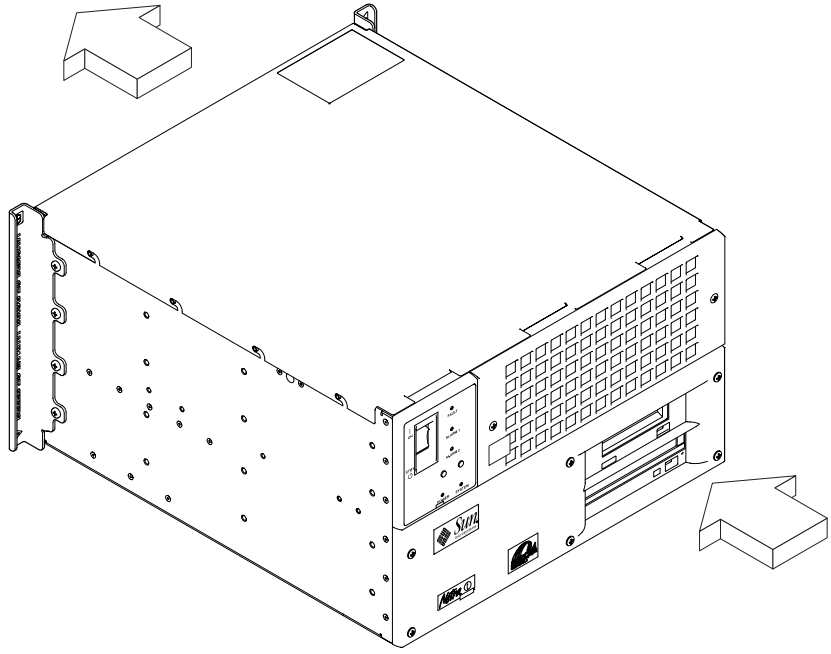


FIGURE C-3 Netra t 1400/1405 Airflow (front and rear)

4. To maintain adequate airflow we strongly recommend that you inspect and, if necessary, replace or clean the air filter on a regular basis. *See the Netra t 1400/1405 Installation and User Guide* for further information.

5. If the Netra t 1400/1405 computer system is fully enclosed by its host equipment rack, the host rack must have ventilation openings in the front door. This permits unrestricted access to an external air source.

Index

E

F

G

H

I

R

S

T

U

W

X