Netra™ T4 AC100/DC100 Service and System Reference Manual

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Preface

This manual supports the Netra T4 AC100/DC100 server and comprises two parts:

- Part I, *Service*, is written for technicians, advanced computer system end-users with experience in replacing hardware and troubleshooting, system administrators, and authorized service providers (ASPs). Only suitably qualified service personnel may carry out tasks described in this manual that involve the removal of the top cover.
- Part II, *System Reference*, is written for OEM engineers, system designers and application programmers who have to perform advanced tasks concerned with the maintenance and configuration of the system.

How This Book Is Organized

Chapter 1 provides an overview of the key features of the Netra T4 server.

Chapter 2 describes the Power-On Self-Test (POST) diagnostics.

Chapter 3 contains an overview of the SunVTS Validation Test Suite.

Chapter 4 describes how to troubleshoot and correct hardware problems.

Chapter 5 discusses the precautions you should take before working on the system, and explains how to gain access to the internal components.

Chapter 6 describes how to remove and fit the PSU and power subassemblies.

Chapter 7 describes how to remove and fit the system fans.

Chapter 8 describes how to remove and fit the system storage devices.

Chapter 9 describes how to remove and fit the motherboard and the components that interface with it.

Chapter 10 provides a functional description of the system.

Chapter 11 provides information about the I/O connectors.

Chapter 12 describes how to connect and set up a modem.

Appendix A provides an illustrated list of replaceable parts and components.

Appendix B provides a product specification.

Appendix C contains a list of tools that are needed to service the system.

Appendix D provides details of the internal motherboard connectors.

Appendix E provides an example of a typical POST diagnostic output.

Appendix F describes how to update LOMlite2 firmware.

Appendix G describes how to connect to the Netra T4 serial ports.

Typographic Conventions

Typeface	Meaning	Examples
`AaBbCc123`	The names of commands, files, and directories; on-screen computer output	Edit your `.login` file. Use `ls -a` to list all files. `% You have mail.`
`AaBbCc123`	What you type, when contrasted with on-screen computer output	`% su` `Password:`
AaBbCc123	Book titles, new words or terms, words to be emphasized	Read Chapter 6 in the *User's Guide*. These are called *class* options. You *must* be superuser to do this.
	Command-line variable; replace with a real name or value	To delete a file, type `rm` *filename*.

Shell and System Prompts

Shell	Prompt
C shell	*machine_name*%
C shell superuser	*machine_name*#
Bourne shell and Korn shell	$
Bourne shell and Korn shell superuser	#
OpenBoot PROM	ok[1]
LOMlite2	lom>

1. In dual processor systems, the processor number, 0 or 1, is included; for example, {0} ok

Related Documentation

Application	Title	Part Number
Installation User	*Netra T4 AC100/DC100 Installation and User's Guide*	806-7334-11
Compliance	*Netra T4 AC100/DC100 Compliance and Safety Manual*	806-7335-11
OpenBoot PROM	*OpenBoot 3.x Command Reference* *OpenBoot PROM Quick Reference*	806-1377-10 806-2908-10

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PART I Service

CHAPTER 1

System Description

This chapter lists the main features of the Netra™ T4 AC100/DC100 server, and describes the function of the LEDs located on the front and rear panels.

The chapter contains the following sections:

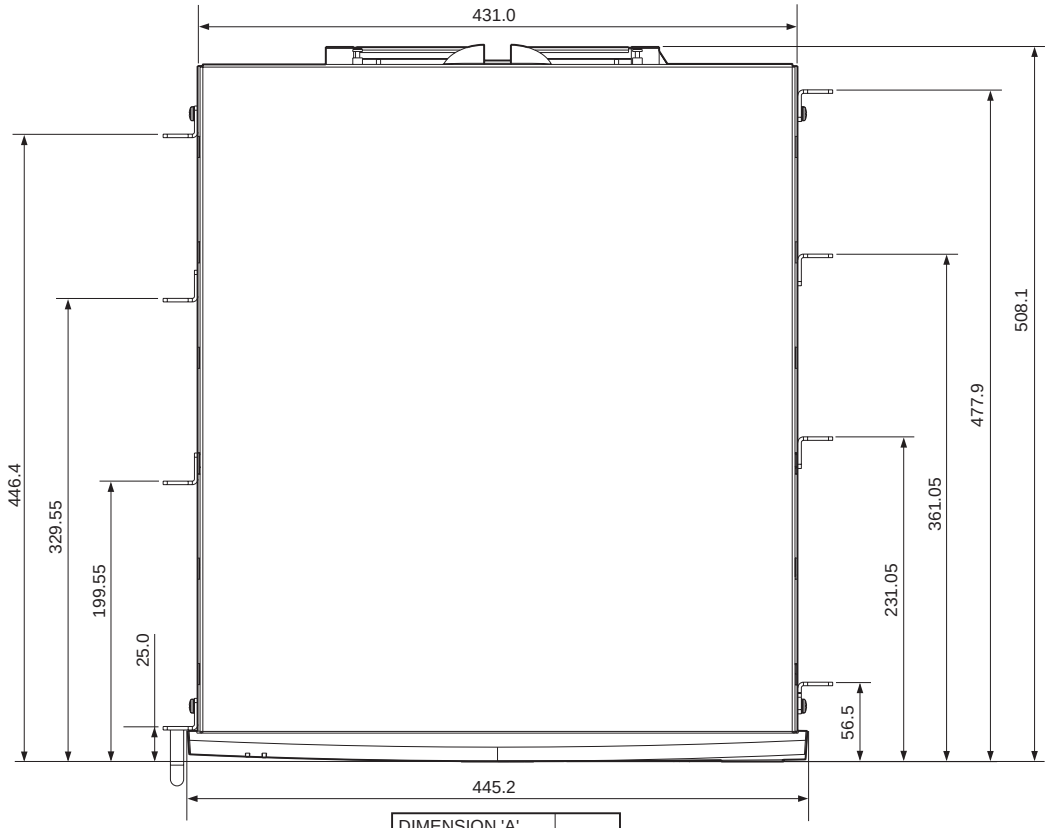
- Section 1.1, “System Features” on page 1-1
- Section 1.2, “System Unit Components” on page 1-5
- Section 1.3, “Environmental Performance” on page 1-5
- Section 1.4, “LEDs” on page 1-6

The Netra T4 server is a single or dual processor device that uses the UltraSPARC™ III processor.

- High performance processors
- High performance disk, system, memory and I/O subsystems
- High performance peripheral component interconnect (PCI) I/O
- Rack mounting options
- Front-to-back cooling
- AC and DC power supply options
- Alarms functionality for remote management
- System configuration card
- Hot swap disk drives
- Visual diagnostics
- Environmental monitoring

1.1 System Features

System unit components are housed in a 4RU rack-mounting enclosure designed to NEBS Level 3 standards. Overall chassis dimension (width x depth x height) are 445.2 mm x 508.1 mm x 176.6 mm (17.52 in. x 20.00 in. x 6.95 in.). Flange mounting kits are available for installing the system in 19-inch, 23-inch, 24-inch and 600-mm racks (see FIGURE 2-1). A slide adaptor kit is also available.



DIMENSION 'A'	
19 in. FLANGES	470.4
23 in. FLANGES	561.3
24 in. FLANGES	595.8
600mm FLANGES	518.2

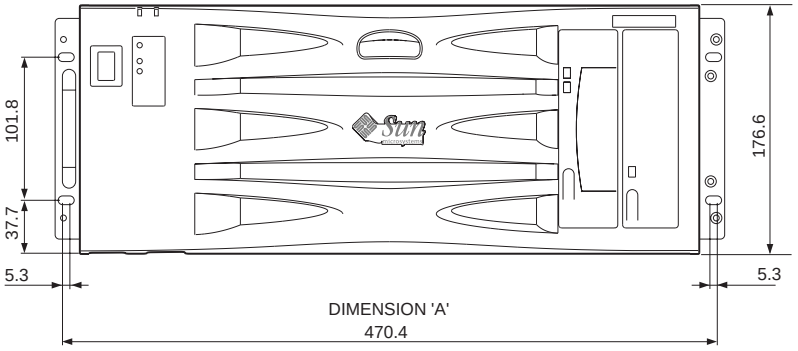


FIGURE 1-1 Netra T4 System Dimensions and Mounting Options (dimensions in mm)

System unit electronics are contained on a single printed circuit board (motherboard). The motherboard contains the CPU modules, memory, system control application-specific integrated circuits (ASICs) and I/O ASICs.

A fully-configured system weighs approximately 27.3 kg (60 lb).

Operating Environment

- Solaris 8 Update 4/01 and Update 7/01

Power

- Rack mounting enclosure with one single-feed 100–240 VAC power supply unit (AC100) or one twin-feed –48 VDC / –60 VDC power supply unit (DC100)

Processors

- Support for up to two 750 MHz UltraSPARC III processor modules, each with 8 MByte Ecache

Memory

- Support for up to eight 128 MByte-, 256 Mbyte-, 512 MByte- or 1 GByte Next Generation Dual Inline Memory Module (NG-DIMMS) installed in two groups of four providing from 512 MByte to 8 GByte of memory

IO

- Four PCI 2.1 compliant slots:
  - one long[1] 64/32-bit, 66/33 MHz
  - two long[1] 64/32-bit, 33 MHz
  - one short[2] 64/32-bit, 33 MHz
- One 10/100BaseT Ethernet connection
- One Fast-Wide SCSI connection
- Four USB connections (two twin Series A ports) @ 12 Mb/s
- One external FC-AL connection
- Two internal FC-AL connections for hard disks
- Two RS232/RS423 serial ports
- One parallel port

---

1. Up to 312 mm long
2. Up to 174.6 mm long

- One DB-15 LOMlite2 alarms relay port
- One RJ45 LOMlite2 alarms serial port

System Configuration

- I2C system configuration card reader (SCCR)

Storage

- Up to two FC-AL 1-inch hot swap hard disks (36GByte)
- External hardware RAID support through PCI
- Software RAID support Sun Logical Volume Manager (SLVM)
- Up to two removable media drives (DVD-ROM and DDS-4 DAT)

Reliability, Availability and Serviceability

- LOMLite 2 automatic system recovery
- Remote diagnosis via Solaris and LOMLite 2
- Hot swap disks
- Diagnostic LEDs
- Environmental monitoring
- Field Replaceable Unit (FRU) ID support

Documentation

- Installation and User's Guide
- Service and System Reference Manual (this document)
- Compliance and Safety Manual
- Release Notes

Software Support

- Lights Out Management 2.0 (LOMlite2)
- SLVM (Sun Logical Volume Manager)
- SunVTS™ 4.4 (Sun Validation Test Suite)
- SunMC (Sun Management Center)
- SNMP (Sun Netra SNMP Management Agent)
- SunCluster
- SRS/SunUP™ ready

PCI Card Support

- SunSwift™
- Fast Ethernet
- Quad Fast Ethernet (QFE)
- High Speed Serial Interface (HSI)
- Serial Asynchronous Interface (SAI)
- ATM-155
- Dual Differential SCSI
- Gigabit Ethernet
- FC-AL
- FC-AL and Gigabit Ethernet combination
- SSL Crypto Accelerator

1.2 System Unit Components

The system unit components are listed by part number in Appendix A.

Note – The part numbers listed in Appendix A were correct when this manual was published but they are subject to change without notice. Numerical references illustrated in FIGURE A-1 correlate to the references listed in TABLE A-1 and TABLE A-2. Refer to your authorized Sun sales representative or service provider to confirm a part number before you order a replacement part.

1.3 Environmental Performance

The principal environmental requirements are given in Section B.3, “Environmental Specification” on page B-4.

1.4 LEDs

The Netra T4 server has three sets of LEDs that show the status of the system.

1.4.1 System LEDs

The system LEDs are located behind the front fascia, immediately to the right of the ON / STBY switch as you face the unit, as shown in FIGURE 1-2.

Light pipes transmit the Power, System, Alarm1, Alarm2 and Fault LEDs through the fascia and are visible from the front of the system. To view the remaining LEDs, you must lower the front fascia.

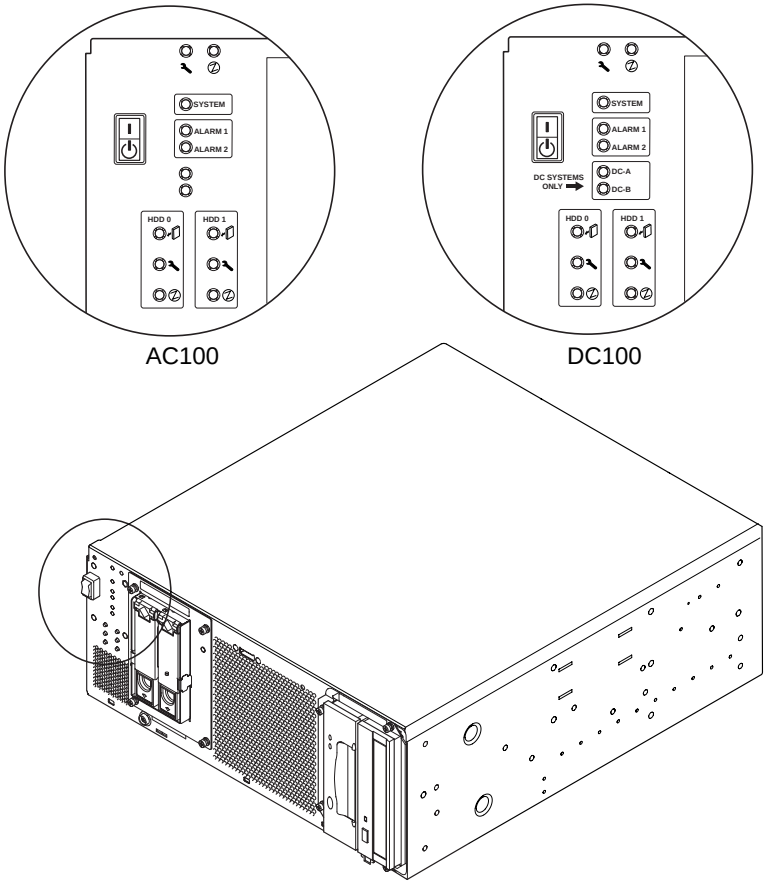


FIGURE 1-2 Front Panel System LEDs

The Alarm1, Alarm2, System and Fault LEDs are mirrored on the LOMlite2 card visible from the rear of the system (see Section 1.4.2, “LOMlite 2 LEDs” on page 1-8).

TABLE 1-1 Front Panel System LED Functions

LED	Icon/Legend	Color	Function
Power		Green	**Illuminated** continuously while power is supplied to the system.
System[1]	SYSTEM	Green	**Off** (or reset) during power up procedures and **illuminated** when UNIX is running and the Alarms driver is installed. This LED is reset by a hardware Watchdog timeout, or whenever the user-defined Alarm3 is asserted.
Alarm1[1]	ALARM1	Amber	**Illuminated** whenever the user-defined Alarm1 is asserted
Alarm2[1]	ALARM2	Amber	**Illuminated** whenever the user-defined Alarm2 is asserted
Input A OK	DC-A	Green	**Illuminated** when the input voltage from feeder A is above 37V **Off** when Input A is below 35V Not used by the AC100
Input B OK	DC-B	Green	**Illuminated** when the input voltage from feeder B is above 37V **Off** when Input B is below 35V Not used by the AC100
Fault[1]		Amber	Driven by the LOMlite2 module under identified system fault conditions
Disk0 Active[2]		Green	**Illuminated** when Disk0 is active
Disk0 OK to Remove[2]		Blue	**Illuminated**, in response to a user request, when Disk0 can be removed safely without affecting the system operation
Disk0 Fault[2]		Amber	**Illuminated** when the system has identified a fault in Disk0

TABLE 1-1 Front Panel System LED Functions *(Continued)*

LED	Icon/Legend	Color	Function
Disk1 Active[2]		Green	**Illuminated** when Disk1 is active
Disk1 OK to Remove[2]		Blue	**Illuminated**, in response to a user request, when disk1 can be removed safely without affecting the system operation
Disk1 Fault[2]		Amber	**Illuminated** when the system has identified a fault in Disk1

1. These LEDs are duplicated on the LOMlite2 card face plate (see Section 1.4.2, "LOMlite 2 LEDs" on page 1-8).
2. Lower the front fascia to view these LEDs.

1.4.2 LOMlite 2 LEDs

The LOMlite2 status LEDs, which mirror the alarm status and power LEDs on the front panel, are located on the rear of the system, between the LOMlite2 DB-15 alarms relay port and RJ45 serial port as shown in FIGURE 1-3.

TABLE 1-2 LOMlite2 Status LED Functions

LED	Icon/Legend	Color	Function
Alarm 1	1	Amber	**Illuminated** when user-defined Alarm 1 is asserted
Alarm 2	2	Amber	**Illuminated** when user-defined Alarm 2 is asserted
Fault		Amber	Driven by the LOMlite 2 card and **illuminated** when a system fault condition exists
System	SYS	Green	**Illuminated** when Solaris is running and the LOMlite2 driver is installed **Off** while the system is powering up Reset by watchdog timeout, assertion of user-defined Alarm 3

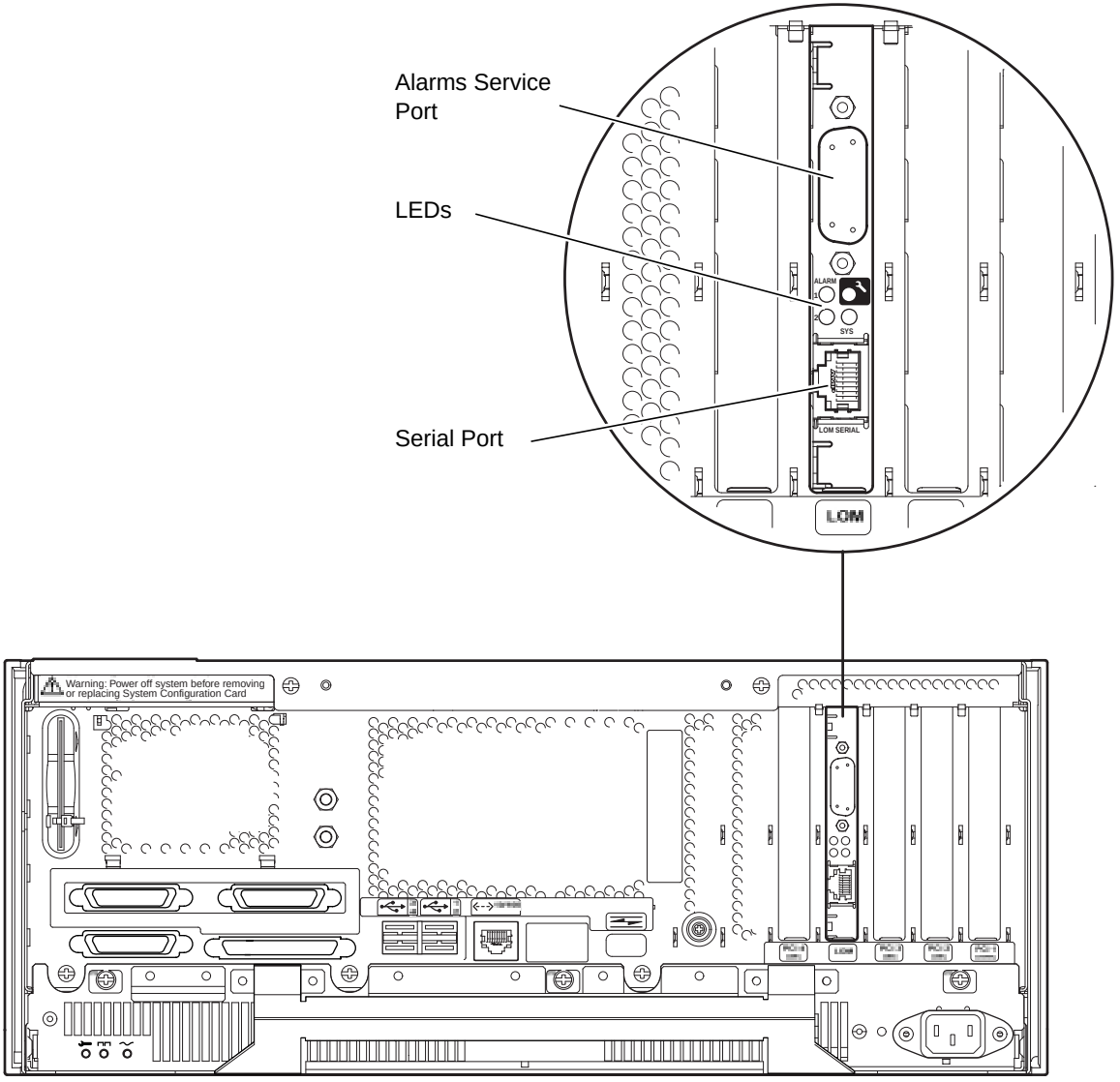


FIGURE 1-3 LOMLite2 Status LEDs

1.4.3 PSU LEDs

The PSU status LEDs are located at the left hand end of the PSU (see FIGURE 1-4).

1.4.3.1 Netra T4 AC100 System

TABLE 1-3 PSU Status LED Functions

LED	Icon	Color	Function
AC Input OK	~	Green	**Illuminated** when AC is present and above 85VAC
PSOK	⊓⊓	Green	**Illuminated** when output voltages are within operating range **Flashes** when PSU is in Standby mode
Fail	🔧	Amber	**Illuminated** when PSU is in a Fault condition **Off** when PSU is enabled (OK) **Flashes** if unit is within 10˚C of thermal shutdown or has shutdown

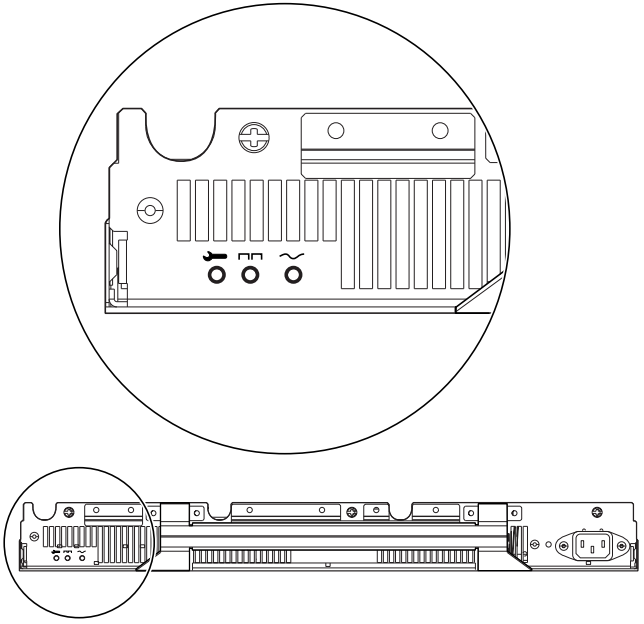


FIGURE 1-4 PSU Status LEDs (Netra T4 AC100 System)

1.4.3.2 Netra T4 DC100 System

TABLE 1-4 PSU Status LED Functions (Netra T4 DC100)

LED	Icon	Color	Function
Fail		Amber	**Illuminated** when PSU is in a Fault condition **Off** when PSU is not enabled (OK) **Flashes** if unit is within 10˚C of thermal shutdown or has shutdown
PSOK		Green	**Illuminated** when output voltages are within operating range **Flashes** when PSU is in Standby mode
Input B OK	B	Green	**Illuminated** when input voltage from feeder B is above 37V **Off** when Input B is below 35V
Input A OK	A	Green	**Illuminated** when input voltage from feeder A is above 37V **Off** when Input A is below 35V

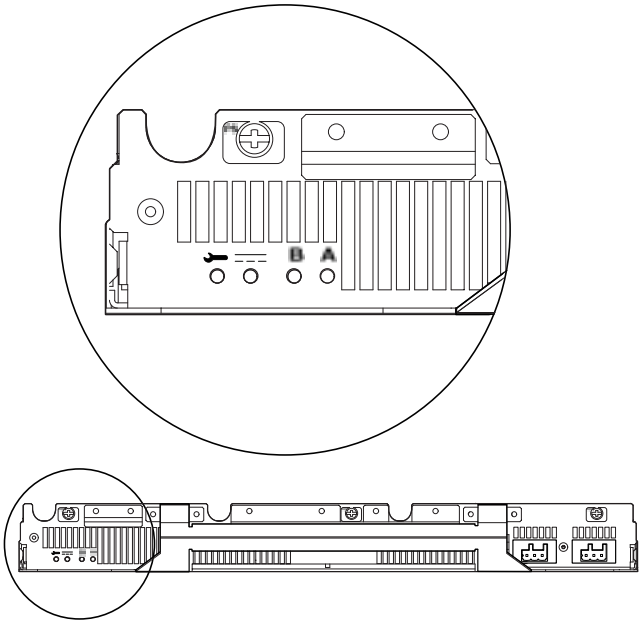


FIGURE 1-5 PSU Status LEDs (Netra T4 DC100 System)

CHAPTER 2

Power-On Self Test

This chapter describes how to initiate power-on self test (POST) diagnostics.

The chapter contains the following topics:

- Section 2.1, “POST Overview” on page 2-1
- Section 2.2, “Pre-POST Preparation” on page 2-3
- Section 2.3, “Running POST” on page 2-4
- Section 2.4, “POST Diagnostic Levels” on page 2-4

2.1 POST Overview

POST is a firmware program that is useful in determining if a portion of the system has failed. POST verifies the core functionality of the system, including the CPU module(s), motherboard, memory, and some on-board I/O devices, and generates messages that can be useful in determining the nature of a hardware failure. POST can be run even if the system is unable to boot.

POST detects most system faults and is located in the motherboard OpenBoot™ PROM. POST can be set to run by the OpenBoot program at power up by setting two environment variables, the `diag-switch?` and the `diag-level` flag, which are stored on the System Configuration Card.

POST diagnostic and error message reports are displayed on a console.

2.1.1 How to Use POST

POST runs automatically when the system power is applied, and following an automatic system reset if both of the following conditions apply:

- `diag-switch?` is set to `true` (default is `false`)
- `diag-level` is set to `min`, `max` or `menus` (default is `min`)

If `diag-level` is set to `min` or `max`, POST performs an abbreviated or extended test, respectively (see Section 2.4, “POST Diagnostic Levels” on page 2-4).

If `diag-level` is set to `menus`, a menu of all the tests executed at power up is displayed (CODE EXAMPLE 2-1):

CODE EXAMPLE 2-1 POST Test Menu

```
{0}* Xcall Test
{0}Sending Cross Calls to CPU AID 1
{0}     0    Return
{0}     1    Run all Tests in this Menu
{0}     2    Change Test Control Flags
{0}     3    * Reset Menu
{0}     4    * CPU Tests
{0}     5    * Ecache Tests
{0}     6    * Memory Tests
{0}     7    * Schizo Tests
{0}     8    * RIO Tests
{0}     9    * Estar Test (UP only)
{0}     a    * ECC Tests
{0}     b    * MP Tests
{0}     c    * BIST
{0}     d    * System Frequency and CPU Ratio
{0}     e    * I2C/Fan/Temperature/Smart card
{0}     f    * Run POST
{0}    10    * Return to OBP
{0}Selection
```

Selection 2 enables you to change the test control flags (CODE EXAMPLE 2-2):

CODE EXAMPLE 2-2 POST Test Control Flags Menu

```
{0}Selection:2
{0}     0    Return
{0}     1    Run all Tests in this Menu
{0}     2    Change Test Control Flags
{0}     3    * Toggle Trace Flag - c
{0}     4    * Toggle Loop-a-test flag - l
{0}     5    * Toggle Loop-on-error flag - e
{0}     6    * Toggle Print-all-error flag  - p
{0}     7    * Display current state of all flags
{0}     8    * Help on Test Flags
{0}Selection:
```

Note – If `diag-switch` = false, POST is disabled. If `diag-switch` = `true` and `diag-level` = `max`, POST runs in `max` mode. If `diag-switch` = `true` and `diag-level` = `min`, POST runs in `min` mode.

To run POST, power cycle the system.

2.2 Pre-POST Preparation

1. **Connect a terminal to the LOM serial port on the Netra T4 server to view POST progress and error messages. See Section G.1, “Connecting to the LOM Serial Port” on page G-1.**

Note – By default, the input and output device is the LOM serial port. To direct POST output to ttya or ttyb, set both `input-device` and `output-device` to `ttya` or `ttyb`:

---

2. **Set the** `diag-switch?` **and** `diag-out-console` **configuration variables to** `true`:

```
ok setver diag-switch? true
ok setver diag-out-console true
```

Alternatively, from the shell prompt:

```
# eeprom diag-switch?=true
# eeprom diag-out-console=true
```

3. **Set the** `diag-level` **configuration variable to** `max` **or** `min` **(see Section 2.4, "POST Diagnostic Levels" on page 2-4).**

```
ok setenv diag-level value
```

or

```
# eeprom diag-level=value
```

Note – The default value is `min`.

2.3 Running POST

To run POST:

- **Initiate POST using one of the following methods**:

  a. Briefly press the power ON/STBY switch to power cycle the system.

  b. At the LOM prompt, type `poweroff` followed by `poweron`.

2.4 POST Diagnostic Levels

Two levels of POST are available: maximum (`max`) level and minimum (`min`) level. The system initiates the selected level of POST based on the setting of `diag-level`, a configuration variable.

The time required to complete POST depends on the CPU configuration and the amount of installed memory. The following table lists the approximate time required to complete the POST for single and dual processor systems with varying memory installed, for `diag-level` variable settings of `max` and `min`.

TABLE 2-1 POST Completion Times

CPU and Memory	`max` setting	`min` setting
2P, 4GByte	8 minutes	5 minutes
2P, 1GByte	4 minutes	6 minutes
1P, 2GByte	4 minutes	7 minutes
1P, 512MByte	3 minutes	5 minutes

The default value for `diag-level` is `min`.

2.4.1 `diag-level` Variable Set to `max`

When the `diag-level` variable is set to `max`, POST enables an extended set of diagnostic-level tests. See TABLE 2-1 for approximate completion times.

CODE EXAMPLE E-1 in Appendix E provides an example of the POST output from a system with two 750MHz CPUs and 4Gbyte of memory, and with the `diag-level` variable set to `max`.

2.4.2 `diag-level` Variable Set to `min`

When the `diag-level` variable is set to `min`, POST enables an abbreviated set of diagnostic-level tests. See TABLE 2-1 for approximate completion times.

CODE EXAMPLE E-2 in Appendix E provides an example of the POST output from a system with two 750MHz CPUs and 4Gbyte of memory, and with the `diag-level` variable set to `min`.

2.4.3 Error Messages

CODE EXAMPLE 2-3 shows a sample error message at the console:

CODE EXAMPLE 2-3 Sample POST Console Error Message

```
Power On Self Test Failed.
Cause: DIMM J0406 or System Board

ok
```

CODE EXAMPLE 2-4 shows a sample error message at the serial port.

CODE EXAMPLE 2-4 Sample POST Serial Port Error Message

```
{0} ERROR: TEST=*Memory Initial area TESTID=2
{0} H/W under test=*MAIN MEMORY
{0} Fault address 00000000.00000010
{0} Fault status 00000002.0000004f
{0} (CE) Correctable system data ECC error
{0} CPU data bit 6
{0} Memory data bit 146
{0} DIMM connector J0406
{0} Connector pin 124
{0} CPMS slice 124
```

CHAPTER 3

SunVTS

This chapter contains an overview of the Sun Validation Test Suite 4.4 (SunVTS™) diagnostic tool. You can use SunVTS to validate a system when troubleshooting and during periodic maintenance.

This chapter contains the following topics:

- Section 3.1, “The Validation Test Suite” on page 3-1
- Section 3.1.1, “SunVTS Requirements” on page 3-2
- Section 3.1.2, “SunVTS References” on page 3-2
- Section 3.1.3, “Installation” on page 3-3
- Section 3.1.4, “New and Modified Features and Options” on page 3-3
- Section 3.2, “SunVTS Tests” on page 3-6

3.1 The Validation Test Suite

SunVTS Version 4.4 is the Sun online Validation Test Suite supplied with the Netra T4 system.

SunVTS is a comprehensive software diagnostic package that tests and validates hardware by verifying the connectivity and functionality of most hardware controllers, devices, and platforms.

SunVTS can be tailored to run on various types of systems ranging from desktops to servers and has many features that you can customize to meet the varying requirements of differing diagnostic situations.

SunVTS executes multiple diagnostic tests from a graphical user interface (GUI) or TTY interface that provide test configuration and status monitoring.

The SunVTS interface can run on one system to display the SunVTS test session of another system on the network.

SunVTS is distributed with each Solaris release. It is located on the Sun Computer Systems Supplemental CD.

3.1.1 SunVTS Requirements

Your system must meet the following requirements to run SunVTS:

- The SunVTS packages must be installed. The main package is `SUNWvts`. There are additional supporting packages that differ with the revision of the Solaris operating system that is installed. See also Section 3.1.3, “Installation” on page 3-3 and the corresponding SunVTS documentation.
- The system must be booted to the multiuser level (level 3).
- To run SunVTS with a GUI (CDE or Open Look), that GUI must be installed. Otherwise, run SunVTS with the TTY-mode interface.

3.1.2 SunVTS References

To find out more information about the using SunVTS, refer to the SunVTS documentation for the Solaris release that you are running.

The SunVTS documents are part of the Solaris on Sun Hardware AnswerBook™ collection. This AnswerBook collection is pre installed on the hard disk of new systems. It is also distributed on the Software Supplemental CD that is part of each Solaris Media Kit release and is also accessible at `http://docs.sun.com`.

The following list describes the contents of each SunVTS document:

- *SunVTS User’s Guide* describes how to install, configure, and run the SunVTS diagnostic software.
- *SunVTS Test Reference Manual* provides details about each individual SunVTS test.
- *SunVTS Programmer’s Guide* supports the development of custom tests.

3.1.3 Installation

The SunVTS 4.4 software comprises four installation packages:

- SUNWvts—SunVTS kernel, user interface and tests
- SUNWvtsx—SunVTS 64-bit package
- SUNWvtsol—SunVTS user interface
- SUNWvtsmn—SunVTS man pages

For details of the installation procedure, refer to the *Netra T4 AC100/DC100 Installation and User's Guide*.

3.1.4 New and Modified Features and Options

The following additions have been made to support the Netra T4 system:

- Tests have been included for the new components of the hardware platform.
- Remote features enable you to interface to SunVTS from a remote system.
- Multiple user interfaces can monitor and run tests concurrently.
- A test scheduler enables you to specify groups of tests to be conducted in a predefined order. Tests in a group are executed concurrently so that all tests in one group complete before the tests in another group begin.
- A new SunVTS message format displays the information re-ordered and labeled:

```
<timestamp> <hostname> "SunVTS:"[VTSID <vts msgid>]
<modulename> [.<submodulename>] [.<insttnum>].<vts_msgtype>]
[<device_pathname>:] <msg_txt>
```

```
08/05/01 17:19:47 vrij SunVTS: VTSID 34 disktest.VERBOSE c0t0d0:
"number of blocks 3629760"
```

3.1.4.1 New and Modified Tests and Commands

The following commands have been added to this release of SunVTS.

TABLE 3-1 New SunVTS Commands

Command	Function
`testadd`	Adds a test's resource object files to the SunVTS shared object library (contained in the SUNWvtstk package)
`testrm`	Removes a test's resource object file from the SunVTS shared object library (contained in the SUNWvtstk package)
`testinfo`	Lists all the resource object files from the SunVTS shared object library (contained in the SUNWvtstk package)
`vts_cmd`	Enables direct control of SunVTS from your program or scripts on a remote machine
`connect`	Enables a user interface to connect to a SunVTS kernel on any system on a network
`trace`	System call tracing that assists in tracing test flows through the system interfaces
`Record/Replay`	Enables test sequences and forks to be recorded and replayed to improve failure reproducibility
`Reprobe`	Searches and recompiles (reprobes) the system's configuration on demand

Note – To add a third party test executable binary, add the test to `/opt/SUNWvts/bin/sparcv9`, then modify the `/opt/SUNWvts/bin/sparc9/.customtest file`.

The commands are shown in the SunVTS GUI menus (FIGURE 3-1):

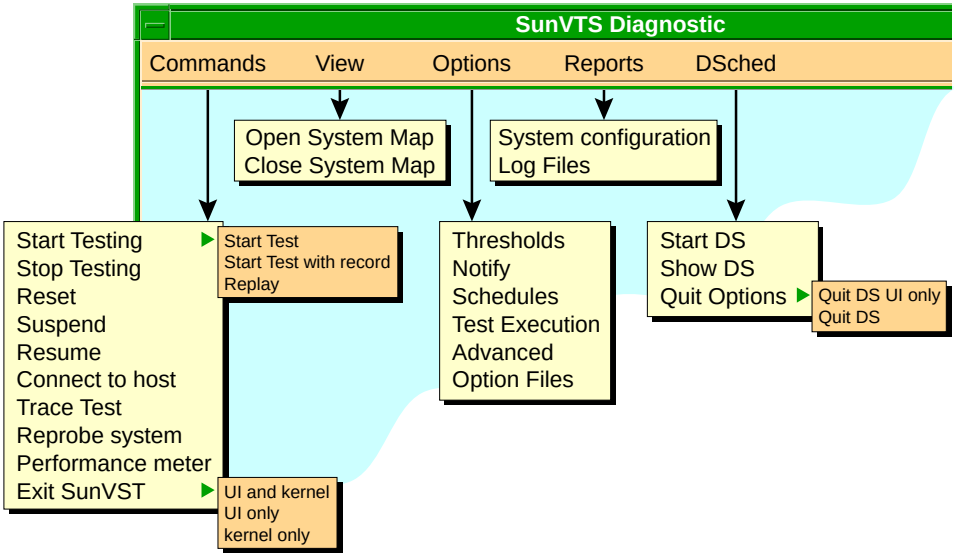


FIGURE 3-1 SunVTS Menu Bar

3.1.5 Starting SunVTS

You can start SunVTS in one of four modes, depending on whether you are executing locally or remotely, on a CDE GUI, OpenLook GUI, or in TTY mode:

- To run SunVTS kernel and default GUI on the local system, type:

```
# cd /opt/SUNWvts/bin
# ./sunvts
```

- To run SunVTS kernel and OpenLook GUI on the local system, type:

```
# cd /opt/SUNWvts/bin
# ./sunvts -l
```

- To run SunVTS kernel in TTY mode on the local system, type:

```
# cd /opt/SUNWvts/bin
# ./sunvts -t
```

- To connect and test a remote system, hostname, but display the GUI on the local host, type:

```
# cd /opt/SUNWvts/bin
# ./sunvts -h
```

Note – The latest SunVTS features may not be supported by the SunVTS OpenLook GUI.

3.2 SunVTS Tests

This section lists the tests available in SunVTS 4.4. Some tests have been modified and new tests have been added to support the Netra T4 hardware platform.

TABLE 3-2 SunVTS Processor Tests

Test	Function
`cputest`	This new test checks the specific functionality of the SPARC processor data path, including: ■ `g0` register functionality ■ `Compress/Uncompress/Compare` command
Legacy Tests	These include: ■ `systest`—tests the I/O, memory and CPU channels ■ `fputest`—tests the floating point unit ■ `mptest`—tests two or more processors by having them access a shared memory page

TABLE 3-3 SunVTS Memory Tests

Test	Function
Legacy Tests	These include: ■ `pmemtest`—tests the physical memory by targeting parity, ECC, memory read, and addressing problems ■ `vmemtest`—tests the virtual memory and the swap partitions of the disks

TABLE 3-4 SunVTS Storage Device Tests

Test	Function
`dvdtest`	This new test checks the DVD-R drive by reading the DVD.
`qlctest`	This new test checks the ISP2200A FC-AL controller. The sub tests include: ■ Revision checks ■ Internal loopback tests ■ External loopback tests (require external loopback cable)
Legacy Tests	These include: ■ `cdtest`—tests the CD-ROM drive by reading the CD ■ `tapetest`—tests tape devices by writing, reading and verifying synchronous and asynchronous data blocks

TABLE 3-5 SunVTS Network Tests

Test	Function
`netlbtest`	This new test checks the ERI and GEM Ethernet controllers by performing internal and external loopback tests (replaces `gemtest`).
`nettest`	This system-to-system legacy test covers all networking devices found in the system.

TABLE 3-6 SunVTS Communications Port Tests

Test	Function
`usbkbtest`	This new test covers the keyboard and mouse.
Legacy Tests	These include: ■ `sptest`—tests the serial sync. and async. ports ■ `ecpptest`—tests the parallel ports

TABLE 3-7 SunVTS Custom Test

Test	Function
cpupmtest	This new test checks the CPU power management functionality.

Note – Test failures occur if you run `nettest` and `netlbtest` simultaneously.

3.2.1 Guide to Using SunVTS 4.4

The following guidance notes points are included to help you use SunVTS 4.4.

- The packages SUNWeswsa, SUNWsycfd, SUNWesnta and SUNWeswgn are no longer required or supplied for physical mapping support.
- The disktest probe does not premount any partitions by default. You can set the environment variable BYPASS_FS_PROBE to zero to force all unmounted partitions to premount.
- Premounting will not take place, even if you have enabled it, if the disktest probe detects the presence of Veritas or Solstice DiskSuite.
- If you run a media subtest on a disk partition in WriteRead mode, data corruption can occur if the partition is shared with other programs.
- An option file created when BYPASS_FS_PROBE was set to 0 may not load when BYPASS_FS_PROBE is set to 1. If required, create option files for both states of BYPASS_FS_PROBE
- SunVTS (Kerebos SEAM) security is now on by default. To turn security off, edit the security file `/opt/SUNvts/bin/.sunvts` to include a "+" in the HOST section. This will make all the listed hosts *trusted* hosts.
- Physical mapping is supported only on systems that support `configd`.
- Do not mix CDE and OpenLook environments.
- The files `.customtest` and `.customtest_OtherDevices` are separate files in the 64-bit version of SunVTS. They are installed in `/opt/SUNWvts/bin/spacv9`, and not `/opt/SUNWvts/bin` as is the case for the 32-bit version.
- The environment variable VTS_PM_PATH is used to locate the pix map files when SunVTS is not installed in the default base directory (`/opt`).
- The following tests have been renamed:
  - `spif -> spiftest`
  - `pmem -> pmemtest`
  - `vmem -> vmemtest`
- The following tests are not supported in 64-bit mode:
  - `cg14test`
  - `isdntest`
  - `tcxtest`
- The physical map view displays only one level of the hierarchy. To view the complete hierarchy, use the logical view.

CHAPTER 4

Troubleshooting

This chapter describes how to troubleshoot possible hardware problems and suggests corrective actions.

This chapter contains the following topics:

- Section 4.1, “Power-On Failure” on page 4-2
- Section 4.2, “System LEDs” on page 4-2
- Section 4.3, “Drive Failure” on page 4-2
- Section 4.4, “Power Supply Unit Troubleshooting” on page 4-4
- Section 4.5, “OpenBoot PROM Diagnostics” on page 4-7
- Section 4.6, “OpenBoot Emergency Procedures” on page 4-30

Caution – Regardless of the position of the ON/STBY switch, when an AC power cord remains connected to the system, hazardous voltage is always present within the power supply.

Caution – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system unit components, use an antistatic wrist strap with a 10mm press stud connection and attach the antistatic wrist strap to the press stud at the rear or front of the chassis before removing the top access cover.

Caution – Owing to the weight of the unit, two persons are required to remove the unit from and replace it in the rack.

4.1 Power-On Failure

This section provides examples of power-on failure symptoms and suggested actions.

Symptom

The system does not power up when you press the ON/STBY switch.

Action

- Ensure that a PSU is installed and properly seated. Check that the three PSU fixing screws have been tightened.
- Ensure that the AC power cord is properly connected to the system and to the wall socket. Verify that the wall socket is supplying AC power to the system.
- Press the ON/STBY switch. If the system does not power on, the CPU module(s) may not be properly seated. Inspect the CPU module(s) for proper seating, and press the ON/STBY switch again.
- If the AC power wall socket is live and the CPU module(s) are properly seated, but the system does not power on, the PSU may be defective. Check the status of the PSU LEDs and see Section 4.4, “Power Supply Unit Troubleshooting” on page 4-4.

4.2 System LEDs

The system LEDs located on the front and rear system panels provide information about the status of the system and many of its subsystems. Refer to Section 1.4, “LEDs” on page 1-6 for a description of their function.

4.3 Drive Failure

This section provides hard drive, DVD-ROM and DAT drive failure symptoms and suggested actions.

Symptom

A hard drive read, write, or parity error is reported by the operating environment or customer application.

A DVD-ROM or DAT drive read error or parity error is reported by the operating environment or customer application.

Action

Replace the drive indicated by the failure message. The operating environment identifies the internal drives, as listed in the following table.

TABLE 4-1 Internal Drives Identification

Operating Environment Address	Drive Physical Location and Target
`c1t1d0s#`	Left hard drive, LiD / HA 1
`c1t2d0s#`	Right hard drive, LiD / HA 2
`c0t6d0s#`	DVD-ROM drive, target 6 (optional)
`c0t5d0s#`	DAT drive, target 5 (optional)

Note – The # symbol in the operating environment address examples is a numeral between 0 and 7 that describes the slice or partition on the drive.

Symptom

The DVD-ROM drive fails to respond to commands.

Action

Test the drive response to the `probe-scsi` command as follows.

Note – To bypass POST, type **`setenv diag-switch? false`** at the `ok` prompt.

At the OBP `ok` prompt, type:

```
ok reset-all
ok probe-scsi-all
```

If the DVD-ROM drive responds correctly to `probe-scsi-all`, the message identified in CODE EXAMPLE 4-2 is displayed; the system SCSI controller has successfully probed the device. This is an indication that the motherboard is operating correctly. If the drive does not respond to the SCSI controller probe, replace the unresponsive drive.

4.4 Power Supply Unit Troubleshooting

Caution – During the power supply voltage measurement checks, an operational load must be on the power supply. Ensure that the power supply cables remain connected to the motherboard.

The section describes how to use a digital volt meter (DVM) to test the power supply under operational load. See the figures and tables in this section to identify the J3601 and J3603 power connectors.

1. **Power off the system and remove the top access panel.**

   See Chapter 5 for details.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface. See Section 5.5, “Antistatic Precautions” on page 5-5.

Caution – Hazardous voltages are present. To reduce the risk of electrical shock and danger to personal health, follow the instructions.

2. **Check the continuity of the power cables between the PDB and motherboard.**
3. **Ensure that the PSU is correctly located in the chassis and that the fixing screws are fully tightened.**

4. **Check the PSU LEDs (see Section 1.4.3, “PSU LEDs” on page 1-10) to verify the status of the PSU.**

5. **Check that the power cable connectors are properly seated at the PDB and motherboard.**

6. **Power on the system.**

7. **Using a DVM, check the power supply output voltages.**

   See FIGURE 4-1 for the power supply connector location on the motherboard.

   Note – All power supply connectors being tested must remain connected to the motherboard and PDB.

   ---

   a. **With the negative probe of the DVM placed on a connector ground (GND) pin, position the positive probe on each power pin.**

   b. **Verify voltage and signal availability as listed in the voltage-pin tables.**

8. **If any power pin signal is not present with the power supply active, and the power cables between the PDB and motherboard properly connected, replace the power supply.**

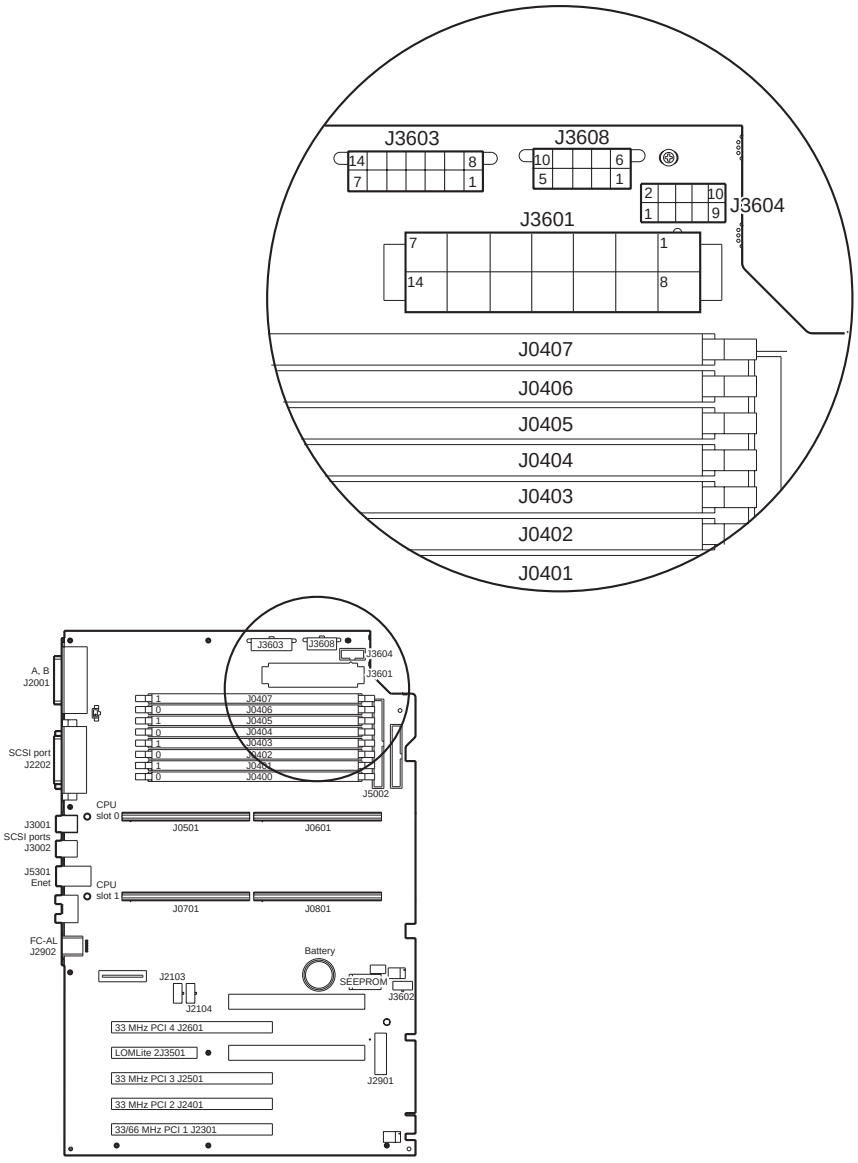


FIGURE 4-1 Power Supply Connector Jack Location

TABLE 4-2 J3601 Voltage-Pin Table

Pin	Voltage	Pin	Voltage
1	0V	8	+5V
2	-12V	9	n/a
3	0V	10	+5V
4	0V	11	+3.3V
5	0V	12	+12V
6	0V	13	+12V
7	n/a	14	+5V

TABLE 4-3 J3603 Voltage-Pin Table

Pin	Voltage	Pin	Voltage
1	+3.3V	8	0V
2	+3.3V	9	0V
3	+3.3V	10	0V
4	+3.3V	11	0V
5	+5V	12	0V
6	+5V	13	0V
7	+5V	14	0V

4.5 OpenBoot PROM Diagnostics

The following sections describe the OpenBoot PROM diagnostics. To execute the OpenBoot PROM on-board diagnostics, the system must be at the ok prompt.

- Section 4.5.1, “New Features” on page 4-8
- Section 4.5.2, “New and Modified Commands and Tests” on page 4-10
- Section 4.5.3, “Device Tree” on page 4-14
- Section 4.5.4, “Running the Diagnostics” on page 4-18

4.5.1 New Features

This section summarizes the features supported in OpenBoot 4.2 that are not covered in the *OpenBoot 3.x Command Reference Manual* (part no. 806-1377-10) and the *OpenBoot 3.x Quick Reference* (part no. 806-2908-10).

- Universal Serial Bus (USB)
- FC-AL drive support
- New device driver support for:
  - PCI prober
  - I2C
  - USB
  - NVRAM
  - FC-AL
  - ERI
- Safari Giga Plane Two (`gptwo`) support
- Autoconfiguration
- Flash PROM (2MByte) divided into quadrants
  - Quadrant 0—Sun Blade™ 1000 OBP—Start address 0
  - Quadrant 1—Sun Fire™ E280R OBP / Netra T4 OBP—Start address 512k
  - Quadrant 2—POST (shared)—Start address 1.0M
  - Quadrant 3—OBDiag (shared)—Start address 1.5M
- Flash updates replace two quadrants at a time
  - Quadrant 0 and 1
  - Quadrant 2 and 3
- Support for:
  - Stop-A
  - Stop-A on ttya (#)
  - Stop-N (emulated by `lom>` **`bootmode reset_nvram`**))
  - Stop-F (emulated by `lom>` **`bootmode forth`**)
  - Stop-D (emulated by `lom>` **`bootmode diag`**)

PCI Buses

Two PCI buses are implemented that are fully independent in terms of address and data paths, channel engines, `gptwo` memory physical address space, I/O physical address space and configuration space. As the device space is not shared between the two PCI buses, you must access the specific PCI node to view its properties.

Flash PROM

The flash PROM is divided into quadrants that are dedicated to Sun Blade 1000 OBP, Sun Fire E280R OBP / Netra T4 OBP, POST and OBDiag, respectively. A flash update involves two quadrants, either 0 and 1, or 2 and 3. You can download the quadrants from a standalone utility, bootable DVD-ROM, or from the network. The updates are available in binary or UNIX shell formats.

During a flash PROM update, the OBP firmware overwrites the upper half of PROM (where POST resides), keeping the original OBP unchanged. After the new OBP is tested successfully, the original OBP is overwritten with the new OBP. Finally, after the OBP is tested again, POST is reloaded into the upper half of PROM.

OBP Prompt

On dual processor systems, the OBP prompt includes the CPU number:

```
{0} ok
```

Resets

When the system is first powered up, the configuration is determined using information stored in the motherboard and CPU EEPROMS (CPU speed, memory configuration, and so forth) and is saved in the BootBus Controller (BBC) SRAM. This is termed a *Configuration Reset*. Subsequent system power cycles generate a configuration reset.

A *Soft Reset* occurs on subsequent system resets, which uses the BBC's SRAM configuration information. To avoid booting with corrupted configuration information, a checksum is performed on the data. If the data is found to be corrupt, the subsequent reset reverts to a configuration reset.

4.5.2 New and Modified Commands and Tests

The `probe` and `test` commands have been modified to include FC-AL and USB keyboard and mouse, respectively:

TABLE 4-4 `probe` and `test` Commands

Command	New Features
`probe-scsi`	Identifies the devices attached to the FC-AL buses
`probe-scsi-all`	Identifies all devices attached to all SCSI and FC-AL buses
`test-all`	Includes all tests

4.5.2.1 `probe-scsi` and `probe-scsi-all`

The `probe-scsi` diagnostic transmits an inquiry command to internal and external FC-AL and SCSI devices connected to the system on-board SCSI or FC-AL interface. If the SCSI device is connected and active, the target address, unit number, device type, and manufacturer name are displayed.

The `probe-scsi-all` diagnostic transmits an inquiry command to all devices connected to the system. The first identifier listed in the display is the SCSI host adapter address in the system device tree followed by the SCSI device identification data.

Initiate the `probe-scsi` diagnostic by typing the `probe-scsi` command at the `ok` prompt and initiate the `probe-scsi-all` diagnostic by typing the `probe-scsi-all` command at the `ok` prompt.

To perform a `probe` command, at the `ok` prompt, ensure that `autoboot?` is set to `false`, then perform a `reset-all`.

The following code examples identify the `probe-scsi` and the `probe-scsi-all` diagnostic output messages.

CODE EXAMPLE 4-1 `probe-scsi` Diagnostic Output Message

```
ok probe-scsi
LiD HA --- Port WWN ---      ---- Disk description ----
1   1  210000203700ca78  SEAGATE ST39103FCSUN9.0G01479916021084
3   3  210000203708ad4d  SEAGATE ST39102FCSUN9.0G09299906F45038
ok
```

CODE EXAMPLE 4-2 `probe-scsi-all` Output Message

```
ok probe-scsi-all
/pci@8,600000/SUNW,glc@4
LiD HA  --- Port WWN ---      ---- Disk description ----
3   3  210000203708ad4d  SEAGATE ST39102FCSUN9.0G09299906F45038
1   1  210000203700ca78  SEAGATE ST39103FCSUN9.0G01479916021084
/pci@8,700000/scsi@6,1
Target 0
 Unit 0   Disk     SEAGATE ST39173W SUN9.0G2815
/pci@8,700000/scsi@6

Target 6
 Unit 0  Removable Read Only device   TOSHIBA DVD-ROM SD-M12011B08

ok
```

4.5.2.2 `test` *alias name, device path, -all*

The `test` diagnostic, combined with a device alias or device path, enables a device self-test program. If a device has no self-test program, the message `No selftest method for device name` is displayed. To enable the self-test program for a device, type the `test` command, followed by the device alias or device path name.

The following code example identifies the test output message. TABLE 4-5 lists `test` *alias name* selections, their descriptions, and their required preparation.

CODE EXAMPLE 4-3 Test Output Message

```
ok test net
Testing net
```

TABLE 4-5 Selected OpenBoot PROM On-Board Diagnostic Tests

Type of Test	Description	Preparation
`test net`	Performs internal/external loopback test of the system auto-selected Ethernet interface.	An Ethernet cable must be attached to the system and to an Ethernet tap or hub. If the Ethernet cable is not correctly attached the external loopback test will fail.
`test-all`	Sequentially tests system-configured devices containing selftest.	Tests are sequentially executed in device-tree order (viewed with the `show-devs` command).

4.5.2.3 `watch-clock`

The `watch-clock` diagnostic displays the result as a seconds counter. During normal operation, the seconds counter repeatedly increments from 0 to 59. Initialize the `watch-clock` diagnostic by typing the `watch-clock` command at the `ok` prompt.

The following code example identifies the `watch-clock` diagnostic output message.

CODE EXAMPLE 4-4 Watch-Clock Diagnostic Output Message

```
{0} ok watch-clock
Watching the 'seconds' register of the real time clock chip.
It should be 'ticking' once a second.
Type any key to stop.
4
```

4.5.2.4 `watch-net` and `watch-net-all`

The `watch-net` and `watch-net-all` diagnostics monitor Ethernet packets on the Ethernet interfaces connected to the system. Good packets received by the system are indicated by a period (`.`). Errors such as the framing error and the cyclic redundancy check (CRC) error are indicated with an X and an associated error description. Initiate the `watch-net` diagnostic is by typing the `watch-net` command at the `ok` prompt and initiate the `watch-net-all` diagnostic by typing the `watch-net-all` command at the `ok` prompt.

The following code examples identify the `watch-net` and the `watch-net-all` output messages.

CODE EXAMPLE 4-5 `watch-net` Diagnostic Output Message

```
{0} ok watch-net
Internal loopback test -- succeeded.
Link is -- up
Looking for Ethernet Packets.
'.' is a Good Packet. 'X' is a Bad Packet.
Type any key to stop.............................
```

CODE EXAMPLE 4-6 `watch-net-all` Diagnostic Output Message

```
{0} ok watch-net-all
/pci@8,700000/network@5,1
Internal loopback test -- succeeded.
Link is -- up
Looking for Ethernet Packets.
'.' is a Good Packet. 'X' is a Bad Packet.
Type any key to stop.
```

4.5.2.5 Serial Port Protocol

The serial port protocol is now programmed as RS232 or RS423 using `setenv` rather than by changing a jumper setting.

To change the serial ports to RS232, type:

```
ok setenv ttya-mode 9600,8,n,1,-,rs232
ok setenv ttyb-mode 9600,8,n,1,-,rs232
ok setenv auto-boot? false
ok reset-all
```

To change the serial ports to RS423, type:

```
ok setenv ttya-mode 9600,8,n,1,-,rs423
ok setenv ttyb-mode 9600,8,n,1,-,rs423
ok setenv auto-boot? false
ok reset-all
```

4.5.3 Device Tree

The device tree for the Netra T4 system is shown in FIGURE 4-2.

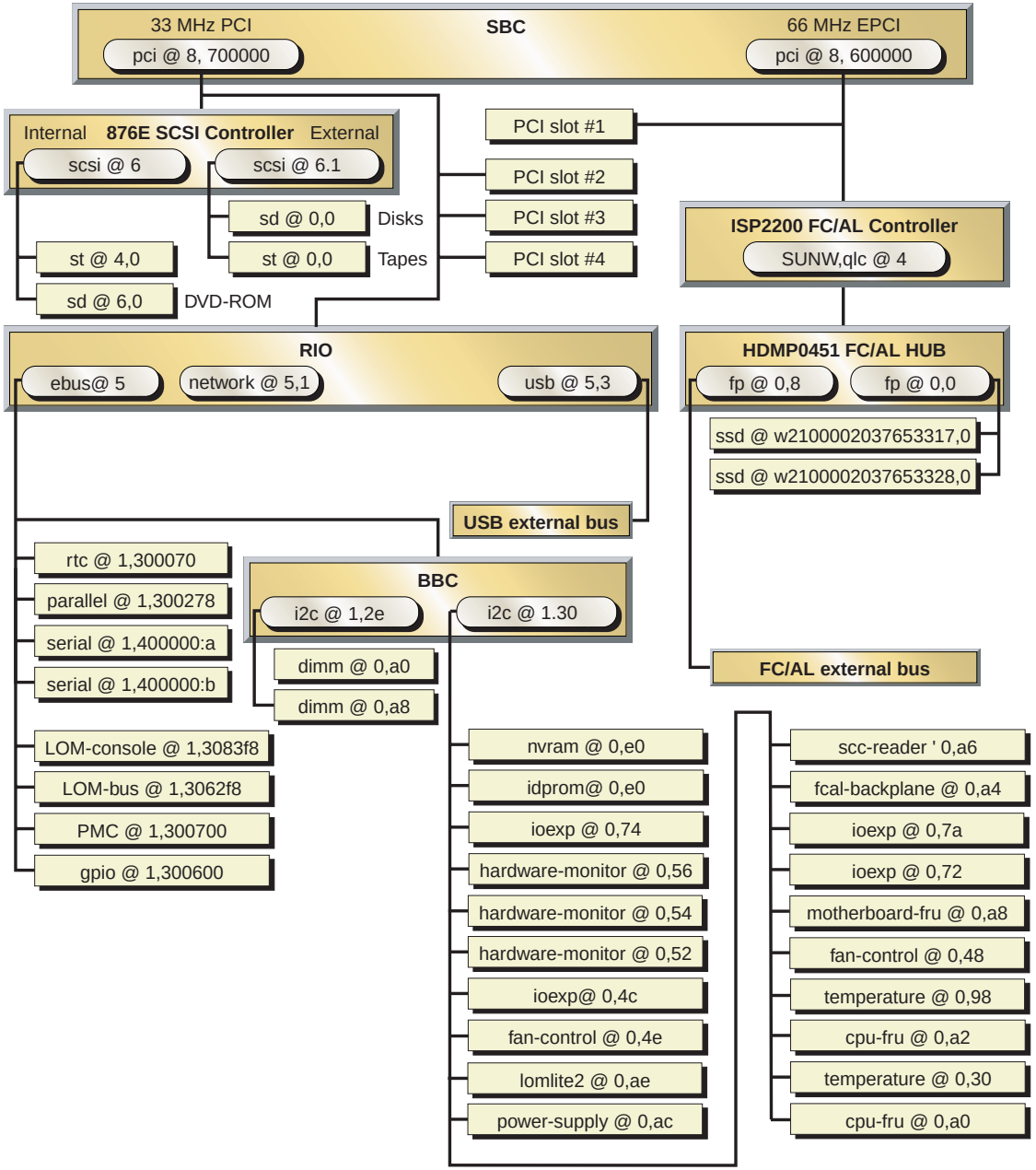


FIGURE 4-2 Netra T4 System Device Tree

The device tree comprises the Parent Node (see TABLE 4-6), the Port ID, and the PCI Bus Module (PBM) Control Space Offset within the System Bus Controller (SBC) address space for the parent node.

TABLE 4-6 Parent Node Names

Description	Child New Name	Parent	Comments
SCSI Bus	scsi	pci@8,700000	Internal SCSI (scsi@6) External SCSI (scsi@6,1)
USB Bus	usb	pci@8,700000	
Ethernet Bus	network	pci@8,700000	
EBus	ebus	pci@8,700000	
FC-AL Bus	qlc	pci@8,600000	

The following values apply to the Netra T4 system:

- Port ID: 8
- PBM Control Space Offset:
  - 600000 for 66MHz PCI bus (Bus A)
  - 700000 for 33MHz PCI bus (Bus B)

CODE EXAMPLE 4-7 shows the result of running the `show-devs` command on the 66MHz PCI bus and CODE EXAMPLE 4-8 on the 33MHz PCI bus.

CODE EXAMPLE 4-7 66MHz PCI Bus Devices

```
ok show-devs /pci@8,600000
/pci@8,600000/SUNW,qlc@4
/pci@8,600000/SUNW,qlc@4/fp@0,0
/pci@8,600000/SUNW,qlc@4/fp@0,0/disk
ok
```

CODE EXAMPLE 4-8 33MHz PCI Bus Devices

```
ok show-devs /pci@8,700000
/pci@8,700000/scsi@6,1
/pci@8,700000/scsi@6
/pci@8,700000/usb@5,3
/pci@8,700000/network@5,1
/pci@8,700000/ebus@5
/pci@8,700000/scsi@6,1/tape
/pci@8,700000/scsi@6,1/disk
/pci@8,700000/scsi@6/tape
/pci@8,700000/scsi@6/disk
/pci@8,700000/ebus@5/serial@1,400000
```

CODE EXAMPLE 4-8 33MHz PCI Bus Devices

```
ok show-devs /pci@8,700000
/pci@8,700000/ebus@5/lom-console@1,3083f8
/pci@8,700000/ebus@5/lombus@1,3062f8
/pci@8,700000/ebus@5/parallel@1,300278
/pci@8,700000/ebus@5/pmc@1,300700
/pci@8,700000/ebus@5/gpio@1,300600
/pci@8,700000/ebus@5/rtc@1,300070
/pci@8,700000/ebus@5/beep@1,32
/pci@8,700000/ebus@5/i2c@1,30
/pci@8,700000/ebus@5/i2c@1,2e
/pci@8,700000/ebus@5/power@1,30002e
/pci@8,700000/ebus@5/bbc@1,0
/pci@8,700000/ebus@5/flashprom@0,0
/pci@8,700000/ebus@5/lombus@1,3062f8/SUNW,lomv@0,0
/pci@8,700000/ebus@5/i2c@1,30/nvram@0,e0
/pci@8,700000/ebus@5/i2c@1,30/idprom@0,e0
/pci@8,700000/ebus@5/i2c@1,30/ioexp@0,74
/pci@8,700000/ebus@5/i2c@1,30/hardware-monitor@0,56
/pci@8,700000/ebus@5/i2c@1,30/hardware-monitor@0,54
/pci@8,700000/ebus@5/i2c@1,30/hardware-monitor@0,52
/pci@8,700000/ebus@5/i2c@1,30/ioexp@0,4c
/pci@8,700000/ebus@5/i2c@1,30/fan-control@0,4e
/pci@8,700000/ebus@5/i2c@1,30/lomlite2@0,ae
/pci@8,700000/ebus@5/i2c@1,30/power-supply@0,ac
/pci@8,700000/ebus@5/i2c@1,30/scc-reader@0,a6
/pci@8,700000/ebus@5/i2c@1,30/fcal-backplane@0,a4
/pci@8,700000/ebus@5/i2c@1,30/ioexp@0,7a
/pci@8,700000/ebus@5/i2c@1,30/ioexp@0,72
/pci@8,700000/ebus@5/i2c@1,30/motherboard-fru@0,a8
/pci@8,700000/ebus@5/i2c@1,30/fan-control@0,48
/pci@8,700000/ebus@5/i2c@1,30/temperature@0,98
/pci@8,700000/ebus@5/i2c@1,30/cpu-fru@0,a2
/pci@8,700000/ebus@5/i2c@1,30/temperature@0,30
/pci@8,700000/ebus@5/i2c@1,30/cpu-fru@0,a0
/pci@8,700000/ebus@5/i2c@1,2e/dimm-fru@1,ae
/pci@8,700000/ebus@5/i2c@1,2e/dimm-fru@1,ac
/pci@8,700000/ebus@5/i2c@1,2e/dimm-fru@1,aa
/pci@8,700000/ebus@5/i2c@1,2e/dimm-fru@1,a8
/pci@8,700000/ebus@5/i2c@1,2e/dimm-fru@1,a6
/pci@8,700000/ebus@5/i2c@1,2e/dimm-fru@1,a4
/pci@8,700000/ebus@5/i2c@1,2e/dimm-fru@1,a2
/pci@8,700000/ebus@5/i2c@1,2e/dimm-fru@1,a0
ok
```

TABLE 4-7 shows the child node names. When accessing a child device from the parent node, you must identify the child node name, PCI device number and PCI function number.

TABLE 4-7 Child Node Names

Description	Child Node Name	Comment
Serial Port	`serial`	Old name (se)
Parallel Port (off Ebus)	`parallel`	Old name (ecpp)
LOMlite2 Card	`lom-console`	
General Purpose I/O Port	`gpio`	
I2C Bus	`i2c`	
Real Time Clock	`rtc`	
BootBus Controller	`bbc`	
Flash PROM	`flashprom`	
Motherboard	`motherboard`	
Temperature Sensor	`temperature`	
CPU	`cpu`	
ID PROM (off I2C bus)	`idprom`	
NVRAM (off I2C bus	`nvram`	
Memory DIMM (off I2C bus)	`dimm`	

The following device ID field values are assigned to the Netra T4 system:

- Device ID 4: FC-AL
- Device ID 5: usb, ebus, eri, serial, parallel, gpio
- Device ID 6: Internal and external SCSI

Example: FC-AL Internal Disk Drive Path

```
/pci@8,60000/SUNW,qlc@4/fp@0,0/ssd@w2100002037653317,0
```

where (from left to right):

- `pci` represent the PCI bus
- `8` represents the Netra T4 platform
- `600000` represents 66MHz PCI
- `qlc` represents the FC-AL controller driver
- `4` is the FC-AL device number

- `fp` is the FC-AL port driver (HUB)
- `0,0` are the FC-AL HUB device number and FC-AL HUB function number
- `ssd` represents the disk driver
- w# is the World Wide ID number

Example SCSI Internal Disk Drive Path

```
/pci@8,7000000/scsi@6/sd@1,0
```

where (from left to right):

- `pci` represent the PCI bus
- `8` represents the Netra T4 platform
- `700000` represents 33MHz PCI
- `scsi` represents the SCSI controller driver
- `6` is the SCSI device number
- `sd` represents the SCSI disk driver
- `1,0` are the SCSI device number and SCSI function number

4.5.4 Running the Diagnostics

This section contains the following OpenBootDiag diagnostic information:

- Section 4.5.4.1, “OBDiag Tests” on page 4-19
- Section 4.5.4.2, “Starting the OBDiag Menu” on page 4-22
- Section 4.5.4.3, “SUNW,lomv@0,0” on page 4-24
- Section 4.5.4.4, “SUNW,qlc@4” on page 4-25
- Section 4.5.4.5, “bbc@1,0” on page 4-25
- Section 4.5.4.6, “ebus@5” on page 4-25
- Section 4.5.4.7, “flashprom@0,0” on page 4-26
- Section 4.5.4.8, “gpio@1,300600” on page 4-26
- Section 4.5.4.9, “i2c@1,2e” on page 4-26
- Section 4.5.4.10, “i2c@1,30” on page 4-27
- Section 4.5.4.11, “network@5,1” on page 4-27
- Section 4.5.4.12, “parallel@1,300278” on page 4-27
- Section 4.5.4.13, “pmc@1,300700” on page 4-28
- *Section 4.5.4.14, “ortc@1,300070” on page 4-28*
- Section 4.5.4.15, “scsi@6” on page 4-28
- Section 4.5.4.16, “scsi@6,1” on page 4-29
- Section 4.5.4.17, “serial@1,400000” on page 4-29
- Section 4.5.4.18, “usb@5,3” on page 4-29
- Section 4.5.4.19, “test-all” on page 4-30

Note – Set the `diag-level` variable to `min` prior to performing these tests. This can be done at the `ok prompt` or within the `obdiag` menu.

The OpenBoot diagnostic (OBDiag) is a menu-driven set of diagnostics that reside in flash PROM on the motherboard. OBDiag can isolate errors in the following system components:

- Motherboard
- DVD-ROM and DAT drives
- Hard drive
- Any option card that contains an onboard self-test

OBDiag performs root-cause failure analysis on the referenced devices by testing internal registers, confirming subsystem integrity, and verifying device functionality.

On the motherboard, OBDiag tests not only the motherboard but also its interfaces:

- PCI
- SCSI
- Ethernet
- Serial
- Parallel
- USB
- I2C
- FC-AL

4.5.4.1 OBDiag Tests

Each self-test executes independently and returns a zero if it completes successfully, or a non zero and an error report if it is unsuccessful. Diagnostic configuration variables determine the level of coverage, execution flow, and the corresponding output. These variables are configured using the `setenv` command.

TABLE 4-8 OBDiag Configuration Variables

Variable	Function	Possible Values	Default Value
`diag-level`	Determines how the tests are performed	`min`[1] `max`[2]	`min`
`diag-passes`	Defines the number of times the self-test method(s) are performed	#[3]	1

1. When `diag-level` is set to `min`, OBDiag performs abbreviated tests.
2. When `diag-level` is set to `max`, OBDiag performs extended tests.
3. Where “#” is the number of times the tests are performed (integer).

The new tests, and their features, for the Netra T4 system are summarized in TABLE 4-9.

TABLE 4-9 Netra T4 System-Specific OBDiag Self Tests

Test	Test Function
SUNW,lomv@0,0	LOMlite2 Selftest ■ Lomlite registers test
SUNW,qlc@4	FC-AL / SCSI Enclosure Services (SES) Subsystem Tests ■ FC-AL (ISP2200A) ■ PCI configuration space register test ■ FPM, FB, DMA, PBUI and RISC register test ■ Mailbox tests ■ Memory bank tests ■ RISC RAM test ■ FIFO load and unload test ■ Disk Tests ■ Read / Write / Restore test ■ Seek test ■ Random seek test ■ Hour glass seek test ■ Built-in self test (BIST) ■ SES Tests ■ Get supported diagnostic page test ■ Get configuration page test ■ Get enclosure status page test
bbc@1,0	BBC Self Test ■ Register test
ebus@5	RIO Ebus Self Test ■ PCI configuration space register test ■ Ebus register test ■ DMA register test ■ DMA functional test ■ TCR register test ■ AUX I / O register test
flashprom@0,0	Flash Self Test ■ Flash read test ■ Flash write test (manufacturing test only)
gpio@0,300600	Super I / O Self Test ■ General purpose I / O test
i2c@1,2e	I2C Self Test ■ I2C bus test

TABLE 4-9 Netra T4 System-Specific OBDiag Self Tests *(Continued)*

Test	Test Function
i2c@1,30	I2C Self Test ■ I2C bus test
network@5,1	RIO-GEM Self Test (10/100 Mbits) ■ PCI configuration space register test ■ RIO-GEM register test ■ Internal loopback (RIO-GEM level) ■ Internal loopback (Lucent 6612 PHY level) ■ External loopback (requires RJ45 loopback connector)
parallel@1,300278	SuperI/O Self Test ■ ECP and EPPP mode parallel port test (requires loopback connector)
pmc@1,300700	
rtc@1,300070	SuperI/O Self Test ■ Advanced power controller/Real time clock (TOD) test
scsi@6	SCSI (53C875) Self Test ■ SCSI (53C875) register test ■ SCSI timer test ■ SCSI DMA test ■ SCSI loopback test ■ SCSI wide transfer test ■ SCSI BIST test
scsi@6,1	SCSI (53C875) Self Test ■ SCSI (53C875) register test ■ SCSI timer test ■ SCSI DMA test ■ SCSI loopback test ■ SCSI wide transfer test ■ SCSI BIST test
serial@1,400000	Serial (SAB 82532) Self Test ■ Internal loopback test ■ External loopback test
usb@5,3	RIO-USB Self Test ■ PCI configuration space register test ■ USB HCI register test ■ Reset test

4.5.4.2 Starting the OBDiag Menu

OBDiag is started from the ok prompt and builds a dynamic menu created from the device tree, including those devices that have associated self-tests.

To start OBDiag:

1. **At the** ok **prompt, type:**

```
ok setenv mfg-mode on
mfg-mode = on
```

2. **Then type:**

```
ok setenv diag-switch? true
diag-switch? = true
```

3. **Then type:**

```
ok setenv auto-boot? false
auto-boot? = false
```

4. **Then type:**

```
ok reset-all
```

5. **Verify that the platform resets (see the following code example).**

CODE EXAMPLE 4-9 Typical reset-all Screen Output

```
ok reset-all
Resetting ...screen not found.
keyboard not found.
Keyboard not present.  Using lom-console for input and output.
Start Reason: Soft Reset
System Reset: (SPOR) (PLL)
Probing gptwo at 0,0 SUNW,UltraSPARC-III (750 MHz @ 5:1, 8 MB)
   memory-controller
Probing gptwo at 1,0 SUNW,UltraSPARC-III (750 MHz @ 5:1, 8 MB)
   memory-controller
Probing gptwo at 8,0 pci pci
Loading Support Packages: kbd-translator
Loading onboard drivers: ebus flashprom bbc power i2c dimm-fru dimm-fru
```

CODE EXAMPLE 4-9 Typical `reset-all` Screen Output *(Continued)*

```
    dimm-fru dimm-fru dimm-fru dimm-fru dimm-fru dimm-fru i2c cpu-fru
    temperature cpu-fru hardware-monitor hardware-monitor
    hardware-monitor temperature fan-control fan-control motherboard-fru
    ioexp ioexp ioexp fcal-backplane scc-reader lomlite2 nvram idprom
    beep rtc gpio pmc parallel lombus SUNW,lomc serial lomp lomv
Memory Configuration:
Segment @ Base:        0  Size:  2048 MB ( 4-Way)
SUNW,Netra-T4
Probing /pci@8,600000 Device 4  SUNW,qlc fp disk
Probing /pci@8,600000 Device 1  Nothing there
Probing /pci@8,700000 Device 5  network usb
Probing /pci@8,700000 Device 6  scsi disk tape scsi disk tape
Probing /pci@8,700000 Device 1  Nothing there
Probing /pci@8,700000 Device 2  Nothing there
Probing /pci@8,700000 Device 3  Nothing there
Probing /pci@8,700000 Device 4  Nothing there

Sun Netra T4 (2 X UltraSPARC-III) , No Keyboard
Copyright 1998-2001 Sun Microsystems, Inc.  All rights reserved.
OpenBoot 4.2, 2048 MB memory installed, Serial #16458092.
Ethernet address 8:0:20:fb:21:6c, Host ID: 80fb216c.
{0} ok
```

6. **At the** `ok` **prompt, type** `obdiag`**. Verify that the OBDiag menu is displayed (**CODE EXAMPLE 4-10**).**

CODE EXAMPLE 4-10 `obdiag` Menu

```
                              o b d i a g

1 SUNW,lomv@0,0          2 SUNW,qlc@4               3 bbc@1,0
4 ebus@5                 5 flashprom@0,0            6 gpio@1,300600
7 i2c@1,2e               8 i2c@1,30                 9 network@5,1
10 parallel@1,300278     11 pmc@1,300700            12 rtc@1,300070
13 scsi@6                14 scsi@6,1                15 serial@1,400000
16 usb@5,3
|Commands:test test-all except help what printenvs setenv versions exit|
```

The following menu is displayed when the `help` command is executed:

TABLE 4-10 `obdiag` Help

Command	Description
`exit`	Exits obdiag tool
`help`	Prints this help information
`setenv`	Sets diagnostic configuration variable to new value
`printenvs`	Prints values for diagnostic configuration variables
`versions`	Prints self tests, library and obdiag tool versions
`test-all`	Tests all devices displayed in the menu
`test 1,2,5`	Tests devices 1, 2 and 5
`except 2,5`	Tests all devices except devices 2 and 5
`what 1,2,5`	Prints some selected properties for devices 1, 2, and 5

4.5.4.3 SUNW,lomv@0,0

The following code example shows the lomv test output:

CODE EXAMPLE 4-11 `SUNW,lomv@0,0` Diagnostic Output Message

```
obdiag> test 1
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/lombus@1,3062f8/SUNW,lomv@0,0
.......... passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:0

Hit any key to return to the main menu
```

4.5.4.4 SUNW,qlc@4

The following code example shows the QLC test output.

CODE EXAMPLE 4-12 SUNW,qlc@4 Diagnostic Output Message

```
obdiag> test 2
Hit the spacebar to interrupt testing
Testing /pci@8,600000/SUNW,qlc@4
..................................... passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:0

Hit any key to return to the main menu
```

4.5.4.5 bbc@1,0

The following code example shows the bbc@1,0 output message.

CODE EXAMPLE 4-13 bbc@1,0 Diagnostic Output Message

```
obdiag> test 3
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/bbc@1,0
.............................. passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:0

Hit any key to return to the main menu
```

4.5.4.6 ebus@5

The following code example shows the ebus output message.

CODE EXAMPLE 4-14 ebus@5 Diagnostic Output Message

```
obdiag> test 4
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5
..................................... passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:2

Hit any key to return to the main menu
```

4.5.4.7 flashprom@0,0

The following code example shows the flashprom output message.

CODE EXAMPLE 4-15 flashprom@0,0 Diagnostic Output Message

```
obdiag> test 5
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/flashprom@0,0
.......................... passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:3

Hit any key to return to the main menu
```

4.5.4.8 gpio@1,300600

The following code example shows the gpio output message.

CODE EXAMPLE 4-16 gpio@1,300600 Diagnostic Output Message

```
obdiag> test 6
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/gpio@1,300600
.......................... passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:0

Hit any key to return to the main menu
```

4.5.4.9 i2c@1,2e

The following code example shows the i2c1,2e output message.

CODE EXAMPLE 4-17 i2c@1,2e Diagnostic Output Message with TIP Line Installed

```
obdiag> test 7
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/i2c@1,2e
.............................. passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:0

Hit any key to return to the main menu
```

4.5.4.10 i2c@1,30

The following code example shows the i2c1,30 output message.

CODE EXAMPLE 4-18 i2c@1,30 Diagnostic Output Message

```
obdiag> test 8
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/i2c@1,30
.............................. passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:0

Hit any key to return to the main menu
```

4.5.4.11 network@5,1

The following code example shows the network@5,1 output message.

CODE EXAMPLE 4-19 network@5,1 Diagnostic Output Message

```
obdiag> test 9
Hit the spacebar to interrupt testing
Testing /pci@8,700000/network@5,1
................................... passed

Hit any key to return to the main menu
```

4.5.4.12 parallel@1,300278

The following code example shows the parallel port output message.

CODE EXAMPLE 4-20 parallel@1,300278 Diagnostic Output Message

```
obdiag> test 10
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/parallel@1,300278
....................... passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:0

Hit any key to return to the main menu
```

4.5.4.13 pmc@1,300700

The following code example shows the pmc@1,300700 output message.

CODE EXAMPLE 4-21 pmc@1,300700 Diagnostic Output Message

```
bdiag> test 11
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/pmc@1,300700
.............................. passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:0

Hit any key to return to the main menu
```

4.5.4.14 ortc@1,300070

The following code example shows the rtc@1,300070 output message.

CODE EXAMPLE 4-22 rtc@1,300070 Diagnostic Output Message

```
obdiag> test 12
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/rtc@1,300070
.............................. passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:5

Hit any key to return to the main menu
```

4.5.4.15 scsi@6

The following code example shows the scsi@6 output message

CODE EXAMPLE 4-23 scsi@6 Diagnostic Output Message

```
obdiag> test 13
Hit the spacebar to interrupt testing
Testing /pci@8,700000/scsi@6
.......................................... passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:5

Hit any key to return to the main menu
```

4.5.4.16 scsi@6,1

The following code example shows the scsi@6,1 output message.

CODE EXAMPLE 4-24 scsi@6,1 Diagnostic Output Message

```
obdiag> test 14
Hit the spacebar to interrupt testing
Testing /pci@8,700000/scsi@6,1
..................................... passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:5

Hit any key to return to the main menu
```

4.5.4.17 serial@1,400000

The following code example shows the serial output message.

CODE EXAMPLE 4-25 serial@1,400000 Diagnostic Output Message

```
obdiag> test 15
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/serial@1,400000
....................... passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:1

Hit any key to return to the main menu
```

4.5.4.18 usb@5,3

The following code example shows the USB output message.

CODE EXAMPLE 4-26 usb@5,3 Diagnostic Output Message

```
obdiag> test 16
Hit the spacebar to interrupt testing
Testing /pci@8,700000/usb@5,3
..................................... passed
Pass:1 (of 1) Errors:0 (of 0) Tests Failed:0 Elapsed Time: 0:0:0:0

Hit any key to return to the main menu
```

4.5.4.19 test-all

The test-all diagnostic runs all tests in sequence.

Note – You can exclude certain tests using the except command.

The following code example shows the test-all output message.

CODE EXAMPLE 4-27 test-all Diagnostic Output Message

```
obdiag> test-all
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/lombus@1,3062f8/SUNW,lomv@0,0 ......... passed
Testing /pci@8,600000/SUNW,qlc@4 ..................................... passed
Testing /pci@8,700000/ebus@5/bbc@1,0 ................................. passed
Testing /pci@8,700000/ebus@5 ......................................... passed
Testing /pci@8,700000/ebus@5/flashprom@0,0 ........................... passed
Testing /pci@8,700000/ebus@5/gpio@1,300600 ........................... passed
Testing /pci@8,700000/ebus@5/i2c@1,2e ................................ passed
Testing /pci@8,700000/ebus@5/i2c@1,30 ................................ passed
Testing /pci@8,700000/network@5,1 .................................... passed
Testing /pci@8,700000/ebus@5/parallel@1,300278 ....................... passed
Testing /pci@8,700000/ebus@5/pmc@1,300700 ............................passed
Testing /pci@8,700000/ebus@5/rtc@1,300070 ............................passed
Testing /pci@8,700000/scsi@6 ......................................... passed
Testing /pci@8,700000/scsi@6,1 ....................................... passed
Testing /pci@8,700000/ebus@5/serial@1,400000 .........................passed
Testing /pci@8,700000/usb@5,3 ........................................passed
Hit any key to return to the main menu
```

4.6 OpenBoot Emergency Procedures

The following paragraphs describe how to emulate the functions of the Stop-commands from the lom> prompt.

4.6.1 Stop-A

To emulate Stop-A, type **break** at the lom> prompt.

4.6.2 Stop-N

To emulate Stop-N, type **bootmode reset_nvram** at the lom> prompt.

4.6.3 Stop-F

To emulate Stop-F, type **bootmode forth** at the lom> prompt.

4.6.4 Stop-D

To emulate Stop-D (diags), type **bootmode diag** at the lom> prompt.

CHAPTER 5

Before Servicing the System

This chapter lists the tools you will need to install or remove components, describes the function of the system ON/STBY switch, states the antistatic precautions that must be taken before working on the Netra T4 system, describes how to access system unit, and describes how to change the air filters.

The chapter contains the following sections:

- Section 5.1, “Accessibility” on page 5-1
- Section 5.2, “Tools” on page 5-2
- Section 5.3, “System ON/STBY Switch” on page 5-2
- Section 5.4, “Disconnection and Isolation” on page 5-5
- Section 5.5, “Antistatic Precautions” on page 5-5
- Section 5.6, “Top Access Cover” on page 5-8
- Section 5.7, “Front Fascia” on page 5-10
- Section 5.8, “Air Filter” on page 5-12

5.1 Accessibility

The following components can be accessed while the system is in the rack:

- PSU
- Front fascia
- Air filter
- Hard drive units

Access to all other components requires removal of the top cover. This is achieved by sliding the unit from the rack, if it is mounted on rails and there is sufficient height above the unit to work, or removing the unit from the rack and carrying out the procedure on a work bench.

Caution – Owing to the weight of the unit, two persons are required to remove the unit from and replace it in the rack.

5.2 Tools

To perform the removal and fitting procedures described in Part 1 of this manual, you will need the following tools:

- Phillips No. 2 screwdriver, stubby
- Phillips No. 2 screwdriver, 15cm (6in.)
- Phillips No. 1 screwdriver, 10cm (4in.)
- 6mm (0.25 in.) flat blade screwdriver, stubby
- Grounding wrist strap
- Anti-static mat
- Torque tool (supplied with the system and located inside the system chassis)

5.3 System ON / STBY Switch

The Netra T4 system switch is a rocker, momentary switch that functions as a standby device only, controlling logic circuits that enable power module output.

5.3.1 Powering On the System

Before powering on, inspect the supply conductors for mechanical security.

5.3.1.1 Netra T4 AC100 System

1. **Plug the AC power cord into the appliance inlet on the PSU and into the mains supply.**
2. **Set the front panel ON/STBY system switch to the ON | position and hold it until the system starts to power up, or use the LOMlite2** `poweron` **command or OBP** `poweron` **command.**

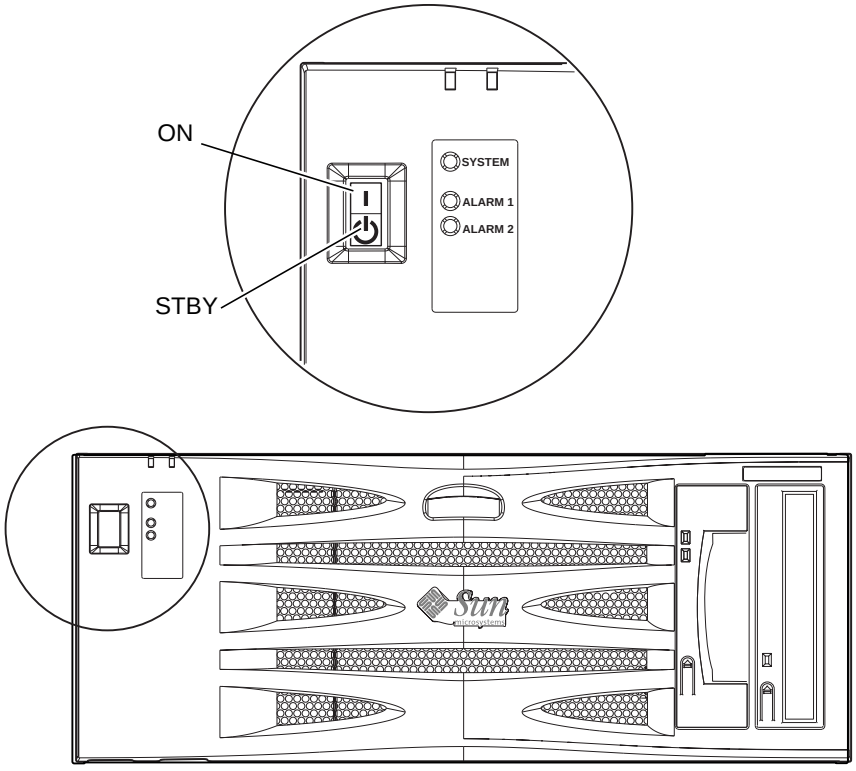


FIGURE 5-1 System Power On/STBY (Front Panel)

5.3.1.2 Netra T4 DC100 System

1. **Insert both DC input connectors.**
2. **Close both DC circuit breakers.**
3. **Momentarily set the front panel ON/STBY system switch to the ON | position and hold it until the system starts to power up.**

5.3.2 Powering Off the System

Caution – Before you turn off power to the system, back up the files and exit from the operating environment. Failure to do so may result in data loss.

Where necessary, notify the users that the system is going down.

5.3.2.1 Netra T4 AC100 System

1. **Follow step a. or b., as appropriate.**

   a. **Halt the operating environment.**

      Set the ON/STBY switch at the front of the system to the STBY ⏻ position and hold it until the system shuts down (this can take several seconds) or use the LOMlite2 `poweroff` **command or OBP** `power-off` **command.**

   b. **Set the ON/STBY switch at the front of the system to the STBY ⏻ position and release it immediately to initiate a clean shut down followed by a power off.**

2. **Verify that the Power LED is off.**

3. **Disconnect the AC power cord from the rear of the system.**

Caution – Regardless of the position of the ON/STBY switch, when an AC power cord remains connected to the system, hazardous voltage could be present within the power supply.

5.3.2.2 Netra T4 DC100 System

1. **Follow step a. or b., as appropriate.**

   a. **Halt the operating environment.**

      Set the ON/STBY switch at the front of the system to the STBY ⏻ position and hold it until the system shuts down (this can take several seconds) or use the LOMlite2 `poweroff` **command or OBP** `power-off` **command.**

   b. **Set the ON/STBY switch at the front of the system to the STBY ⏻ position and release it immediately to initiate a clean shut down followed by a power off.**

2. **Verify that the Power LED is off.**

3. **Open both DC circuit breakers.**

4. **Detach both DC input connectors.**

5.4 Disconnection and Isolation

5.4.1 Netra T4 AC100 System

The disconnect devices for servicing are defined as:

- The appliance inlet on the rear of the system
- The circuit breakers in the rack in which the system is mounted
- The mains plug

5.4.2 Netra T4 DC100 System

The disconnect devices for servicing are defined as:

- The circuit breakers in *both* negative supply conductors
- *Both* DC input connectors

5.5 Antistatic Precautions

Caution – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system unit components, use an antistatic wrist strap with a 10mm press stud connection and attach the antistatic wrist strap to the press stud at the rear or front of the chassis before removing the top access cover.

5.5.1 Attaching the Antistatic Wrist Strap

To attach the antistatic wrist strap to the chassis, connect the strap as shown in or FIGURE 5-3**.**

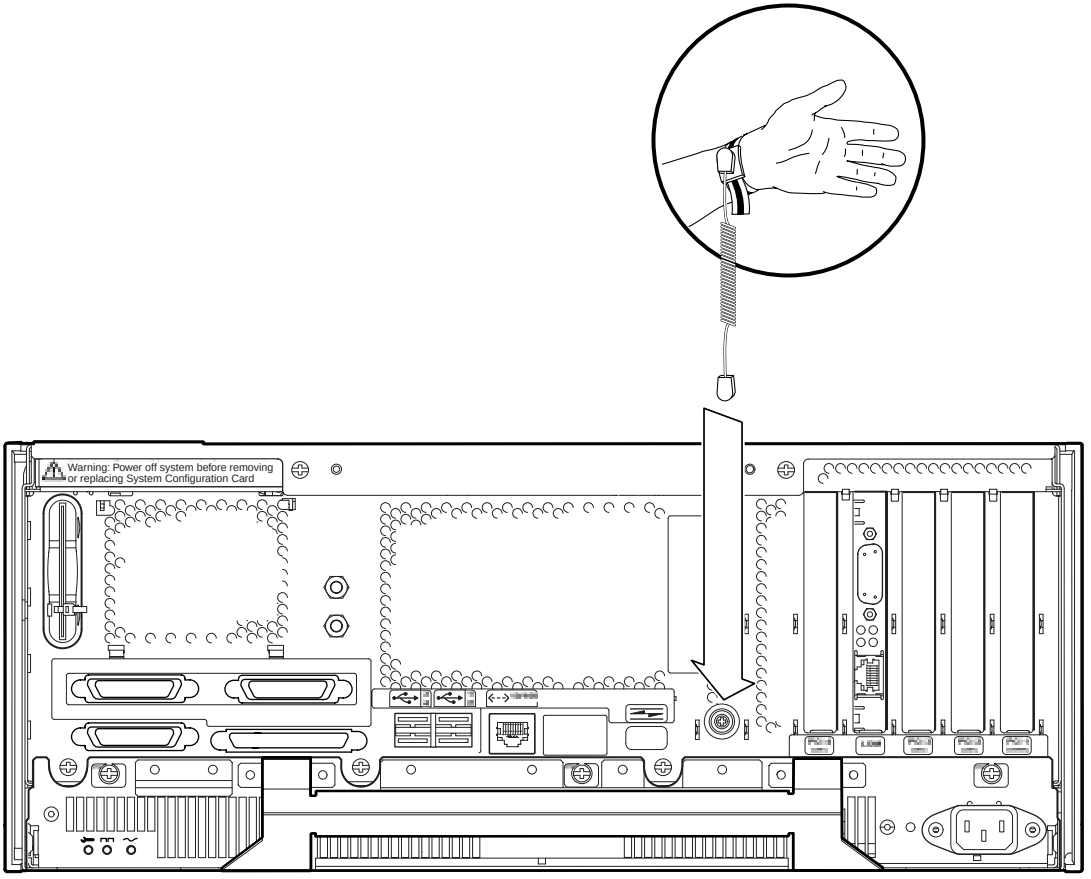


FIGURE 5-2 Attaching the Antistatic Wrist Strap to the Rear of the Chassis

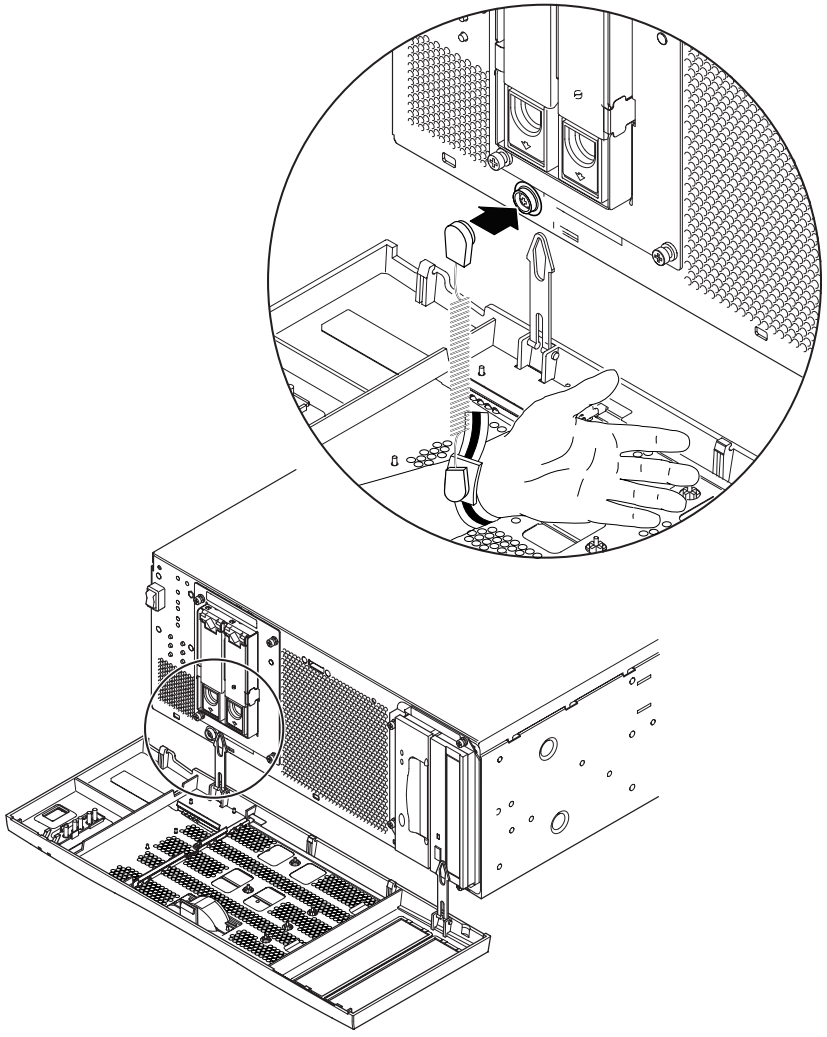


FIGURE 5-3 Attaching the Antistatic Wrist Strap to the Front of the Chassis

5.6 Top Access Cover

The top access cover is secured by two captive screws located at the rear of the system.

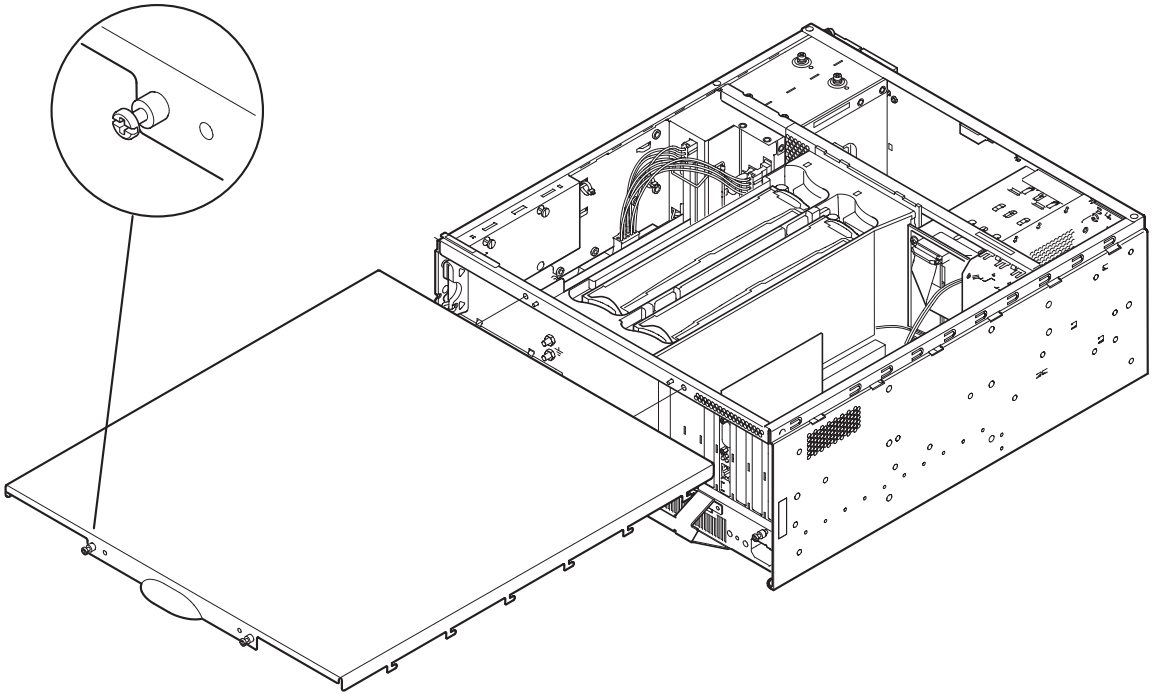


FIGURE 5-4 Top Access Cover

Only the PSU, hard disk drives, front fascia and air filter can be accessed without removing the top cover. If there is sufficient clearance above the unit and it is mounted on slide rails, you should be able to carry out servicing with the system in the rack. Otherwise you must remove the system from the rack and service it on a bench.

Caution – The unit is heavy and requires two people to remove it from and install it in the rack.

Note – Beryllium copper EMI shielding gaskets are attached to the under surface of the access cover. Handle the access cover carefully to avoid damaging the gaskets.

5.6.1 Preparation

Before proceeding to remove the top access cover, carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and remove the power.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

Caution – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system unit components, attach an ESD Strap to the wrist, then to the connection point provided on the rear of system, and only then remove the power cord from the system unit. Following this caution equalizes all electrical potentials with the system unit.

5.6.2 Removing the Top Access Cover

1. **Carry out the appropriate steps listed in Section 5.6.1, “Preparation” on page 5-9.**
2. **Release the two captive Phillips screws from the rear of the access cover.**
3. **Push the cover away from the front of the chassis to disengage the lugs and lift it off.**

   When handling the access cover, ensure that you do not damage the EMI shielding gaskets on the underside of the cover.

5.6.3 Fitting the Top Access Cover

1. **Carry out the appropriate steps listed in Section 5.6.1, “Preparation” on page 5-9 as required.**
2. **With the fixing screws on the access cover towards the rear of the system chassis, locate the lugs on the access cover in the slots on the side panels of the system chassis (see** FIGURE 5-4**).**
3. **Slide the access cover forward to engage the lugs.**

   Ensure that the rear of the access cover is flush with the rear of the system chassis.

4. **Tighten the two captive Phillips screws to secure the access cover.**

5.7 Front Fascia

The detachable front fascia houses the optional air filter and is fastened to the system chassis at the bottom edge by two plastic tethers. You need to detach the fascia completely only to change the filter (to avoid dust from the filter being sucked back into the system); you can carry out all other procedures by lowering the fascia and leaving the tethers attached.

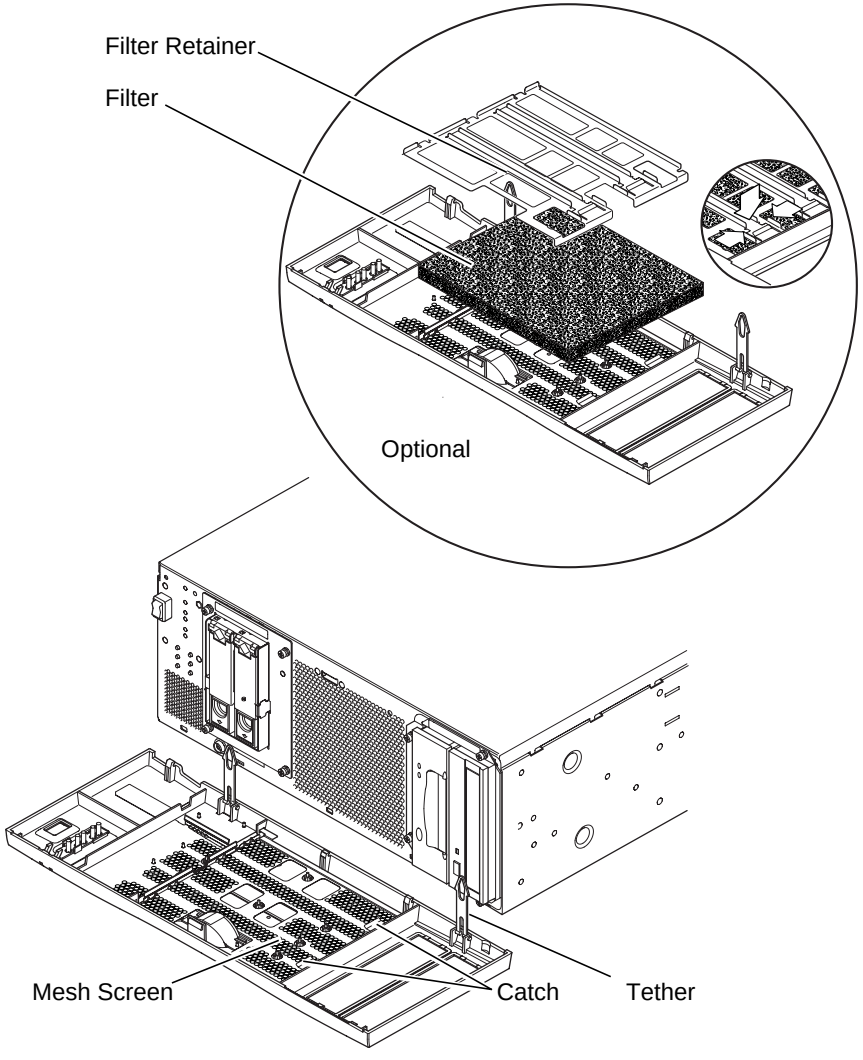


FIGURE 5-5 Front Fascia and Filters

5.7.1 Removing the Front Fascia

Caution – Exercise care when opening the fascia. You must detach the plastic locating pegs on the bottom edge of the fascia before lowering it.

1. **Pull the fascia away from the top of the chassis not more than 2.5cm (1in.) using the finger hold in the middle of the fascia.**
2. **Lift the fascia forward and off the locating pegs on the bottom edge of the fascia.**
3. **Swing the fascia forward and down so that it hangs on the two plastic tethers.**

5.7.1.1 Detaching the Fascia Tethers

4. **Squeeze together the sides of each plastic tether and pull it from the system chassis.**
5. **Similarly, squeeze together the sides of the tether to detach each locating pin in turn from the retainers on the fascia.**

5.7.2 Fitting the Front Fascia

Follow Step 1 through Step 5 if you are refitting the tethers to the fascia, otherwise start at Step 6.

1. **Insert one side of the locating pin on the tether in the retainer on the fascia.**
2. **Squeeze the sides of the tether together to insert the other locating pin.**
3. **Repeat Step 1 and Step 2 for the other tether.**
4. **Insert the other end of one of the tethers in the corresponding slot in system chassis.**

   If the tether is a tight fit, squeeze the sides of the tether together.
5. **Repeat Step 4 for the other tether.**

6. **Swing the fascia up until it is nearly vertical and insert the locating pegs on the bottom of the fascia in the slots on the system chassis.**

Caution – Do not swing the fascia forward once you have inserted the locating pegs or they may break.

---

7. **Press the top of the fascia forward until the catch on the fascia clicks into place on the system chassis.**

5.8 Air Filter

If required, you can replace the black mesh screen located behind the front fascia with the optional foam air filter and metal retainer supplied with the system (see FIGURE 5-5). Clean or replace the filter regularly to maintain the airflow through the system.

Caution – To ensure that dust is not sucked into the system when you replace the filter, remove the fascia completely from the system before proceeding.

5.8.1 Removing and Fitting the Mesh Screen

1. **Detach the front fascia and place it on a workbench away from the immediate vicinity of the system.**

   See Section 5.7.1, “Removing the Front Fascia” on page 5-11.

2. **Press the two catches on the mesh screen and lift that side away from the fascia.**

3. **Carefully disengage the two tabs at the other side from the fascia and lift out the screen.**

   Take care that you do not damage the plastic locating lugs when you detach the screen.

4. **Continue with Step a or Step b, as required.**

   a. **Replace with a foam filter and retainer as described in Step 4 through Step 6 in Section 5.8.2, “Replacing the Filter” on page 5-13.**

   b. **Continue from the following step to replace the screen.**

5. **Insert the locating tabs one side of the mesh screen into the corresponding slots on the fascia.**
6. **Carefully swing the other side down until the catches on the screen engage with the fascia.**
7. **Re-attach the fascia to the system chassis.**

   See Section 5.7.2, “Fitting the Front Fascia” on page 5-11.

5.8.2 Replacing the Filter

1. **If not already removed, detach the front fascia and place it on a workbench away from the immediate vicinity of the system.**

   See Section 5.7.1, “Removing the Front Fascia” on page 5-11.
2. **Release the two clips securing the filter retainer and lift it from the fascia.**
3. **Remove the filter and carefully dispose of it.**
4. **Clean the fascia to remove any remaining dust.**
5. **Insert a new filter and secure it with the retainer.**
6. **Re-attach the fascia to the system chassis.**

   See Section 5.7.2, “Fitting the Front Fascia” on page 5-11.

CHAPTER 6

Power Subassemblies

This chapter describes procedures for removing and replacing the power subassemblies of the Netra T4 system unit.

The chapter contains the following sections:

- Section 6.1, “Power Supply Unit” on page 6-1
- Section 6.2, “Power Distribution Board” on page 6-4
- Section 6.3, “System Switch and LED Assembly” on page 6-8

Caution – The plug at the end of the AC power cord is the primary means of disconnection for the Netra T4 AC100 system.

Caution – To isolate the Netra T4 DC100 system, open the circuit breakers in both negative supply conductors.

6.1 Power Supply Unit

The PSU is located below the motherboard and is accessed from the rear of the system. The method of removal is the same for the AC and DC PSUs.

6.1.1 Preparation

Before proceeding to remove the PSU, carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and power off the system.**
   See Section 5.3.2, “Powering Off the System” on page 5-4.

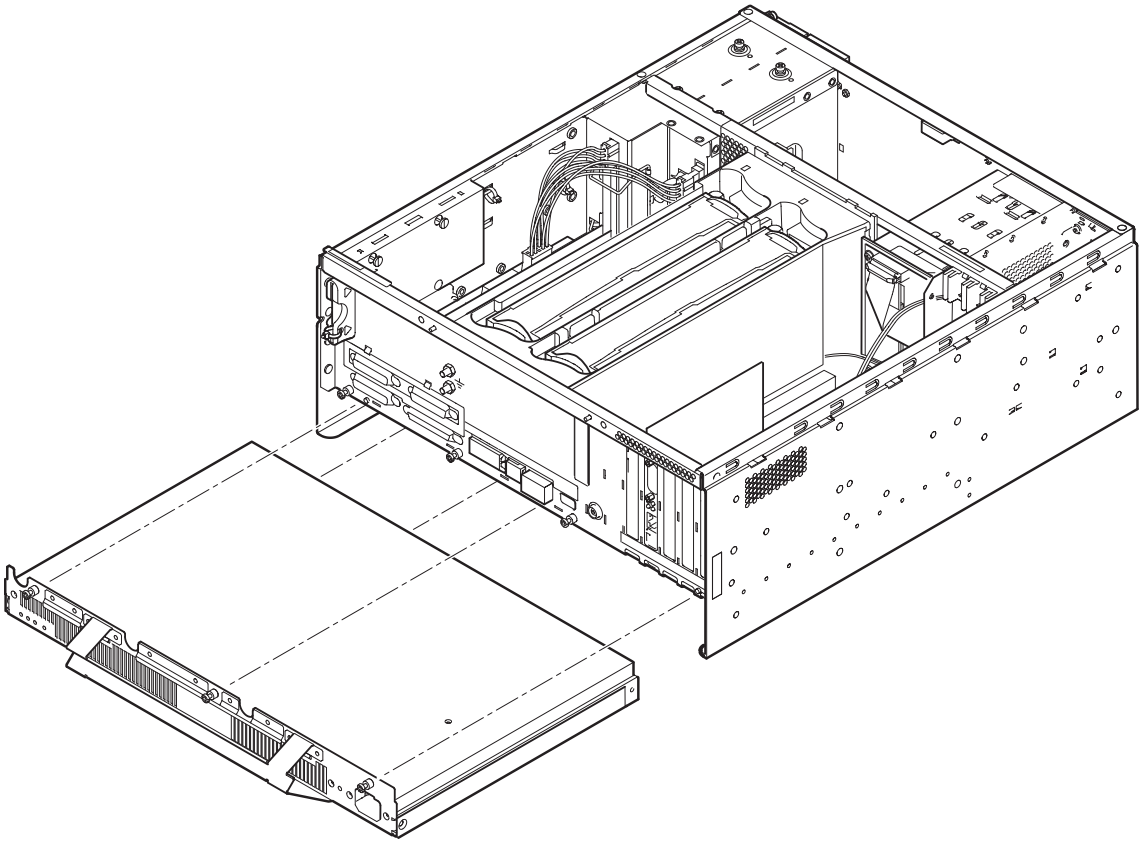


FIGURE 6-1 Power Supply Unit

6.1.2 Removing the PSU

1. **Perform the appropriate steps listed in Section 6.1.1, “Preparation” on page 6-1.**
2. **Remove the power cord from the PSU.**
3. **Release the three captive Phillips screws (colored purple) located along the top of the PSU that secure it to the system chassis.**

4. **Ensure that the system chassis cannot move then pull briefly on the PSU handle to detach the PSU from the Power Distribution Board (PDB).**

   If you are working on a bench, you may require an additional person to hold the system chassis steady while you disengage the PSU.

5. **Using the PSU handle, gently withdraw the PSU from the system chassis and place it on an antistatic mat.**

Note – Lay the PSU flat on the mat; do not stand it on its front edge.

6.1.3 Installing the PSU

1. **Perform the steps, as required, listed in Section 6.1.1, “Preparation” on page 6-1.**
2. **From the rear of the system, locate the PSU in its bay in the base of the system.**
3. **Gently slide the PSU into its bay until it starts to engage the connectors on the PDB.**
4. **Engage the connectors by pushing the PSU firmly into place until the rear plate on the PSU is flush against the rear of the system chassis.**

   If you are working on a bench, you may require an additional person to hold the system chassis steady while you engage the connectors.

5. **Tighten the three captive phillips screws (colored purple) to secure the PSU to the system chassis.**
6. **Reconnect the power connector to the PSU appliance inlet.**

6.2 Power Distribution Board

The power distribution board (PDB) receives power from the PSU and distributes it to the motherboard connectors, drive units and system fans,

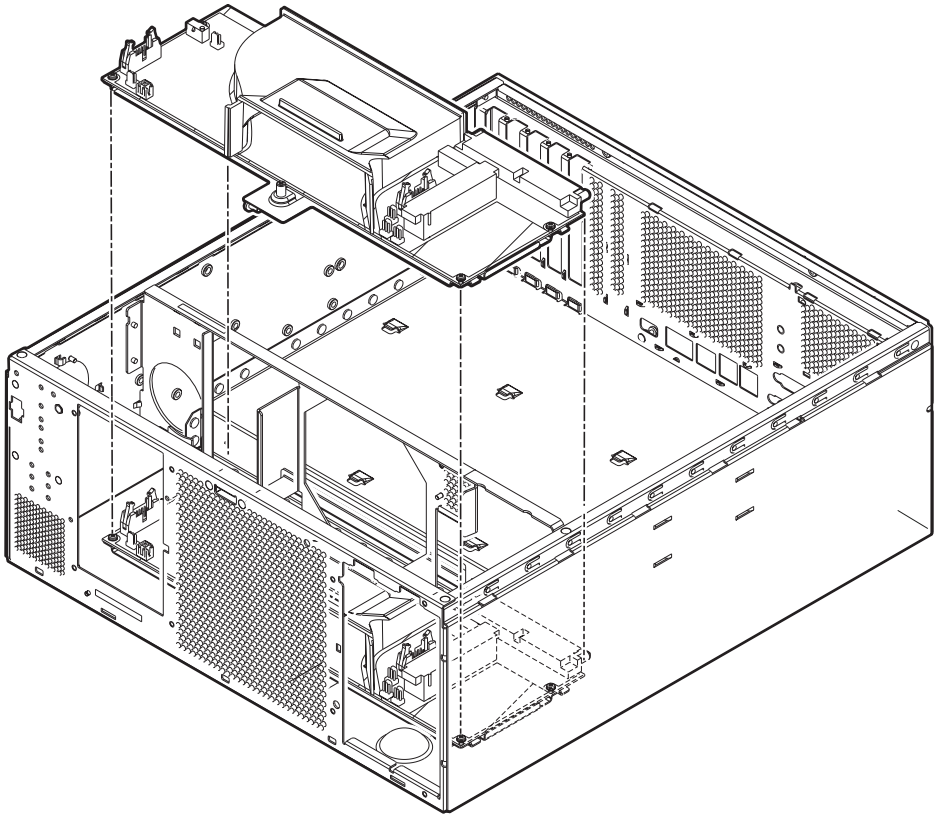


FIGURE 6-2 Power Distribution Board

6.2.1 Preparation

Before proceeding to remove a power distribution board (PDB), carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and power off the system.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

4. **Detach the PSU from the PDB connector by performing Step 2 through Step 4 of the PSU removal procedure.**

   Note that it is not necessary to remove the PSU from the system completely. See Section 6.1.2, “Removing the PSU” on page 6-2.

5. **Remove the Removable Media Module (RMM).**

   See Section 8.3.2, “Removing a Removable Media Module” on page 8-11.

6. **Remove the FC-AL disk drive assembly.**

   See Section 8.2.2, “Removing the FC-AL Backplane and Drive Bay” on page 8-8.

7. **Remove the CPU fan assembly.**

   See Section 7.2.2, “Removing the CPU Fan Assembly” on page 7-7.

8. **Remove the PSU fans assembly.**

   See Section 7.1.2, “Removing the PSU Fans Assembly” on page 7-4.

9. **Remove the CPU shroud cover.**

   See Section 9.2.2, “Removing a CPU Module” on page 9-6.

6.2.2 Removing the PDB

1. **Perform the steps, as required, listed in Section 6.2.1, “Preparation” on page 6-4.**

2. **Disconnect the large black 14-way power cable at J2 on the PDB by pressing the side locking lugs on the connector and pulling it away from the socket.**

   The cable connects to J3604 on the motherboard.

3. **Disconnect the small white 14-way power cable at J3 on the PDB by pressing the central locking lug at the back of the connector and pulling it away from the socket.**

   The cable is connected to J3603 on the motherboard.

4. **Disconnect the I2C ribbon cable from J4 on the PDB by opening the retaining lugs at each end of the socket and pulling out the connector.**

   The I2C cable is connected to J3604 on System Configuration Card Reader (SCCR) board.

5. **Disconnect the FC-AL drive fan at J16 on the PDB.**
6. **Disconnect the cable at J3302 on the motherboard.**

   This cable is connected to J10 on the PDB.
7. **Disconnect the cable at J3303 on the motherboard.**

   This cable is connected to J8 on the PDB.
8. **Disconnect the power interlock cable at J3602 on the motherboard.**

   The power interlock cable connects to J14 on the PDB.
9. **Disconnect the ON/STBY switch and LED cable at J15 on the PDB by opening the retaining lugs at each end of the socket and pulling out the connector.**
10. **Remove the single captive Phillips screw retaining the PDB.**

    See FIGURE 6-2.
11. **Slide the PDB towards the front of the system and lift it from the chassis.**
12. **Place the PDB on the antistatic mat.**

6.2.3 Installing the PDB

1. **Perform the steps, as required, listed in Section 6.2.1, “Preparation” on page 6-4.**
2. **Locate the PDB in the chassis with the fixing screw towards the front of the system and align the cut-outs in the metal shielding on the base of the PDB with the three hooks in the base of the chassis.**
3. **Ensure that the PSU connector and the plastic air guide on the PDB align with the cut-outs in the chassis, then slide the PDB towards the rear of the chassis to engage the hooks.**
4. **Tighten the single captive Phillips screw to secure the PDB to the chassis.**
5. **Reconnect the ON/STBY switch and LED cable at J15 on the PDB by inserting the connector in the socket and closing the retaining lugs at each end of the socket.**
6. **Reconnect the power interlock cable from J14 on the PDB to J3602 on the motherboard.**
7. **Reconnect the cable from J8 on the PDB to J3303 on the motherboard.**
8. **Reconnect the cable from J10 on the PDB to J3302 on the motherboard.**
9. **Reconnect the FC-AL drive fan to J16 on the PDB.**

10. **Refit the PSU fan assembly.**

    See Section 7.1.3, “Installing the PSU Fans Assembly” on page 7-4.

11. **Refit the CPU fan assembly.**

    See Section 7.2.3, “Installing the CPU Fan Assembly” on page 7-7.

12. **Reconnect the I2C ribbon cable from J3604 on the SCCR board to J4 on the PDB by inserting the connector in the socket and closing the retaining lugs at each end of the socket.**

13. **Reconnect the small white 14-way power cable from J3603 on the motherboard to J3 on the PDB by inserting the connector until the central locking lug at the back of the connector clicks into place.**

14. **Reconnect the large black 14-way power cable from J3604 on the motherboard to J2 on the PDB by inserting the connector until the two locking lugs at each end of the connector click into place.**

15. **Refit the CPU shroud.**

    See Section 9.2.3, “Installing a CPU Module” on page 9-7.

16. **Refit the FC-AL disk drive assembly.**

    See Section 8.2.3, “Installing the FC-AL Backplane and Drive Bay” on page 8-9.

17. **Refit the RMM assembly.**

    See Section 8.3.3, “Installing a Removable Media Module” on page 8-12.

18. **Engage the PSU connector with the PDB by performing Step 4 through Step 6 of the PSU fitting procedure.**

    See Section 6.1.3, “Installing the PSU” on page 6-3.

19. **Refit the top access cover.**

    See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

6.3 System Switch and LED Assembly

The system switch and LEDs are mounted on a card attached to the front of the chassis by four spring-loaded pins (see FIGURE 6-3). The LEDs are transmitted to the front fascia by light pipes attached to the inside of the front fascia.

6.3.1 Preparation

Before proceeding to remove the system switch and LED assembly, carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and remove the power.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

4. **Remove the FC-AL drive assembly.**

   See Section 8.2.2, “Removing the FC-AL Backplane and Drive Bay” on page 8-8.

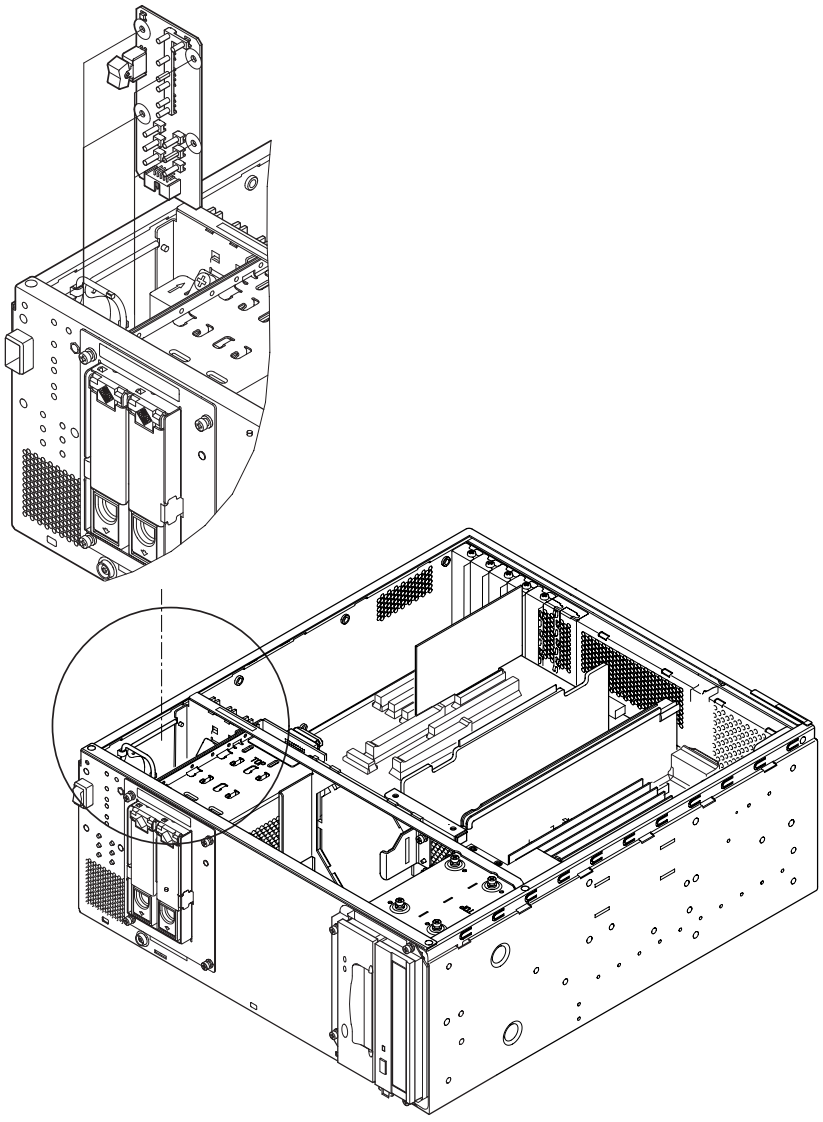


FIGURE 6-3 System Switch and LED Assembly

6.3.2 Removing the System Switch and LED Assembly

1. **Perform the steps, as required, listed in Section 6.3.2, “Removing the System Switch and LED Assembly” on page 6-10.**
2. **Gently prise the board from the four retaining spring-loaded pins.**

   Apply pressure evenly at each pin during removal to ensure that you do not bend the board.
3. **Disconnect the ribbon cable at J201 on the LED board.**
4. **Place the assembly on an antistatic mat.**

6.3.3 Installing the System Switch and LED Assembly

1. **Perform the steps, as required, listed in Section 6.3.2, “Removing the System Switch and LED Assembly” on page 6-10.**
2. **Reconnect the ribbon cable from J15 on the PDB and J0302 on the LOMlite2 board to J201 on the LED board**
3. **Locate the assembly on the four mounting pins on the inside of the chassis front panel.**

   See FIGURE 6-3.
4. **Apply pressure evenly at all four pins until the board is securely located on the pins.**
5. **Refit the top access cover.**

   See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

CHAPTER 7

Fan Subassemblies

This chapter contains procedures for removing and replacing the two fan subassemblies of the Netra T4 system unit, as shown in FIGURE 7-1.

The chapter contains the following sections:

- Section 7.1, “PSU Fans” on page 7-2
- Section 7.2, “CPU Fan Assembly” on page 7-5

Caution – The plug at the end of the AC power cord is the primary means of disconnection for the Netra T4 AC 100 system.

Caution – To isolate the Netra T4 DC100 system, open the circuit breakers in both negative supply conductors.

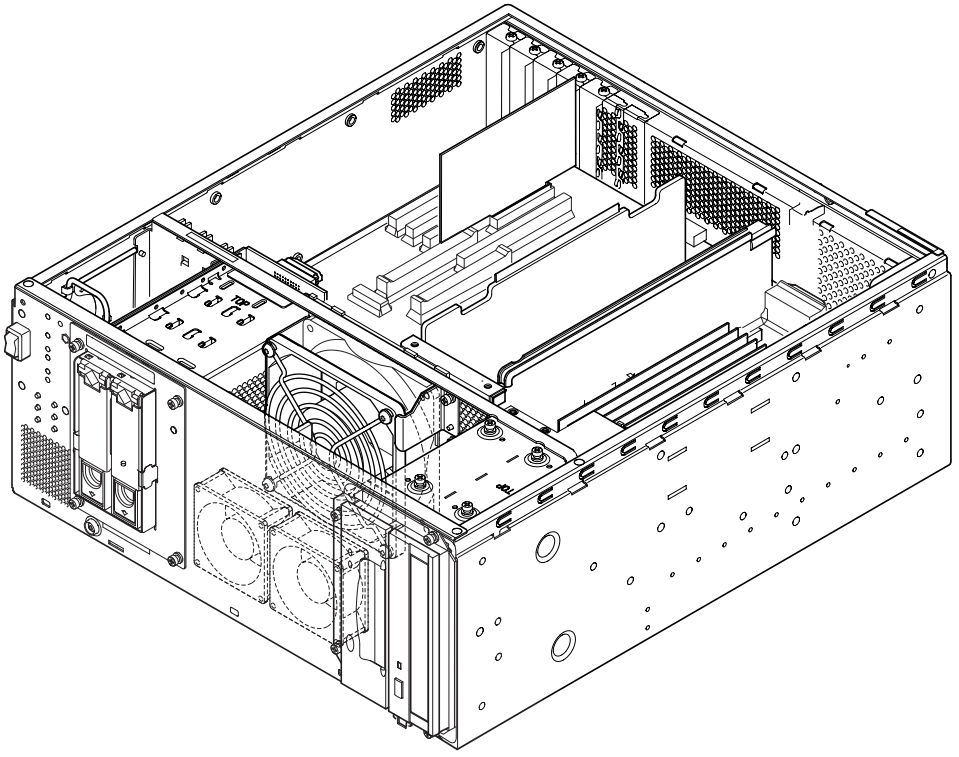


FIGURE 7-1 Netra T4 System Fans

7.1 PSU Fans

The two PSU fans are mounted in a plastic airflow guide at the front of the chassis, between the FC-AL disk drive assembly and the RMM assembly. The two fans and the airflow guide form a single FRU.

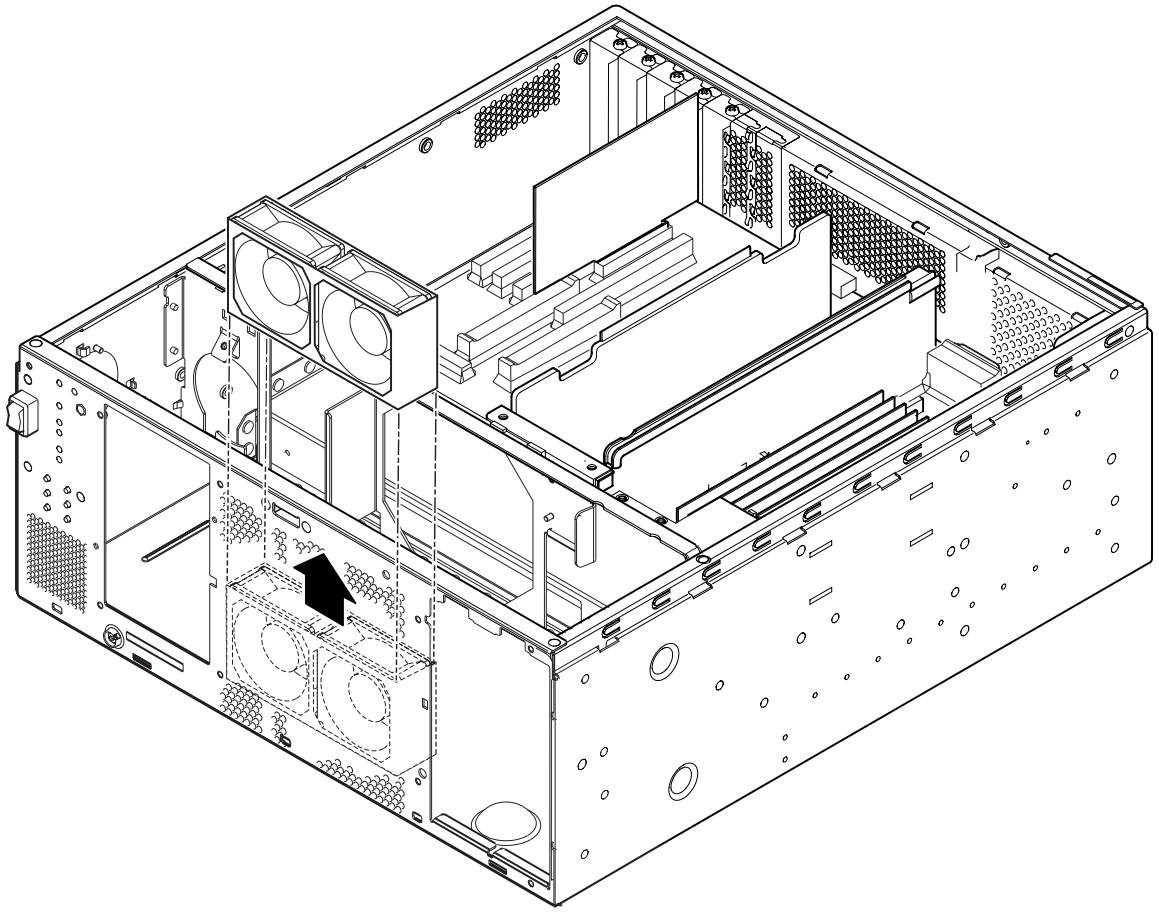


FIGURE 7-2 PSU Fans Assembly

7.1.1 Preparation

Before proceeding to remove the PSU fans assembly, carry out the following:

1. **Initiate antistatic precautions.**
   See Section 5.5, “Antistatic Precautions” on page 5-5.
2. **If the system is running, shut it down and remove the power.**
   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Lower the front fascia.**

   See Section 5.7.1, “Removing the Front Fascia” on page 5-11.

4. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

5. **Remove the FC-AL drive assembly.**

   See Section 8.2.2, “Removing the FC-AL Backplane and Drive Bay” on page 8-8.

6. **Remove the RMM drive assembly.**

   See Section 8.3.2, “Removing a Removable Media Module” on page 8-11.

7.1.2 Removing the PSU Fans Assembly

1. **Perform the steps in Section 7.1.1, “Preparation” on page 7-3 as required.**
2. **Disconnect the fan power cables at J6 and J7 on the PDB.**
3. **Disengage the hooks on the plastic airflow guide from the chassis front panel.**
4. **Lift the plastic airflow guide, together with the two fans, from the chassis enclosure.**

7.1.3 Installing the PSU Fans Assembly

1. **Perform the steps in Section 7.1.1, “Preparation” on page 7-3 as required.**
2. **Insert the fans in the plastic airflow guide.**

   Ensure that the airflow direction arrows are aligned with the arrow on the plastic guide.

3. **Insert the plastic airflow guide and fans into the enclosure and gently press into place until the plastic hooks on the guide locate in the notches in the chassis front panel.**
4. **Reconnect the fan power cables to J6 and J7 on the PDB.**

   Connect the left-hand fan, Fan 1, to J6 and the right-hand fan, Fan 2, to J7.

5. **Refit the RMM drive assembly.**

   See Section 8.3.3, “Installing a Removable Media Module” on page 8-12.

6. **Refit the FC-AL drive assembly.**

   See Section 8.2.3, “Installing the FC-AL Backplane and Drive Bay” on page 8-9.

7. **Refit the top access cover.**

   See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

8. **Refit the front fascia.**

   See Section 5.7.2, “Fitting the Front Fascia” on page 5-11.

7.2 CPU Fan Assembly

The CPU fan is mounted on the transverse support bar, in front of the CPU module housing.

7.2.1 Preparation

Before proceeding to remove the CPU fan assembly, carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and remove the power.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

4. **Lower the front fascia.**

   See Section 5.7.1, “Removing the Front Fascia” on page 5-11.

5. **Remove the RMM drive assembly.**

   See Section 8.3.2, “Removing a Removable Media Module” on page 8-11.

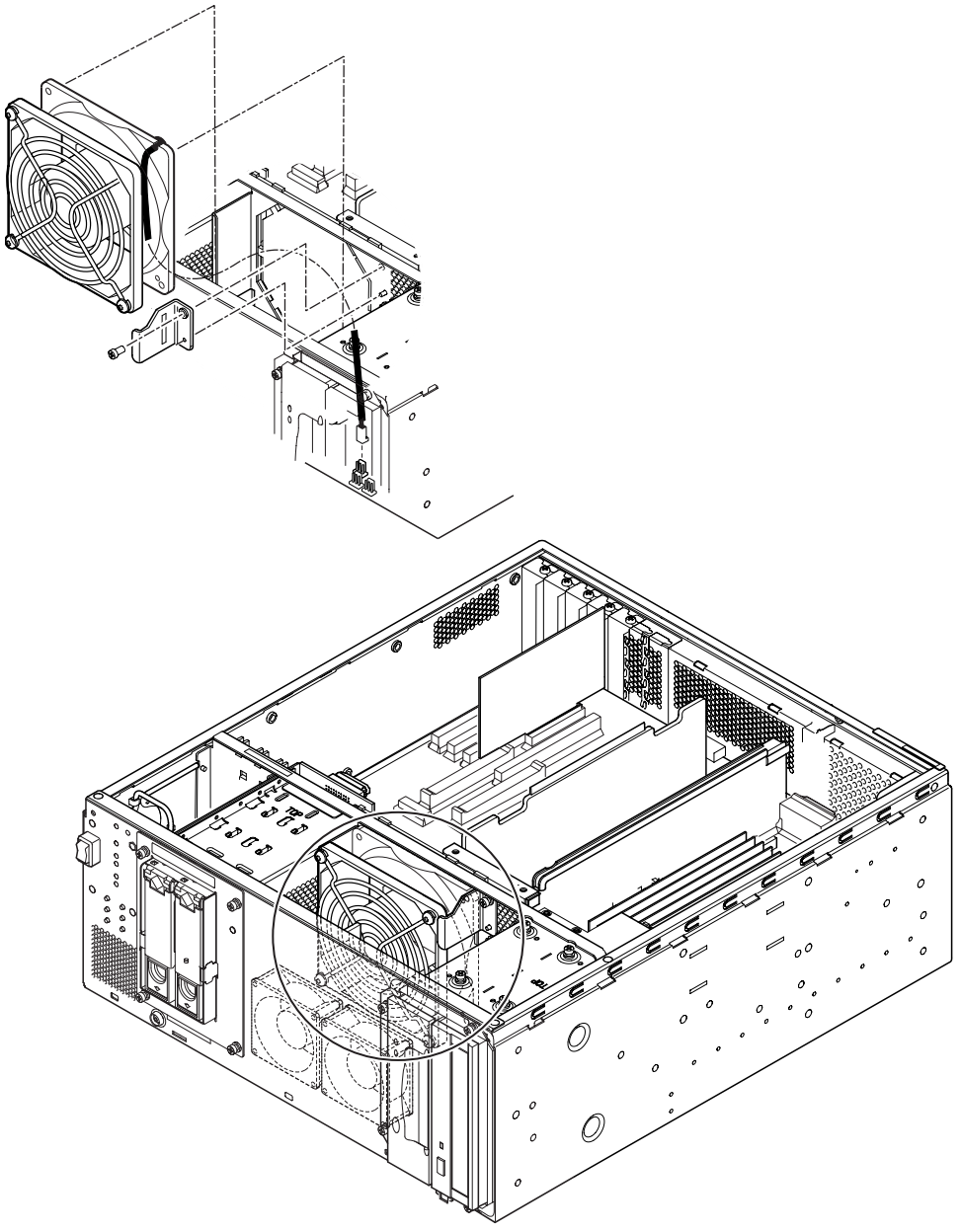


FIGURE 7-3 CPU Fan

7.2.2 Removing the CPU Fan Assembly

1. **Perform the steps in Section 7.2.2, “Removing the CPU Fan Assembly” on page 7-7 as required.**
2. **Disconnect the fan power cable at J9 on the PDB.**
3. **Using a stubby Phillips screwdriver, remove the two captive screws securing the retaining clip on the right hand side of the fan.**
4. **Slide the fan to the right to clear the fan retainer, and ease the assembly from beneath the transverse support bar.**

7.2.3 Installing the CPU Fan Assembly

1. **Perform the steps in Section 7.2.2, “Removing the CPU Fan Assembly” on page 7-7 as required.**
2. **Orientate the fan so that the arrow on the body is pointing towards the rear of the chassis, the fan grill is facing towards the front of the system and the cable exits from the right (see** FIGURE 7-3**).**
3. **Working from the right, slide the fan into position above the PSU fan airflow guide and under the transverse support bar.**

   Ensure that the fan body is properly located in the metal retainer on the left-hand side.
4. **Refit the retaining clip and tighten the two captive Phillips screws.**
5. **Reconnect the fan power cable to J9 on the PDB.**
6. **Refit the RMM drive assembly.**

   See Section 8.3.3, “Installing a Removable Media Module” on page 8-12.
7. **Refit the top access cover.**

   See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.
8. **Refit the front fascia.**

   See Section 5.7.2, “Fitting the Front Fascia” on page 5-11.

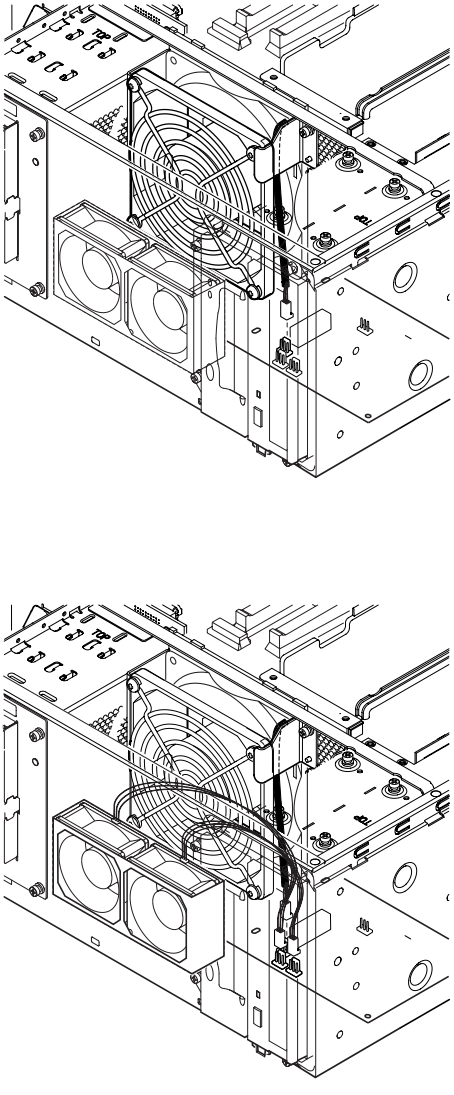


FIGURE 7-4 Fan Connectors

CHAPTER 8

Storage Devices

This chapter contains procedures for removing and fitting the Netra T4 system storage devices.

The chapter contains the following sections:

- Section 8.1, “FC-AL Hard Disk Drive” on page 8-1
- Section 8.2, “Fiber Channel Backplane and Drive Bay” on page 8-6
- Section 8.3, “Removable Media Module” on page 8-10

Caution – The plug at the end of the AC power cord is the primary means of disconnection for the Netra T4 AC100 system.

8.1 FC-AL Hard Disk Drive

The following procedure is concerned with the physical removal and replacement of a hard disk drive as

- A non hot swap device
- A hot swap device

From an operational point of view, whether a disk can be considered to be a hot swap device and can be removed without shutting down Solaris depends on how the disk drives are configured in the operating environment.

The disk is a hot swap device if:

- The disk is not a root disk.

or if both of the following statements are true:

- The disk is a root disk.
- The disk is mirrored or RAID 5-protected.

In other words, if the disk is a root disk and is not mirrored, you must treat it as a non hot swap device.

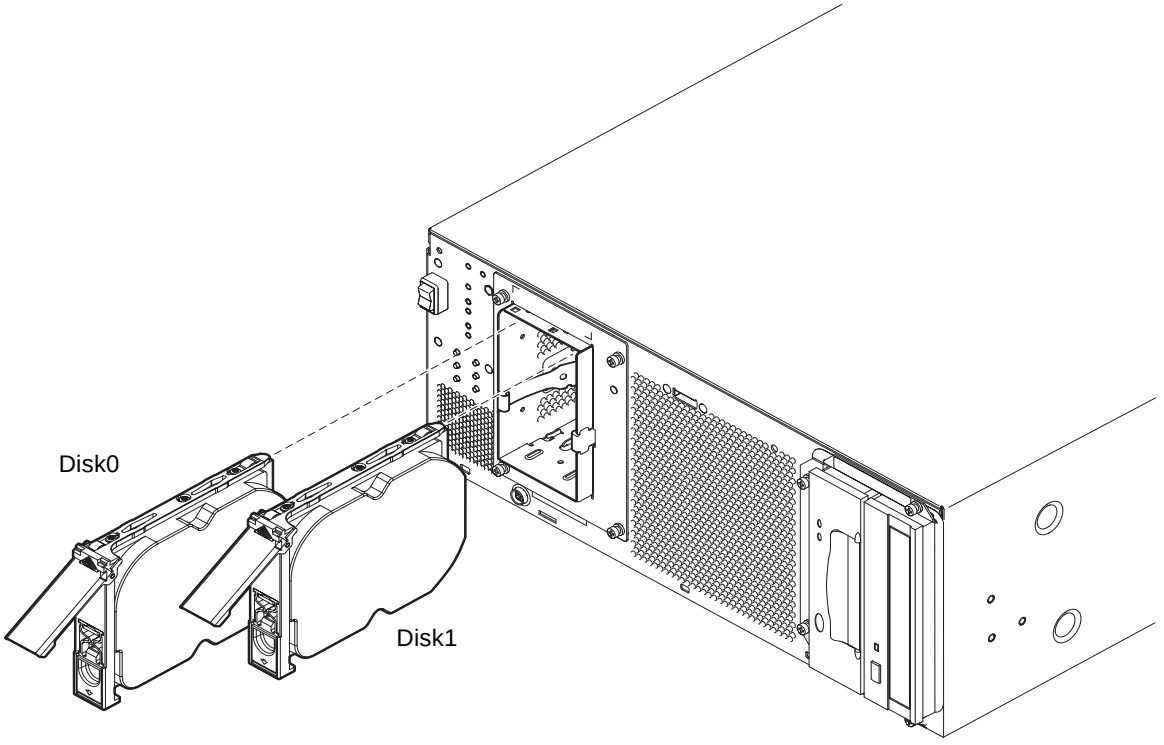


FIGURE 8-1 FC-AL Disk Drive and Drive Bay Assembly

8.1.1 Preparing to Remove a Disk Drive (Hot Swap)

Before proceeding to remove a hard disk drive, carry out the following:

1. **Lower the front fascia.**

   See Section 5.7.1, “Removing the Front Fascia” on page 5-11.

2. **Identify all volumes or applications using the drive.**

   - If the volumes are mirrored or RAID 5-protected, you can replace the drive without taking down the volume.
   - Otherwise stop all I/O activity on the disk drive using the appropriate commands for the particular application.

8.1.2 Removing a Disk Drive (Hot Swap)

1. **Carry out the steps listed in Section 8.1.1, “Preparing to Remove a Disk Drive (Hot Swap)” on page 8-2.**
2. **Isolate the drive from the operating environment.**

Caution – Ensure that no file systems are mounted on the device and back up all data before proceeding.

Logically remove the drive from the FC-AL bus by typing:

```
# luxadm remove_device /dev/rdsk/c1t1d0s2
The list of devices which will be removed is:
1: Device /dev/rdsk/c1t1d0s2

Please enter q to Quit or <Return> to Continue:

Stopping: /dev/rdsk/c1t1dos2....Done
Offlining: /dev/rdsk/ccc11t1dos2....Done

Hit <Return> after removing the device(s)
```

3. **Identify the disk to be remove and the bay in which it is installed.**
4. **Use the World Wide Number (WWN) or Target ID to identify the disk.**

```
# ls -als /dev/rdsk/*

2 lrwxrwxrws 1 root root 74 May 10 11:16 /dev/rdsk/c0t1d0s0 ->
../../devices/pci@8,600000/SUNW,qlc@4/fp@0,0/ssd@w2100002307652252,0:a,raw
[truncated for clarity]
2 lrwxrwxrws 1 root root 74 May 10 11:16 /dev/rdsk/c0t2d0s1 ->
../../devices/pci@8,600000/SUNW,qlc@4/fp@0,0/ssd@w2100002307653317,0:a,raw
[truncated for clarity]
```

- For internal FC-AL disks:

  Target ID Number = Disk Bay Number

- For external FC-AL disks:

  Target ID = (Multipack ID x 8) + Drive Bay Number

5. **Push the disk drive latch downwards to release the drive handle.**

6. **Using the drive handle, ease the drive from the drive bay until you feel the drive connector disengage from the FC-AL backplane connector.**

7. **Holding the disk by the handle, slide the disk drive out of the bay.**

   Support the weight of the drive with your other hand to avoid unnecessary pressure on the drive handle.

8. **Place the disk drive on an antistatic mat.**

8.1.3 Hot Swapping a Disk Drive (Installation)

1. **Logically add the drive to the FC-AL bus by typing:**

```
# luxadm insert_device
The list of devices which will be inserted is:
1: Device /dev/rdsk/c1t2d0s2

Please enter q to Quit or <Return> to Continue:

Stopping: /dev/rdsk/c1t1dos2....Done
Offlining: /dev/rdsk/ccc11t1dos2....Done

Hit <Return> after insertion of the device(s)
```

2. **If necessary, lower the front fascia.**

   See Section 5.7.1, “Removing the Front Fascia” on page 5-11.

3. **Align the disk drive with the slot in the drive bay.**

4. **Slide the disk drive into the drive bay until it makes contact with the FC-AL backplane connector.**

   Do not force it home.

5. **Lock the drive in the bay by pressing on the drive handle until the drive latch closes.**

   This action engages the drive with the FC-AL backplane connector.

6. **Refit the front fascia.**

   See Section 5.7.2, “Fitting the Front Fascia” on page 5-11.

7. **Press <Return> to answer the last line of Step 1.**

8.1.4 Preparing to Remove an Unmirrored Root Disk

Before proceeding to remove a hard disk drive, carry out the following:

1. **Lower the front fascia.**

   See Section 5.7.1, “Removing the Front Fascia” on page 5-11.

2. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

3. **If the system is running, shut it down and remove the power.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

8.1.5 Removing an Unmirrored Root Disk

1. **Perform the steps listed in Section 8.1.4, “Preparing to Remove an Unmirrored Root Disk” on page 8-5.**

2. **Identify the disk to be remove and the bay in which it is installed.**

3. **Use the World Wide Number (WWN) or Target ID to identify the disk.**

```
# ls -als /dev/rdsk/*

2 lrwxrwxrws 1 root root 74 May 10 11:16 /dev/rdsk/c0t1d0s0 ->
../../devices/pci@8,600000/SUNW,qlc@4/fp@0,0/ssd@w2100002307652252,0:a,raw
[truncated for clarity]
2 lrwxrwxrws 1 root root 74 May 10 11:16 /dev/rdsk/c0t2d0s1 ->
../../devices/pci@8,600000/SUNW,qlc@4/fp@0,0/ssd@w2100002307653317,0:a,raw
[truncated for clarity]
```

   - For internal FC-AL disks:

     Target ID Number = Disk Bay Number

   - For external FC-AL disks:

     Target ID = (Multipack ID x 8) + Drive Bay Number

4. **Push the disk drive latch downwards to release the drive handle.**

5. **Using the drive handle, ease the drive from the drive bay until you feel the drive connector disengage from the FC-AL backplane connector.**

6. **Holding the disk by the handle, slide the disk drive out of the bay.**

   Support the weight of the drive with your other hand to avoid unnecessary pressure on the drive handle.

7. **Place the disk drive on an antistatic mat.**

8.1.6 Installing an Unmirrored Root Disk

1. **Perform the steps listed in Section 8.1.4, “Preparing to Remove an Unmirrored Root Disk” on page 8-5, as required.**
2. **Align the disk drive with the slot in the drive bay.**
3. **Slide the disk drive into the drive bay until it makes contact with the FC-AL backplane connector.**

   Do not force it home.

4. **Lock the drive in the bay by pressing on the drive handle until the drive latch closes.**

   This action engages the drive with the FC-AL backplane connector.

5. **Refit the front fascia.**

   See Section 5.7.2, “Fitting the Front Fascia” on page 5-11.

6. **Perform a reconfiguration boot by typing:**

```
ok boot -r
```

8.2 Fiber Channel Backplane and Drive Bay

The FC-AL backplane and drive bay assembly is located at the front of the chassis, to the left of the CPU fan, and houses the two internal disk drives. There are one connector, one power connector and one I2C connector to the backplane, which is mounted on the rear of the drive bay (see FIGURE 8-2).

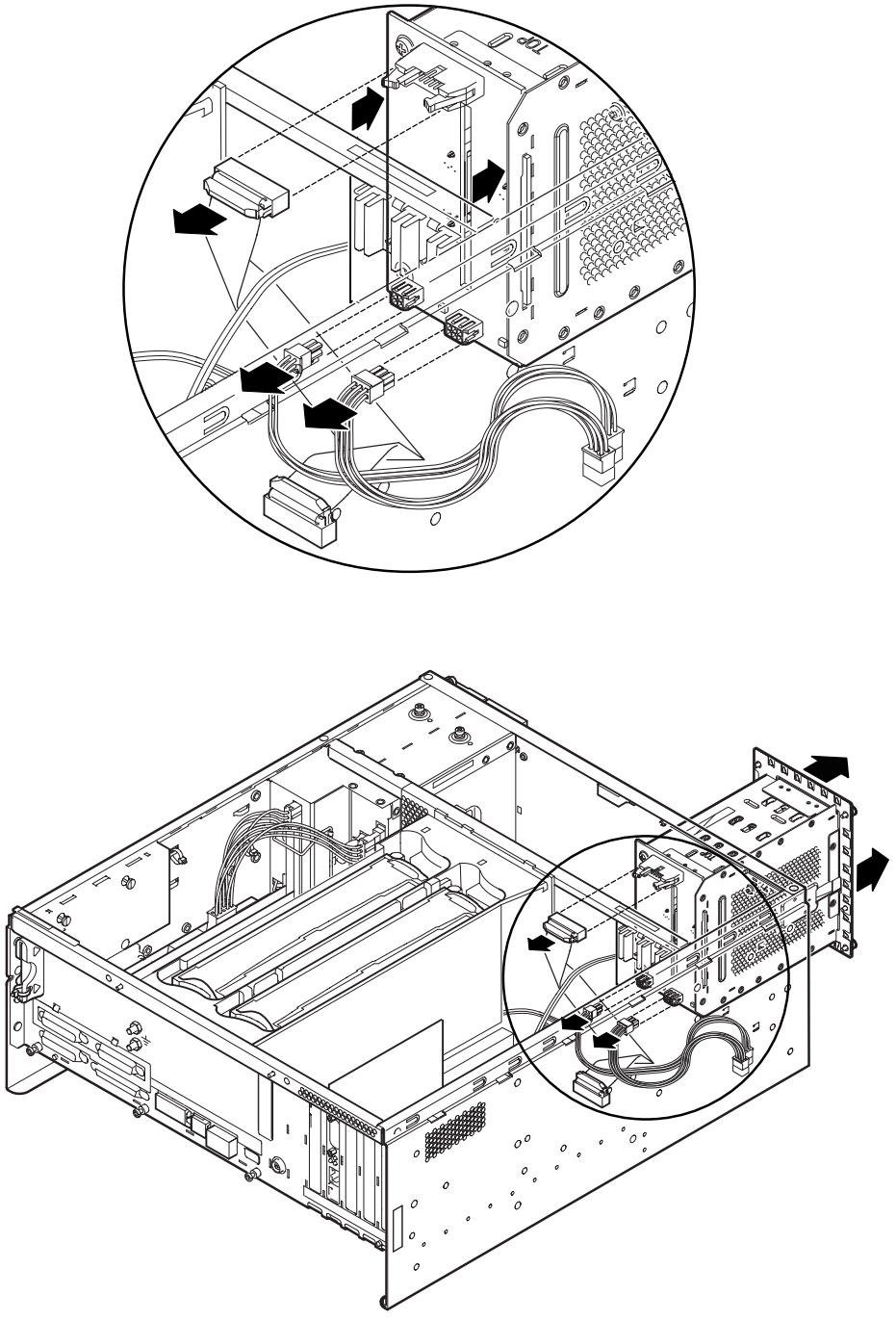


FIGURE 8-2 FC-AL Backplane and Drive Bay Assembly

8.2.1 Preparation

Before proceeding to remove the FC-AL backplane and drive bay assembly, carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and remove the power.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Lower the front fascia.**

   See Section 5.7.1, “Removing the Front Fascia” on page 5-11.

4. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

8.2.2 Removing the FC-AL Backplane and Drive Bay

1. **Perform the appropriate steps listed in Section 8.2.1, “Preparation” on page 8-8.**
2. **Loosen the four captive Phillips screws securing the drive bay to the chassis front panel.**
3. **Disconnect the 20-way ribbon data cable at J0102 on the FC-AL backplane by opening the side locking lugs on the socket and withdrawing the connector.**

   This cable is connected to J2901 on the motherboard.

4. **Ease the drive bay assembly forward to access the two lower connectors to the backplane.**
5. **Disconnect the power cable to J0101 on the FC-AL backplane.**

   The cable is connected to J12 on the PDB.

6. **Disconnect the I2C cable to J0103 on the FC-AL backplane.**

   This cable is connected to J13 on the PDB

7. **Carefully withdraw the assembly from the chassis and place it on the antistatic mat.**

8.2.2.1 Removing the Backplane

8. **With assembly on the antistatic mat, release the two Phillips screws securing the backplane to the drive bay.**
9. **Remove the backplane and place it flat on the antistatic mat.**

8.2.3 Installing the FC-AL Backplane and Drive Bay

1. **Perform the steps listed in Section 8.2.1, “Preparation” on page 8-8, as required.**
2. **If the backplane was removed from the drive bay in Step 8 above, place the backplane and drive bay on the antistatic mat, align the fixing holes on the backplane with those on the rear of the drive bay and refit the two screws.**
3. **Align the assembly with the cutout in the front of the chassis located to the left of the CPU fan.**
4. **Slide the assembly partially into the chassis.**
5. **Reconnect the I2C cable from J13 on the PDB to J0103 on the FC-AL backplane.**
6. **Reconnect the power cable from J12 on the PDB to J0101 on the FC-AL backplane.**
7. **Reconnect the ribbon data cable from J2901 on the motherboard to J0102 on the FC-AL backplane and press it home until the side locking lugs on the socket click into place.**
8. **Slide the assembly completely into the chassis until it is flush with the chassis.**
9. **Tighten the four captive Phillips screws to secure the assembly to the chassis.**
10. **Refit the disk drive(s) if you have removed them previously.**

    Note that the boot disk must be located in drive 0.
11. **Refit the top access cover.**

    See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.
12. **Refit the front fascia.**

    See Section 5.7.2, “Fitting the Front Fascia” on page 5-11.

8.3 Removable Media Module

The optional DVD-R and DDS-4 DAT drive Removable Media Modules (RMM) are housed in their own sub chassis which is located to the right of the CPU fan at the front of the system.

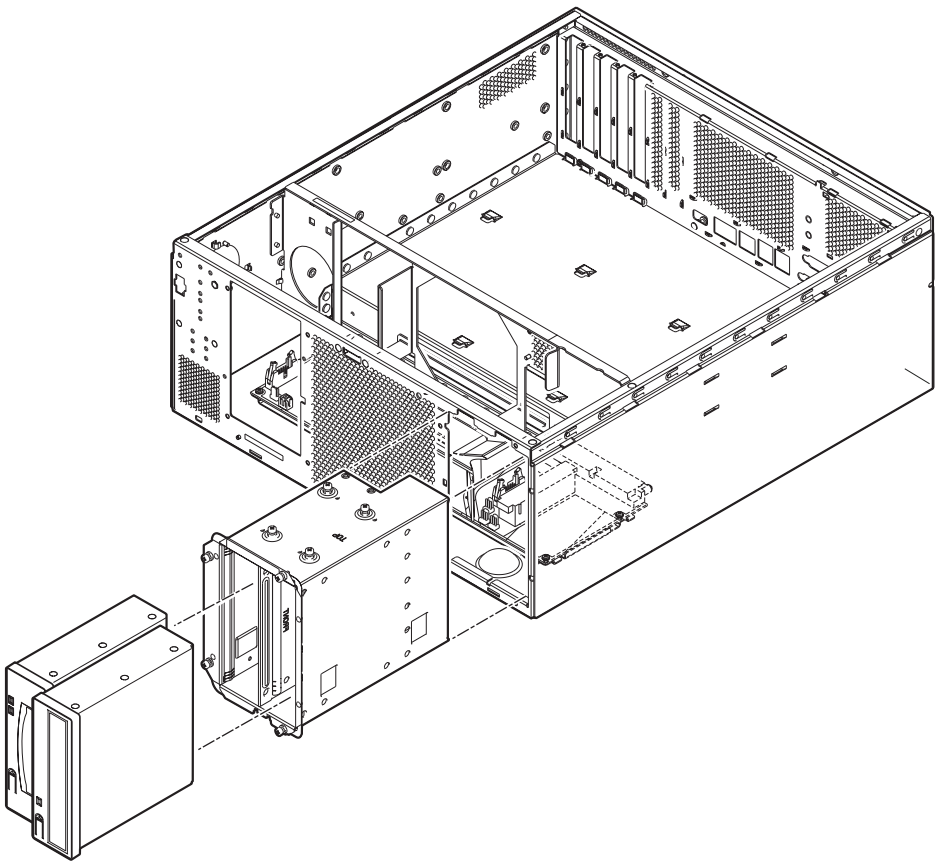


FIGURE 8-3 Removable Media Modules

8.3.1 Preparation

The assembly can be removed with the DVD-R and DAT drives in place. Before proceeding to remove the RMM assembly, carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and remove the power.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Lower the front fascia.**

   See Section 5.7.1, “Removing the Front Fascia” on page 5-11.

4. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

8.3.2 Removing a Removable Media Module

1. **Perform the steps listed in Section 8.3.1, “Preparation” on page 8-10, as appropriate.**
2. **Loosen the four captive Phillips screws securing the RMM drive bay assembly to the front of the chassis and *partially* withdraw the drive bay from the chassis.**
3. **Disconnect the SCSI data cable at the motherboard.**
4. **Disconnect the power cable at the motherboard.**
5. **Carefully withdraw the RMM drive bay assembly from the chassis and place it on the antistatic mat.**
6. **Remove the DVD-R drive as follows:**
   a. **Release the two screws securing the DVD-R drive to the drive bay.**
   b. **Detach the power connector at the rear of the drive bay.**
   c. **Slide the DVD-R drive out of the drive bay and place it on the antistatic mat.**
7. **Remove the DAT drive as follows:**
   a. **Detach the power connector at the rear of the drive bay.**
   b. **Release the clips holding the SCSI connector and detach if from the rear of the drive**
   c. **Release the two screws securing the DAT drive to the drive bay.**
   d. **Slide the DAT drive out of the drive bay and place it on the antistatic mat.**
8. **If you are replacing the drive with a new one, note the position of the jumpers on the drive(s) so that you can set up the new drive identically.**

8.3.3 Installing a Removable Media Module

1. **Perform the steps listed in Section 8.3.1, “Preparation” on page 8-10, as appropriate.**
2. **If you are replacing an existing drive, ensure the jumper settings match those on the drive you are replacing. Otherwise, refer to the documentation enclosed with your drive for information about the settings.**
3. **To refit the DVD-R drive**:
   a. **Slide the drive partially into the right-hand slot in the RMM drive bay. assembly.**
   b. **Align the SCSI connector with the port on the DVD-R drive and press the drive into the drive bay until the connector is firmly attached.**
   c. **Reconnect the power cable at the rear of the drive.**
   d. **Tighten the two captive Phillips screws to secure the drive in its bay.**
4. **To refit the DAT drive**:
   a. **Slide the drive into the left-hand slot in the RMM drive bay.**
   b. **Tighten the two captive Phillips screws to secure the drive in its bay.**
   c. **Attach the SCSI connector at the rear of the drive and lock the retaining clips over the connector.**
   d. **Reconnect the power cable at the rear of the drive.**
5. **Slide the drive bay assembly** *partially* **into the chassis.**
6. **Reconnect the SCSI data cable to the drives at the motherboard.**
7. **Reconnect the power cable to the drives at the motherboard.**
8. **Slide the drive bay assembly fully into the chassis until it is flush with the front panel.**
9. **Refit the four Phillips screws to secure the drive bay assembly to the chassis.**
10. **If necessary, fit a plastic cover to any unoccupied drive bay.**
11. **Refit the top access cover.**
    See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.
12. **Refit the front fascia.**
    See Section 5.7.2, “Fitting the Front Fascia” on page 5-11.

CHAPTER 9

Motherboard and Component Replacement

This chapter describes how to remove and fit the Netra T4 motherboard and the components that interface directly with the motherboard.

The chapter contains the following sections:

- Section 9.1, “PCI Cards” on page 9-2
- Section 9.2, “Processor Modules” on page 9-4
- Section 9.3, “Memory Modules” on page 9-9
- Section 9.4, “Replaceable Battery” on page 9-12
- Section 9.5, “LOMLite2 Card” on page 9-14
- Section 9.6, “System Configuration Card Reader” on page 9-16
- Section 9.7, “Motherboard” on page 9-18

Note – The only hot-swap components in the Netra T4 system are the hard disks. All other components, including those described in this chapter, require the system to be powered down and electrically isolated before they can be removed or fitted.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – The plug at the end of the AC power cord is the primary means of disconnection for the Netra T4 AC100 system.

Caution – To isolate the Netra T4 DC100 system, open the circuit breakers on both negative supply conductors.

9.1 PCI Cards

This section describes how to remove and fit a PCI card.

The PCI cards connector are located on the left hand side of the motherboard at the rear of the chassis. PCI slots 1 through 3 (numbering from the left, viewed from the front) accept long (64-bit) or short (32-bit) cards. PCI slot 4 can accept only short PCI cards owing to the placement of the FC-AL backplane.

All slots support 33MHz cards; slot 1 also supports 66MHz cards.

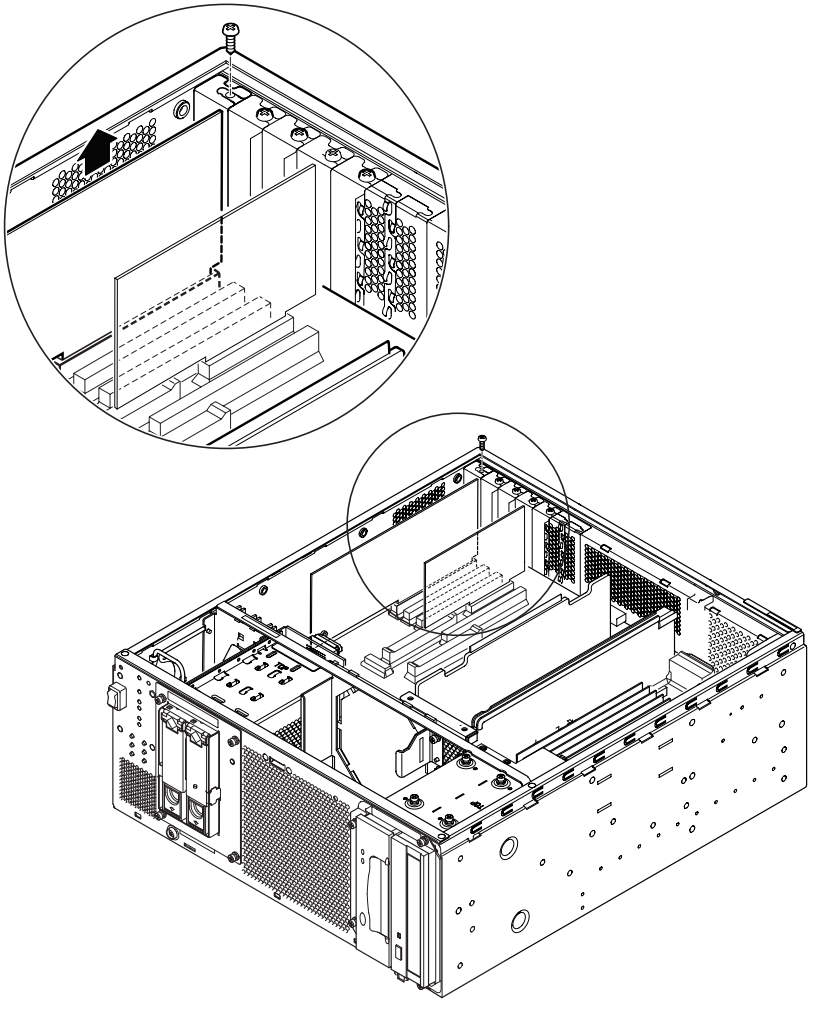


FIGURE 9-1 PCI Card Slots

9.1.1 Preparation

Before proceeding to remove or fit a PCI card, carry out the following:

1. **Initiate antistatic precautions.**
   See Section 5.5, “Antistatic Precautions” on page 5-5.
2. **If the system is running, shut it down and remove the power.**
   See Section 5.3.2, “Powering Off the System” on page 5-4.
3. **Remove the top access cover.**
   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

9.1.2 Removing a PCI Card

1. **Perform the steps listed in Section 9.1.1, “Preparation” on page 9-3.**
2. **Disconnect all external cables connected to the PCI card.**
3. **Disconnect any internal cables connected to the PCI card.**
4. **Remove the fixing screw securing the card to the rear of the chassis.**
5. **Ease the card from its slot.**
6. **Place the card on the antistatic mat.**
7. **If you are not replacing the card, fit a blanking plate to the rear panel of the chassis and secure it with the fixing screw.**
8. **Refit the top access cover.**
   See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

9.1.3 Installing a PCI Card

1. **Perform the steps listed in Section 9.1.1, “Preparation” on page 9-3.**
2. **Locate a vacant PCI slot.**
   If your PCI card is a 66Mhz card, you must use slot 1.
3. **If the slot is protected by a blanking plate, remove the fixing screw and the plate.**
4. **Gently push the card into the connector, applying even pressure at both ends of the card.**

5. **Secure the plate to the rear panel of the chassis using the fixing screw.**
6. **Connect any internal cables to the PCI card, as required.**
7. **Connect any external cables to the PCI card, as required.**
8. **Refit the top access cover.**

See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

9.2 Processor Modules

This section describes how to remove and fit a CPU module.

The processors and associated circuitry are housed in self-contained modules, which are inserted into plastic air guides attached to the motherboard. There are slots for two processor modules on the Netra T4 motherboard. Viewed from the front of the unit, CPU0 is located immediately to the left of the memory modules. The plastic shroud cover and shroud are also stamped 0 and 1 to further aid identification.

Note – Slot 0 must always contain a CPU module.

Caution – To ensure proper cooling, an unused CPU slot must be fitted with a shroud filler panel in place of a CPU module.

Caution – When you unpack a new CPU module from its packing carton, it is important that you observe the following handling precautions to avoid damaging the module. 1.) When you lift the module from the packing carton in its antistatic bag, use both hands to support the module along its short sides. 2.) After you remove the module from its antistatic bag, handle it only by its captive screws. Do not touch the connectors on the bottom edge of the module, which can be easily bent or damaged by improper handling. 3.) Do not remove the plastic cover from the connectors until you are ready to install the module. 4.) Do not grip the module by the heat sinks, which can shift if handled improperly. 5.) Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

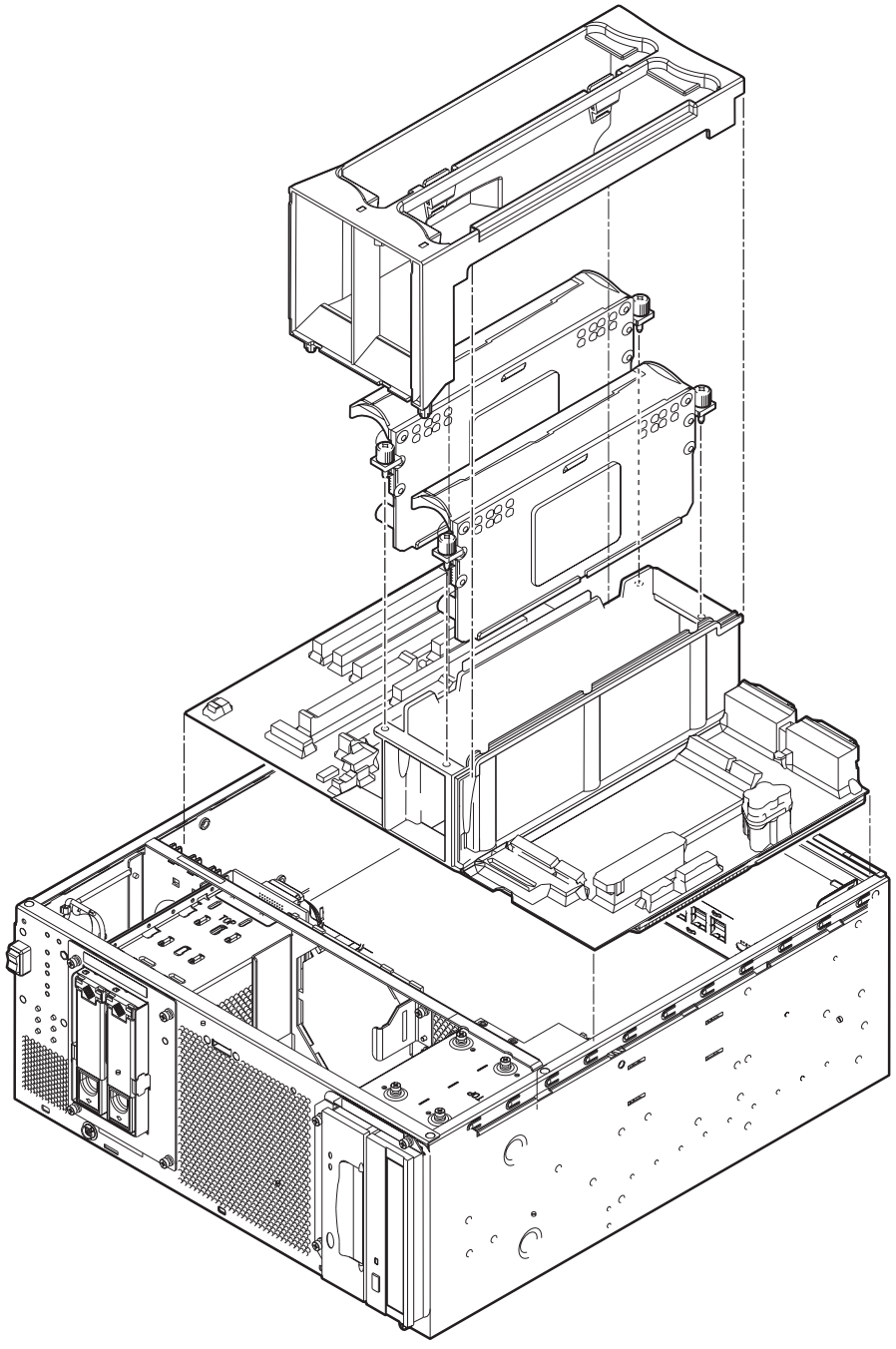


FIGURE 9-2 CPU Modules

9.2.1 Preparation

Before proceeding to remove a CPU module, carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and remove the power.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

9.2.2 Removing a CPU Module

1. **Perform the steps listed in Section 9.2.1, “Preparation” on page 9-6.**
2. **Remove the purple plastic CPU shroud cover by holding the tabs to release them and lifting the shroud from the chassis.**
3. **Identify the CPU module to be removed.**
4. **Remove the torque tool from its location inside the chassis.**

   See FIGURE 9-2.

5. **Use the tool to loosen each knurled torque screw counter-clockwise through 360˚.**
6. **Turn both screws by hand at the same time until the CPU module is released from the slot.**
7. **Without touching the heat sink and the connectors on the base of the CPU module, lift the module out of the CPU shroud and place it on the antistatic mat.**

   You can use the plastic faceplate as a handle.

8. **If you are not immediately fitting a new CPU module, continue below, otherwise continue with Section 9.2.3, “Installing a CPU Module” on page 9-7:**

   a. **Refit the CPU shroud cover by sliding it back into place until the locking tags engage.**

      Note that slot CPU0 must always contain a CPU module.

   b. **Fit a blanking panel in the open slot.**

9. **Return the torque tool to its storage place in the system chassis.**
10. **Refit the top access cover.**

    See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

9.2.3 Installing a CPU Module

1. **Perform the steps listed in Section 9.2.1, “Preparation” on page 9-6 as required.**
2. **If you have not already done so, remove the purple plastic CPU shroud cover by holding the tabs to release them and lifting the cover from the chassis.**
3. **Identify the slot to be used.**
4. **Without touching the heat sink and the connectors on the base of the CPU module, insert the CPU module in the CPU shroud until it touches the socket on the motherboard and the module’s captive screws are aligned with the screw holes in the CPU shroud.**
5. **Turn both screws by hand, clockwise, at the same time until they are finger tight.**
6. **Use the torque tool to tighten each screw until the gap in the tool closes.**

   See FIGURE 9-3.The torque is now set at 5lbf-in.

Note – If you are using an adjustable torque tool, tighten the CPU module screws to 5lbf-in.

Caution – Do not overtighten or subsequently retighten the screws.

---

7. **Refit the shroud cover by sliding it back into place until the locking tags engage.**
8. **Return the torque tool to its storage place in the system chassis.**
9. **Refit the top access cover.**

   See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

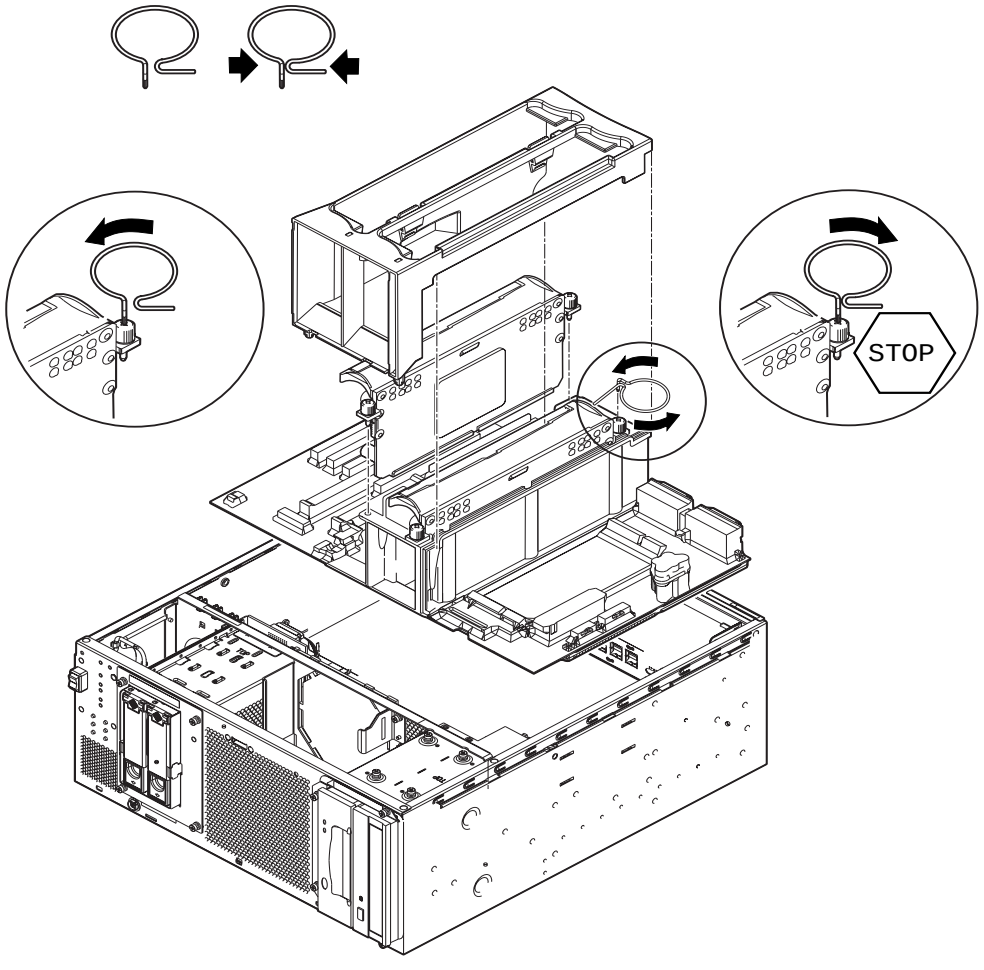


FIGURE 9-3 Using the Torque Tool

9.3 Memory Modules

This section describes how to remove and fit the dual inline memory modules (DIMMs).

The DIMMs are located in two banks, to the right of the CPU modules (see FIGURE 9-4). The banks comprise alternate slots, designated 0 (even slots) and 1 (odd slots), and all four slots in either or both of the banks must be filled.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – When you remove and replace a single DIMM, an identical replacement is required. The replacement DIMM must be inserted into the same socket as the removed DIMM.

Caution – Each DIMM bank must contain at least four DIMMs of equal density (for example, four 256Mbyte DIMMs) to function properly. Do not mix DIMM densities within any bank.

Caution – Handle DIMMs only by the edges. Do not touch the DIMM components or metal parts. Always wear a grounding strap when handling a DIMM.

The DIMMs, keyed for alignment, are available in 128 MByte, 256 MByte, 512 MByte and 1 GByte densities, and each bank must contain four DIMMs of the same density. However, the DIMMs in bank 0 need not be the same as those in bank 1.

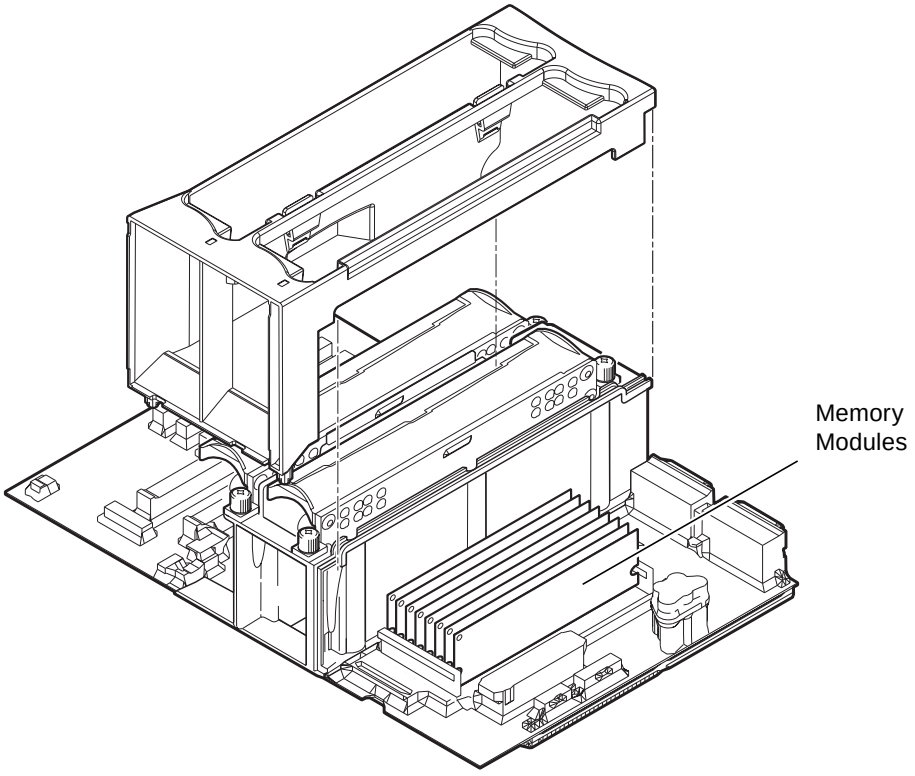


FIGURE 9-4 Memory Modules

9.3.1 Preparation

Before proceeding to remove a memory module, carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and remove the power.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

4. **If necessary, disconnect the power cable at J3601 on the motherboard to ease access.**

9.3.2 Removing a Memory Module

1. **Perform the steps listed in Section 9.3.1, “Preparation” on page 9-10.**
2. **Locate the DIMM(s) to be removed.**
3. **Press down on the lever at each end of the DIMM socket to eject the DIMM from its socket.**
4. **Hold the DIMM by the top corners and put it upwards out of its socket.**
5. **Place the DIMM on an antistatic mat.**
6. **If you are storing the DIMM, place it in an antistatic package, preferably its original container.**
7. **Continue to remove DIMMs as required or fit replacements.**

   See Section 9.3.3, “Installing a Memory Module” on page 9-11.
8. **If necessary, reconnect the power cable at J3601 on the motherboard.**
9. **Refit the top access cover.**

   See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

9.3.3 Installing a Memory Module

1. **Perform the steps listed in Section 9.3.1, “Preparation” on page 9-10.**
2. **Remove the DIMM from its protective antistatic package.**
3. **Locate the socket in which the DIMM is to be fitted.**
4. **Align the DIMM with the socket, noting the orientation of the keyways in the DIMM and the tags in the socket.**
5. **Press down firmly on both corners of the DIMM with your thumbs until the connectors are fully seated in the socket and the levers click into place.**
6. **Continue to fit DIMMs until one or both banks are full (**FIGURE 9-5**).**

Note – All the DIMMs in a single bank must be of the same density.

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7. **Refit the top access cover.**

See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

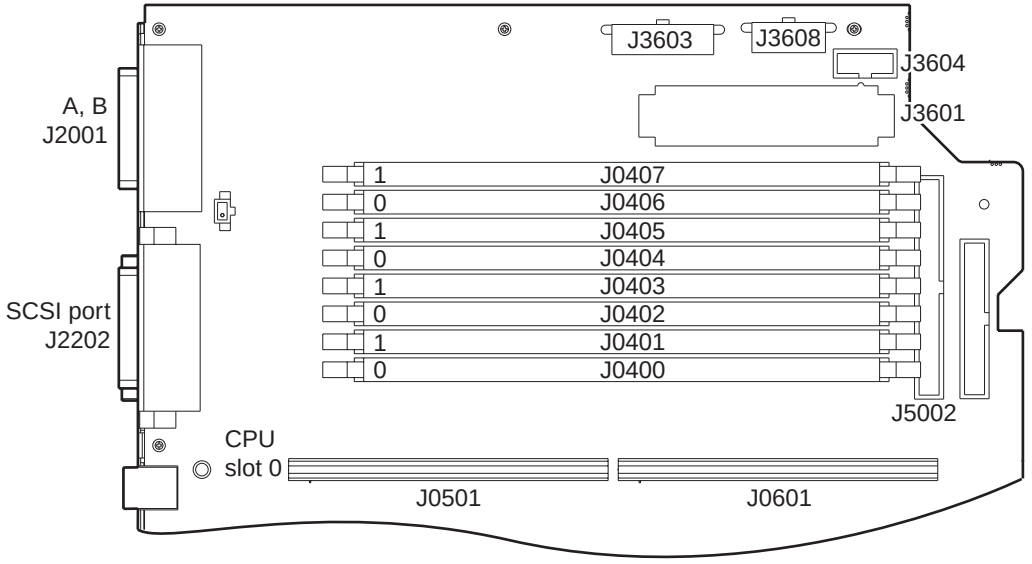


FIGURE 9-5 Memory Banks

9.4 Replaceable Battery

The system contains a replaceable lithium battery, part number 150-2850.

Caution – Danger of explosion if battery is incorrectly replaced. Replace with only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer’s instructions.

9.4.1 Preparation

Before proceeding to remove the lithium battery, carry out the following:

1. **Initiate antistatic precautions.**

See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and remove the power.**
   See Section 5.3.2, “Powering Off the System” on page 5-4.
3. **Remove the top access cover.**
   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

9.4.2 Removing the Battery

1. **Perform the steps listed in Section 9.4.1, “Preparation” on page 9-12 as required.**
2. **Locate the battery on the motherboard.**
   See FIGURE 9-9
3. **Carefully lift the battery retaining clip with a small screwdriver.**
4. **Carefully slide the battery out of its socket and remove it from the system.**

FIGURE 9-6 Battery Location

9.4.3 Installing the Battery

Note – Install the new battery with the plus (+) side up.

---

1. **Hold the battery retaining clip up and slide the battery into its socket.**
2. **Install the CPU shroud cover.**
3. **Refit the top access cover.**
   See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.
4. **Reset the time of day and date.**

9.5 LOMLite2 Card

The LOMlite2 card is located in the RSC connector, the shorter of the two slots between PCI slots 3 and 4.

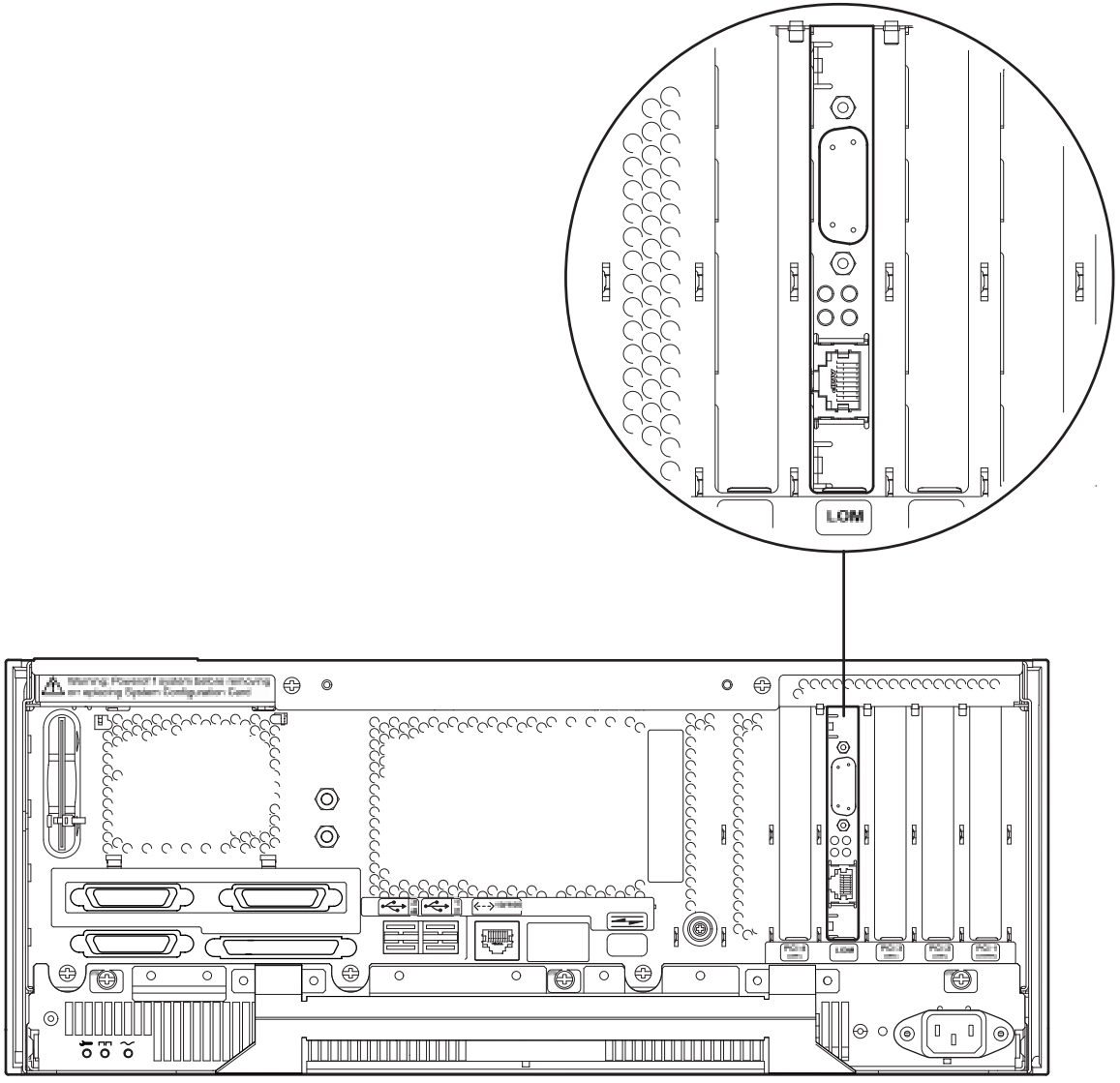


FIGURE 9-7 LOMlite2 Card

9.5.1 Preparation

Before proceeding to remove the LOMlite2 Card, carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Remove the AC power cord from the appliance inlet and allow 10s for the standby power to dissipate before proceeding.**

4. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

9.5.2 Removing the LOMlite2 Card

1. **Perform the steps listed in Section 9.5.1, “Preparation” on page 9-15.**
2. **Locate the LOMlite2 card (see** FIGURE 9-7**).**
3. **Disconnect all external cables to the LOMlite card.**
4. **Disconnect the I2C cable at J0302 on the LOMlite2 card.**
5. **Remove the screw securing the LOMlite2 I/O connector plate to the chassis.**
6. **Pull out the LOMlite2 card and place it on an antistatic mat.**

Note – The LOMlite2 card must always be fitted.

9.5.3 Installing the LOMlite2 Card

1. **Perform the steps listed in Section 9.5.1, “Preparation” on page 9-15.**
2. **Locate the LOMlite2 slot on the motherboard (see** FIGURE 9-7**).**
3. **If necessary, remove the blanking panel from corresponding aperture on the rear panel of the chassis.**
4. **Insert the LOMlite2 card fully into its slot.**
5. **Secure the LOMlite2 card to the chassis by tightening the plate fixing screw.**

6. **Reconnect the I2C ribbon cable to J0302 on the LOMlite2 card.**
7. **Reconnect the external cabling to the I/O connectors as required.**
8. **Refit the top access cover.**

See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

9.6 System Configuration Card Reader

The System Configuration Card Reader (SCCR) is located at the rear of the chassis, on the right-hand side panel.

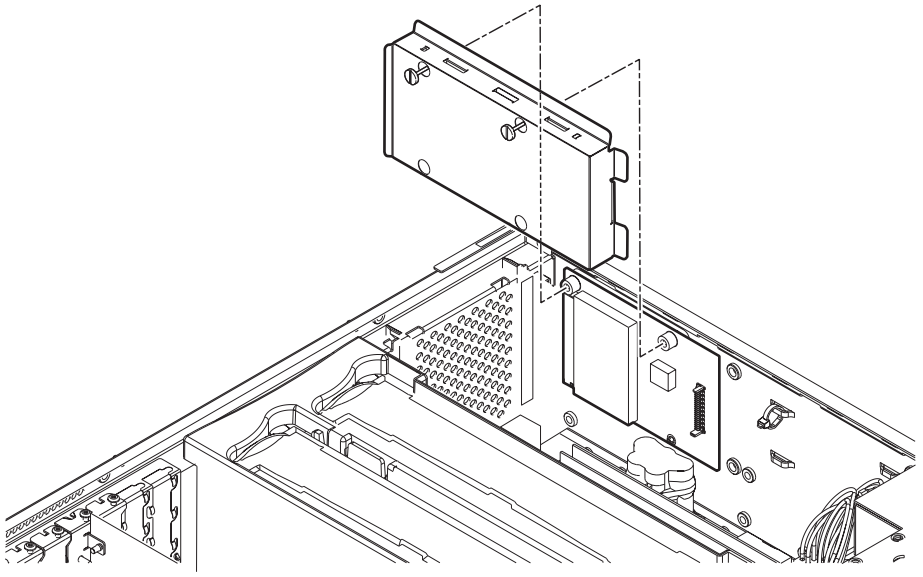


FIGURE 9-8 System Configuration Card Reader

9.6.1 Preparation

Before proceeding to remove a System Configuration Card Reader (SCCR), carry out the following:

1. **Initiate antistatic precautions.**

See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and remove the power.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

4. **Remove the card from the smart card from the SCCR and** ***store it safely*****.**

9.6.2 Removing the SCCR

1. **Perform the steps listed in Section 9.6.1, “Preparation” on page 9-16.**
2. **Remove the two slot head screws securing the SCCR cover and remove it.**
3. **Cut the cable tie securing the ribbon cable to the chassis side panel.**
4. **Disconnect the ribbon cable at J3604 on the motherboard and J4 on the PDB**
5. **Release the two upper captive fixing screws securing the SCCR to the chassis side panel.**
6. **Carefully prise the card off the two lower spring-loaded pins.**
7. **Remove the SCCR and place it on the antistatic mat.**

9.6.3 Installing the SCCR

1. **Perform the steps listed in Section 9.6.1, “Preparation” on page 9-16.**
2. **Locate the SCCR over the two lower spring-loaded fixing pins and press the board gently and evenly onto the pins.**
3. **Tighten by hand the two captive upper fixing screws.**

   Reconnect the ribbon cable to J3604 on the motherboard.

4. **Feed the cable between the large and small power cables to the PDB and reconnect the cable to J4 on the PDB.**

   Replace the cable tie removed in Step 3 in the previous section.

5. **Replace the SCCR cover and tighten the two screws removed in Step 2 of the previous section.**
6. **Refit the CPU fan assembly.**

   See Section 7.2.3, “Installing the CPU Fan Assembly” on page 7-7.

7. **Refit the smart card in the SCCR.**
8. **Refit the top access cover.**

   See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

9.7 Motherboard

The motherboard component and connector layout is shown in FIGURE 9-9.

Caution – Use an antistatic mat when working with the motherboard. An antistatic mat contains the cushioning needed to protect the underside components, to prevent motherboard flexing, and to provide antistatic protection.

Note – If you intend to exchange the motherboard and preserve the Ethernet address, HostID and other configuration settings, you must retain the system configuration card.

9.7.1 Preparation

Before proceeding to remove the motherboard, carry out the following:

1. **Initiate antistatic precautions.**

   See Section 5.5, “Antistatic Precautions” on page 5-5.

2. **If the system is running, shut it down and remove the power.**

   See Section 5.3.2, “Powering Off the System” on page 5-4.

3. **Remove the top access cover.**

   See Section 5.6.2, “Removing the Top Access Cover” on page 5-9.

4. **Remove all memory modules.**

   See Section 9.3.2, “Removing a Memory Module” on page 9-11.

5. **Remove the LOMLite 2 (alarms) card.**

   See Section 9.5.2, “Removing the LOMlite2 Card” on page 9-15.

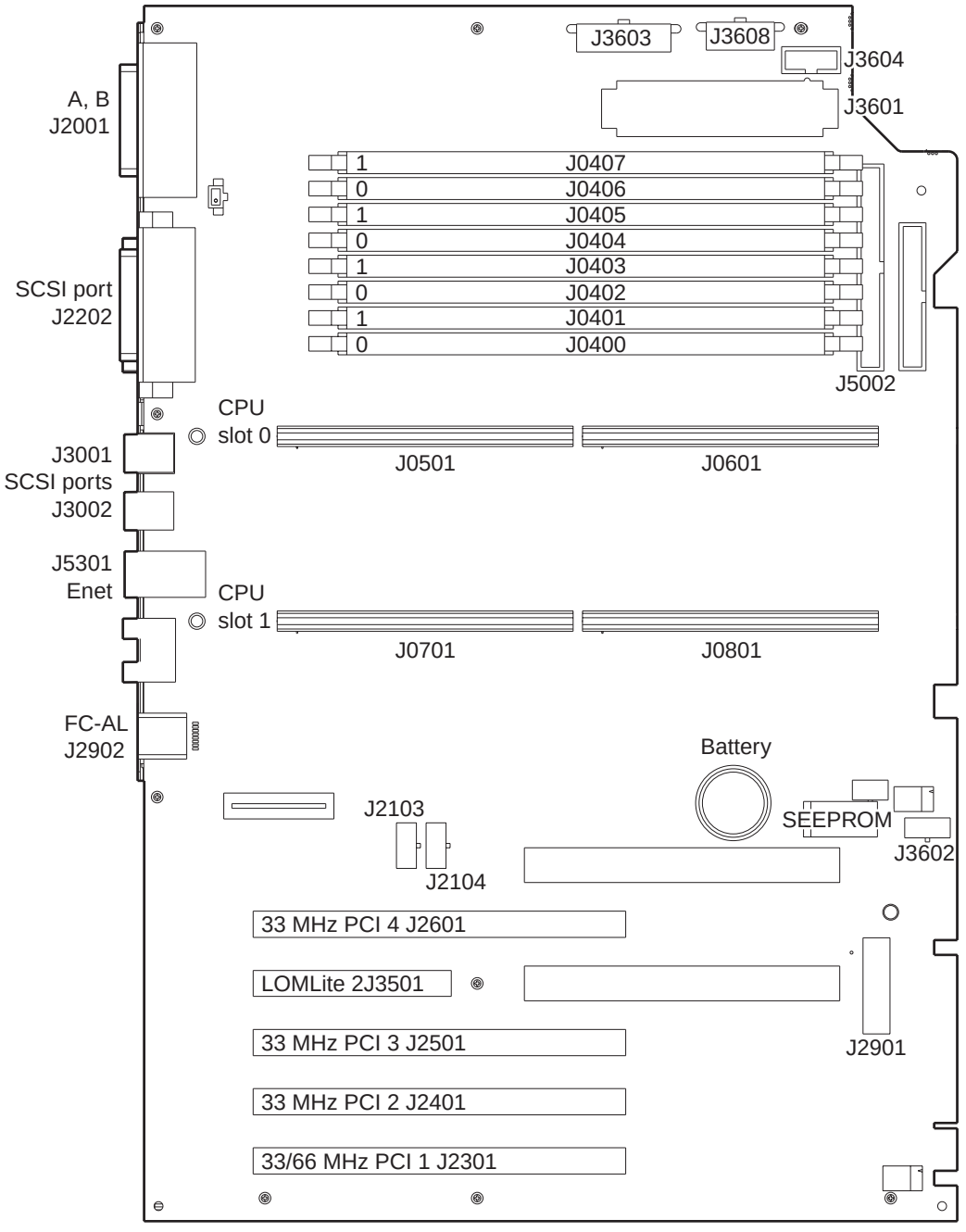


FIGURE 9-9 Motherboard Layout

6. **Remove all PCI cards.**

   See Section 9.1.2, “Removing a PCI Card” on page 9-3.

7. **Remove all CPU modules.**

   See Section 9.2.2, “Removing a CPU Module” on page 9-6

8. **Ease the RMM drive assembly forward in the chassis access the PDB connectors.**

   See Section 8.3.2, “Removing a Removable Media Module” on page 8-11.

9. **Remove the FC-AL drive assembly forward in the chassis to access the PDB connectors.**

   See Section 8.2.2, “Removing the FC-AL Backplane and Drive Bay” on page 8-8.

10. **Remove the SCCR.**

    See Section 9.6.2, “Removing the SCCR” on page 9-17.

9.7.2 Removing the Motherboard

1. **Perform the steps listed in Section 9.7.1, “Preparation” on page 9-18 as required.**
2. **Disconnect the power cable at J3302 on the motherboard.**
3. **Disconnect the power cable at J3303 on the motherboard.**
4. **Disconnect the power cable at J3601 on the motherboard.**
5. **Disconnect the power cable at J3603 on the motherboard.**
6. **Disconnect the RMM power cable at J3608 on the motherboard.**
7. **Disconnect the SCSI data cable at J5002 on the motherboard.**
8. **Disconnect the FC-AL data cable at J2901 on the motherboard.**
9. **Disconnect the power interlock cable at J3602 on the motherboard.**
10. **Remove the three screws securing the motherboard to the rear chassis panel.**
11. **Move the motherboard towards the front of the unit to disengage the I/O sockets from the rear panel of the chassis.**

    See FIGURE 9-11. Ensure that you do not damage the EMI shielding surrounding the I/O connectors.

12. **Carefully lift the motherboard from the chassis and place it on the antistatic mat.**

    Lift the left-hand side of the motherboard first to ensure that the capacitors located at the right-hand side of the board do not foul the SCCR mountings on the chassis side panel.

13. **Note the settings of the Flash PROM jumpers, J2103 and J2104, so that they can be transferred to a new motherboard.**

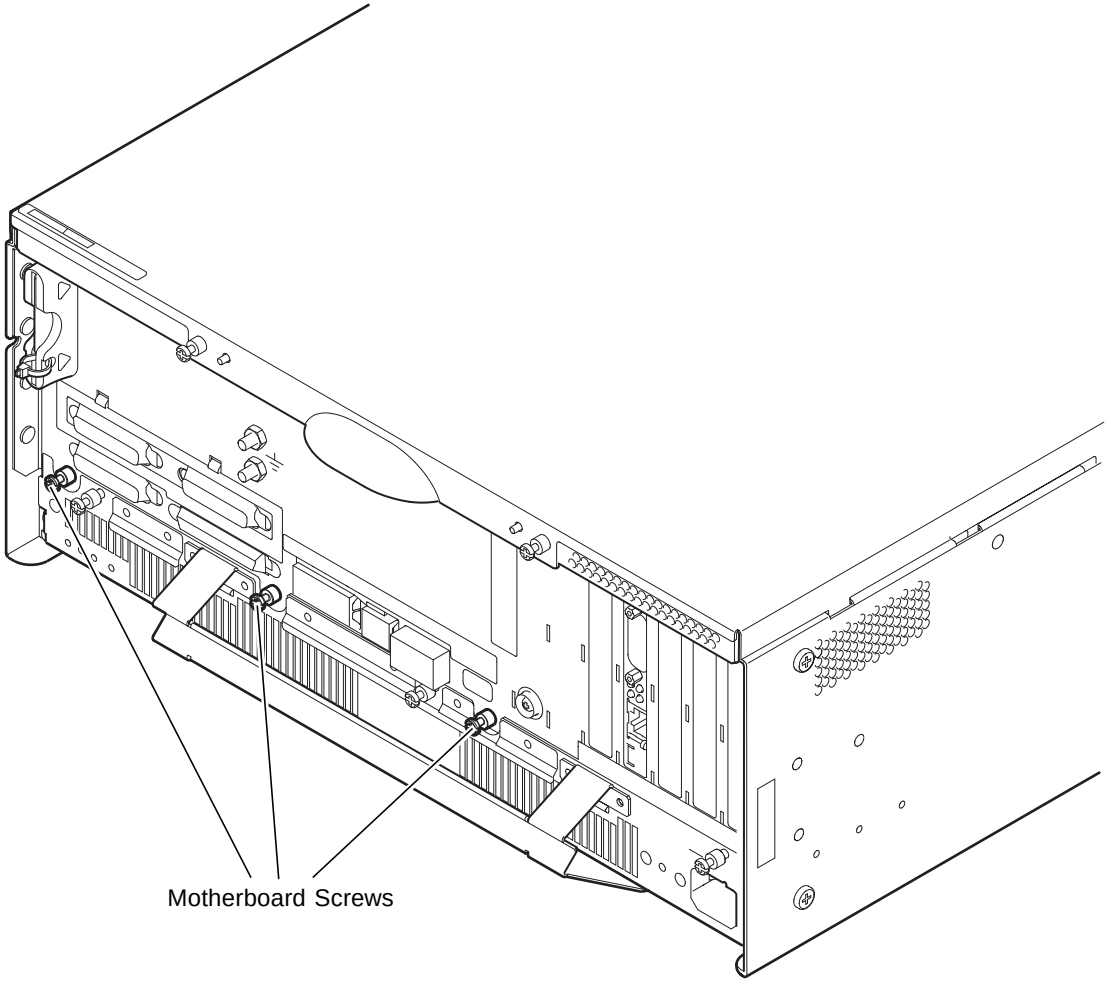


FIGURE 9-10 Motherboard Fixing Screws

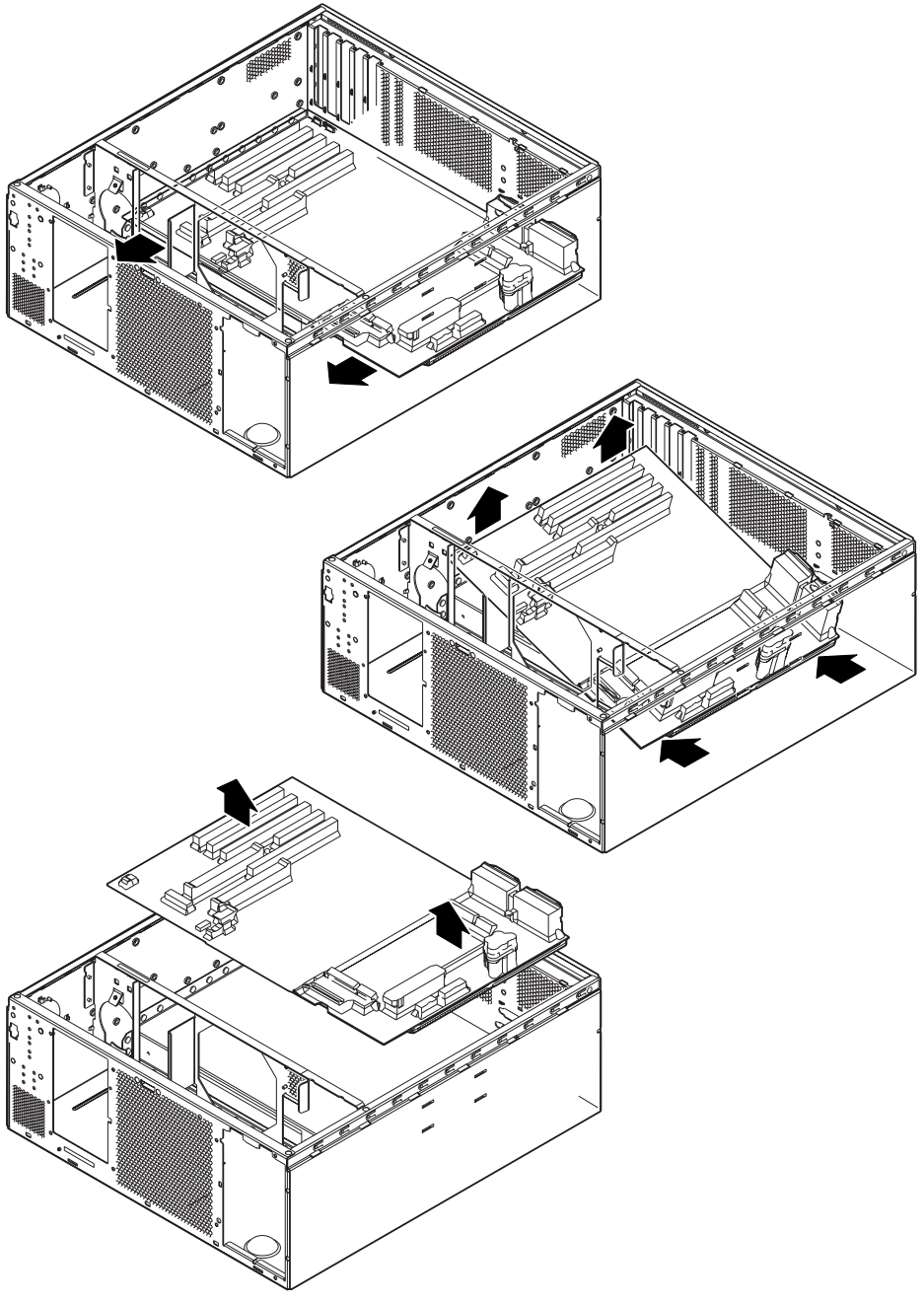


FIGURE 9-11 Removing the Motherboard from the Chassis

9.7.3 Installing the Motherboard

1. **Perform the steps listed in Section 9.7.1, “Preparation” on page 9-18 as required.**
2. **Remove the motherboard from its protective antistatic packaging and place it on the antistatic mat.**
3. **Set the Flash PROM jumpers J2103 and J2104, to the same settings as those on the motherboard being replaced.**
4. **Locate the motherboard in the chassis with the I/O sockets to the rear and move it towards the rear until the sockets engage with the cutouts in the rear panel of the chassis.**

Caution – Ensure that you do not damage the EMI shielding.

5. **Secure the board with the screws removed in Step 10 in the previous section.**
6. **Refit the SCCR and system configuration card.**
   See Section 9.6.3, “Installing the SCCR” on page 9-17.
7. **Fit any memory modules to be installed.**
   See Section 9.3.3, “Installing a Memory Module” on page 9-11.
8. **Reconnect the power interlock cable to J3602 on the motherboard.**
9. **Reconnect the FC-AL data cable to J2901 on the motherboard.**
10. **Reconnect the SCSI data cable to J5002 on the motherboard.**
11. **Reconnect the RMM power cable to J3608 on the motherboard.**
12. **Reconnect the power cable to J3603 on the motherboard.**
13. **Reconnect the power cable to J3601 on the motherboard.**
14. **Reconnect the power cable to J3303 on the motherboard.**
15. **Reconnect the power cable to J3302 on the motherboard.**
16. **Refit the CPU module(s).**
    See Section 9.2.3, “Installing a CPU Module” on page 9-7.
17. **Refit the LOMlite2 card.**
    See Section 9.5.3, “Installing the LOMlite2 Card” on page 9-15.
18. **Refit the PCI card(s).**
    See Section 9.1.3, “Installing a PCI Card” on page 9-3.

19. **Refit the CPU fan assembly.**

    See Section 7.2.3, “Installing the CPU Fan Assembly” on page 7-7.

20. **If necessary, refit the FC-AL drive assembly.**

    See Section 8.2.3, “Installing the FC-AL Backplane and Drive Bay” on page 8-9.

21. **If necessary, refit the RMM drive assembly.**

    See Section 8.3.3, “Installing a Removable Media Module” on page 8-12.

22. **Refit the top access cover.**

    See Section 5.6.3, “Fitting the Top Access Cover” on page 5-9.

PART II System Reference

CHAPTER 10

Functional Description

This chapter provides functional descriptions for the following:

- Section 10.2, “System Overview” on page 10-2
- Section 10.3, “Power Supply” on page 10-36
- Section 10.4, “Motherboard” on page 10-37
- Section 10.5, “Jumper Descriptions” on page 10-40

10.1 System

This section is organized into the following subsections:

- Section 10.2, “System Overview” on page 10-2
- Section 10.2.1, “UltraSPARC-III Processor” on page 10-3
- Section 10.2.2, “Main Memory” on page 10-6
- Section 10.2.3, “I/O Subsystem” on page 10-11
- Section 10.2.4, “Interrupts” on page 10-16
- Section 10.2.5, “BootBus” on page 10-17
- Section 10.2.7, “PCI Bus” on page 10-22
- Section 10.2.8, “Peripherals” on page 10-24
- Section 10.2.9, “Other Peripheral Assembly Options” on page 10-25
- Section 10.2.10, “USB Ports” on page 10-25
- Section 10.2.11, “Parallel Port” on page 10-26
- Section 10.2.12, “Serial Port” on page 10-27
- Section 10.2.13, “Ethernet” on page 10-31
- Section 10.2.14, “FC-AL Subsystem” on page 10-32
- Section 10.2.15, “SCSI” on page 10-33
- Section 10.2.16, “SuperI/O” on page 10-35

10.2 System Overview

The Netra T4 AC100 is available as a single or dual UltraSPARC-III processor controlled server system. The Netra T4 uses shared-memory multiprocessor architecture with both processors installed on a single motherboard (See FIGURE 10-1.

Each UltraSPARC-III processor has a memory controller installed within the processor. When two UltraSPARC-III modules are installed on a Netra T4 system, only the memory controller installed in CPU slot 0 is enabled.

The Netra T4 I/O subsystem is designed around a system bus controller (SBC) ASIC, which is a bridge between the Sun CrossBar Interconnect address bus and the 33MHz and 66MHz PCI buses.

The two PCI buses interface with the FC-AL controller and any other boards that are installed in the PCI slots. A 33MHz PCI bus (PCI-B) supports SCSI controllers that interface with the internal DVD-ROM, or DAT drives. A 66MHz PCI bus (PCI-A or EPCI for extended PCI bus) supports the Fibre Channel-Arbitrated Loop (FC-AL) controller that interfaces with the hard disk drives.

The 33MHz PCI-B I/O buses support the Peripheral Component I/O-2 (PCIO-2) ASIC. This ASIC is an interface between the 33MHz PCI bus, external universal serial buses (USB), the 10/100 Mbit Ethernet ports, the boot PROM, and the EBus.

Note – EBus is a slow byte-wide bus for low-speed devices such as the serial port controller, the SuperI/O controller (used primarily as a parallel port interface), and the boot PROM.

A BootBus controller (BBC) ASIC is connected to both UltraSPARC-III modules through a shared BootBus. The BBC ASIC bridges the BootBus to the EBus, to which slow I/O devices and the boot PROM are attached. The BBC ASIC incorporates an inter-integrated circuit (I2C) bus interface and a JTAG master controller. The I2C controller is used to identify the processor modules, the DIMMs and for environmental control. The JTAG master controller is used for boundary testing on the system board, ASIC, and processor testing.

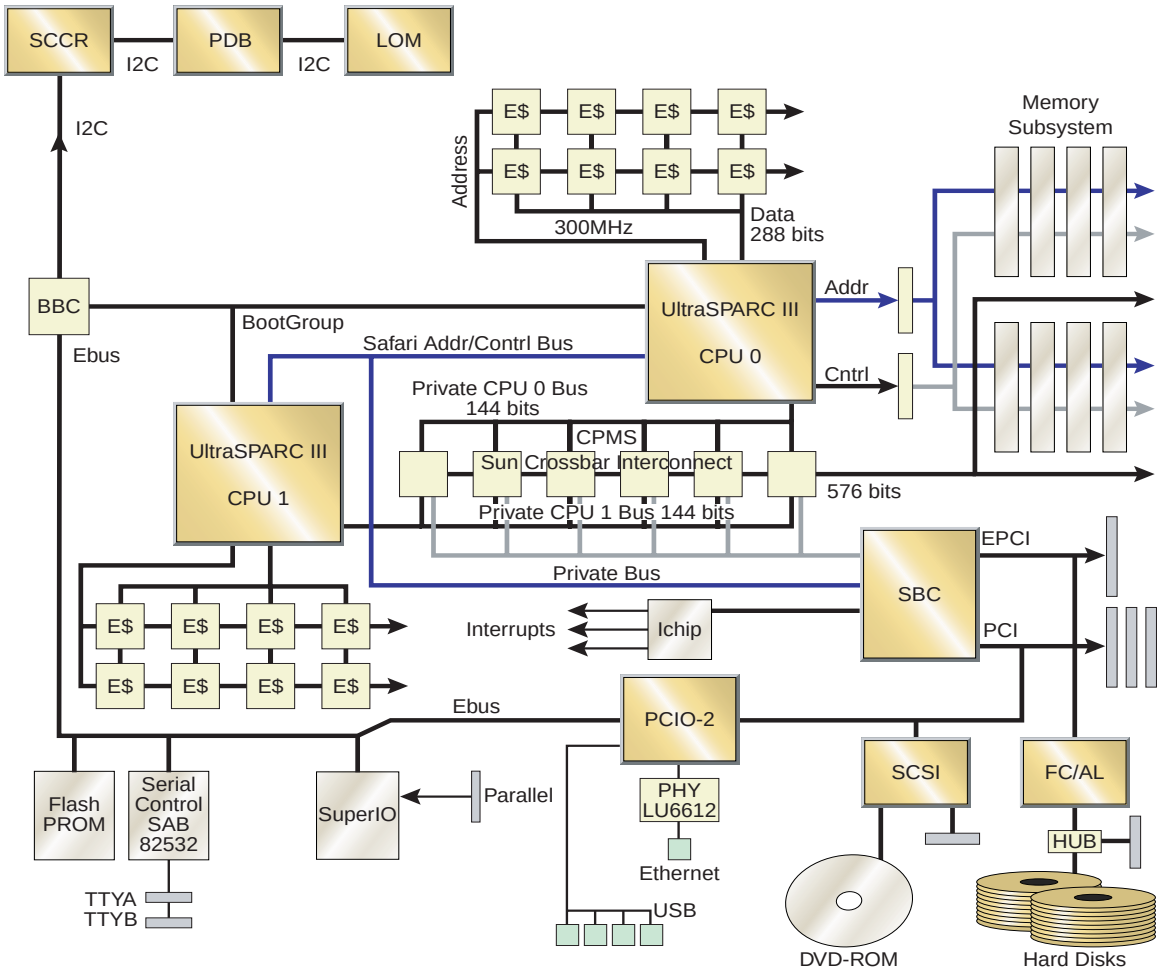


FIGURE 10-1 Netra T4 Logical System Diagram

10.2.1 UltraSPARC-III Processor

Each UltraSPARC-III processor (CPU module) implements the SPARC V-9 architecture with the Visual Instruction Set (VIS™) extension. The CPU module also provides new VIS extensions along with prefetch instructions. FIGURE 10-2 is a functional block diagram of the UltraSPARC-III processor.

The CPU is physically mounted on a module that plugs vertically into the system motherboard. The module contains the processor and eight external cache SRAMs, available either as 4-Mbyte (8 x 4-Mbit) SRAMs or as 8 Mbyte (8 x 8 Mbit) SRAMs.

The module also includes a DC-to-DC converter to limit the current density in the connector at the male/female interface and provide better power regulation at the pins of the processor.

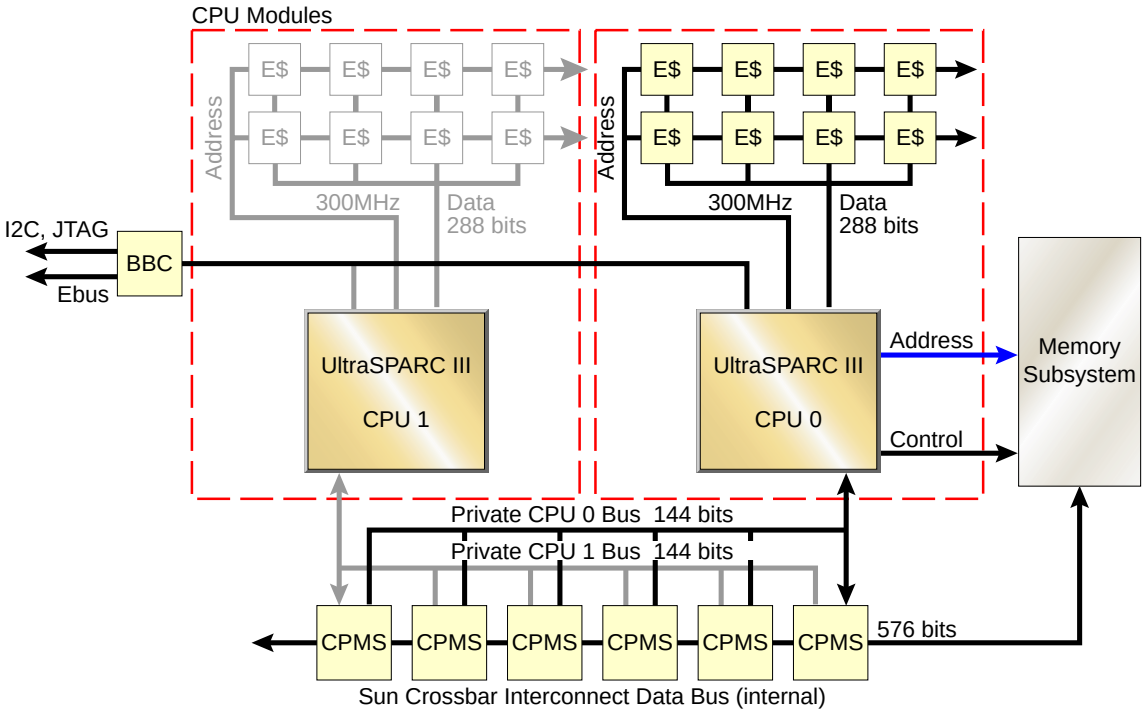


FIGURE 10-2 UltraSPARC-III Processor Functional Block Diagram

The base CPU module frequency is 750 MHz.

Note – The two UltraSPARC-III CPUs need not run at the same frequency.

Each CPU module plugs vertically into the motherboard through a set of two connectors. Each module is equipped with a mechanical insertion/extraction mechanism.

The processors are interconnected through the Sun CrossBar Interconnect bus but the CPU module(s) only support the Sun CrossBar Interconnect address and command signals. The Sun CrossBar Interconnect address and control signals, together with the data signals and the switch control signals, are routed through the module connectors.

The Ultra SPARC-III processors directly supports the main memory SDRAM. The memory controller is on the same die as the processor. The address and control signals for the SDRAM chips originate at the CPU chip pins and are routed to the motherboard through the module connectors.

Note – Only the module in slot CPU0 has an active memory controller.

The SBC (I/O ASIC chip) interface to the Combined Processor Memory Switch (CPMS) chips on the motherboard is through a private data bus, 72 bits wide, of which 8 bits are used for ECC (see FIGURE 10-3).

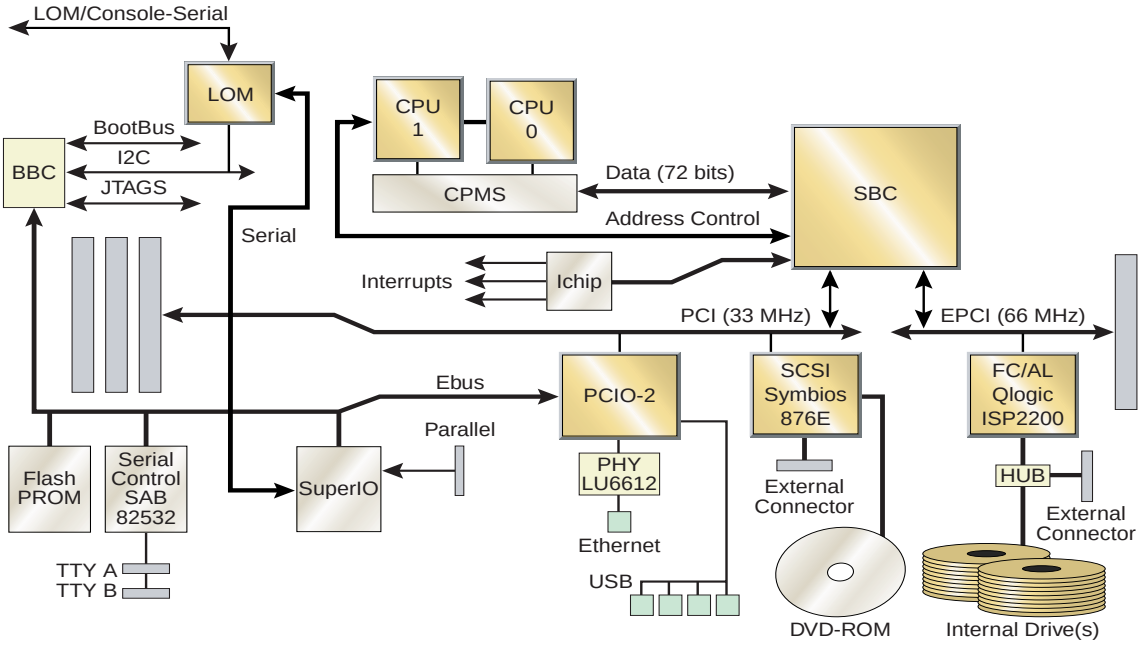


FIGURE 10-3 I/O Logical Diagram

The CPUs contain serial EEPROMs for self-identification at boot time. The SEEPROM is interfaced through the I2C bus and provides the version of the CPU module, the size and speed of the external cache, the maximum internal frequency of the processor, and other operating parameters.

Thermal management relies on high air flow and a large heat sink radiation area to maintain uniform temperature control for the CPU module(s). The temperature of the CPU module(s) is monitored to avoid any destructive effect in case of fan failure. The CPU die contains a temperature sensing diode that is connected to a temperature controller located off the die. This temperature controller performs the analog-to-digital temperature conversion and is interfaced through the I2C serial bus.

10.2.2 Main Memory

The memory subsystem comprises to memory groups and four logical banks. The memory groups are divided into even and odd slots. A configuration is valid only if at least the odd or even slots are filled with four DIMMs of the same density.

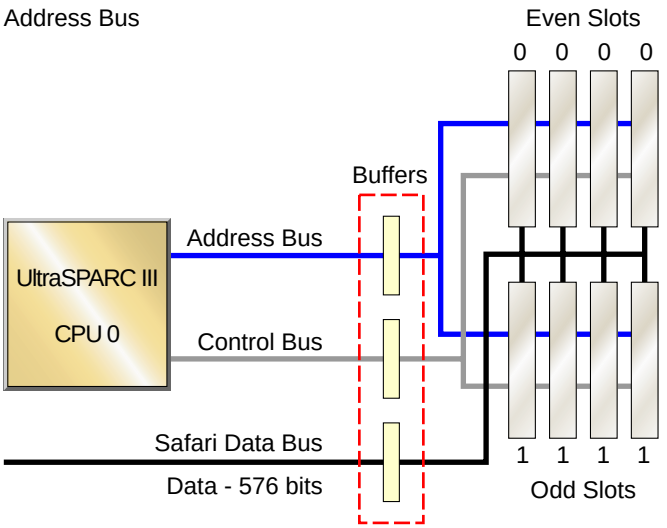


FIGURE 10-4 Memory Subsystem

10.2.2.1 Organization

As shown on FIGURE 10-1, direct access to the system main memory is controlled only by one of the two CPU modules in a multiprocessor environment. Memory is accessed from UltraSPARC Processor 0 through the Sun CrossBar Interconnect bus.

The main memory data bus is 576 bits wide, which corresponds to an external cache block of 64 bytes. The systems main memory delivers an entire block of information on external cache in a single memory bus cycle. This delivery method provides up to 2.4Gbps of sustainable bandwidth.

The main memory is implemented with x144 DIMMs, also referred to as NG-DIMMs (Next Generation Dual-Inline Memory Modules). The system supports up to eight installed NG-DIMMs.

Note – The memory bus is clocked at half the system frequency through a clock connected directly to the CPU module.

The DIMMs also support a SEEPROM for identifying and configuring subsystem memory.

The CPU module memory controller performs reads and writes in blocks of 64 bytes. On non cacheable reads the extraneous data is dropped. On non cacheable write, the processor must perform a read-modify-write. The memory space is cached.

The memory subsystem supports 2- and 4-way logical interleaving. The unit of interleaving is a logical bank. A group of four DIMMs corresponds to two logical banks for interleaving purposes. The interleaving is based on multiples of 64 bytes. Main memory interleaving is described in more details in Section 10.2.2.3, “Interleaving” on page 10-10.

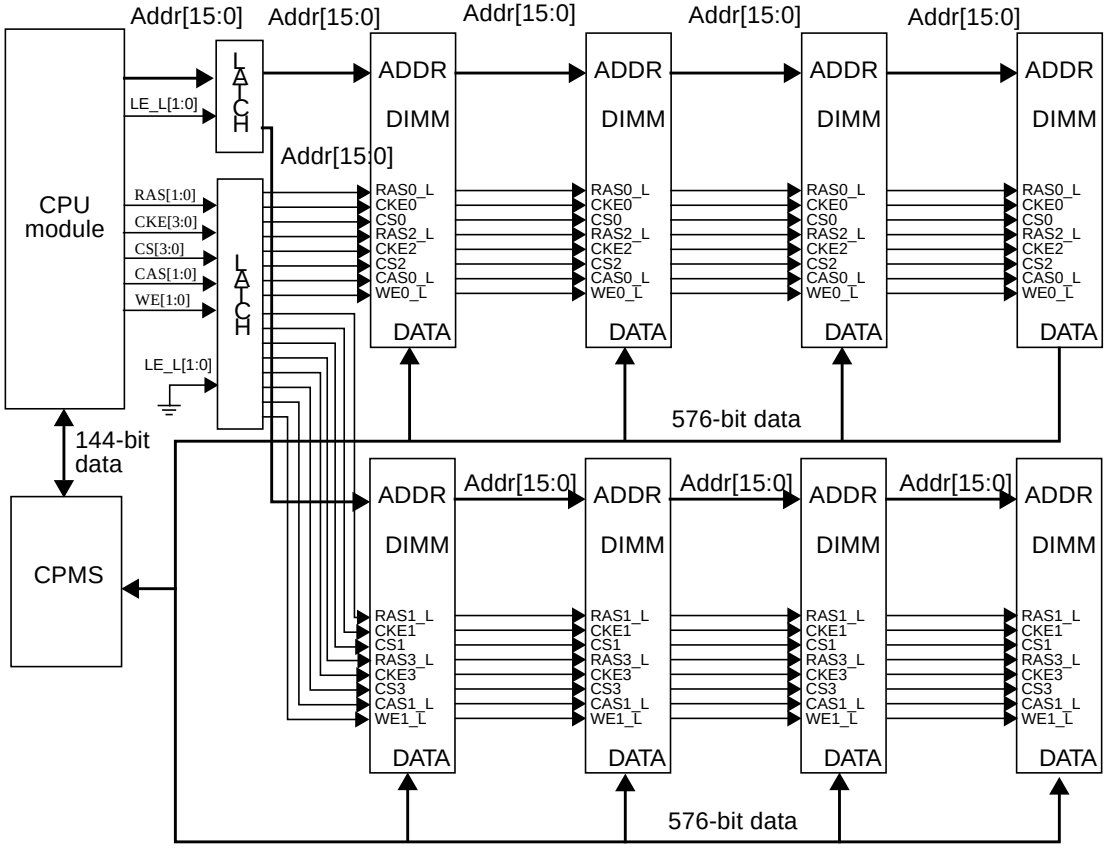


FIGURE 10-5 Main Memory Functional Block Diagram

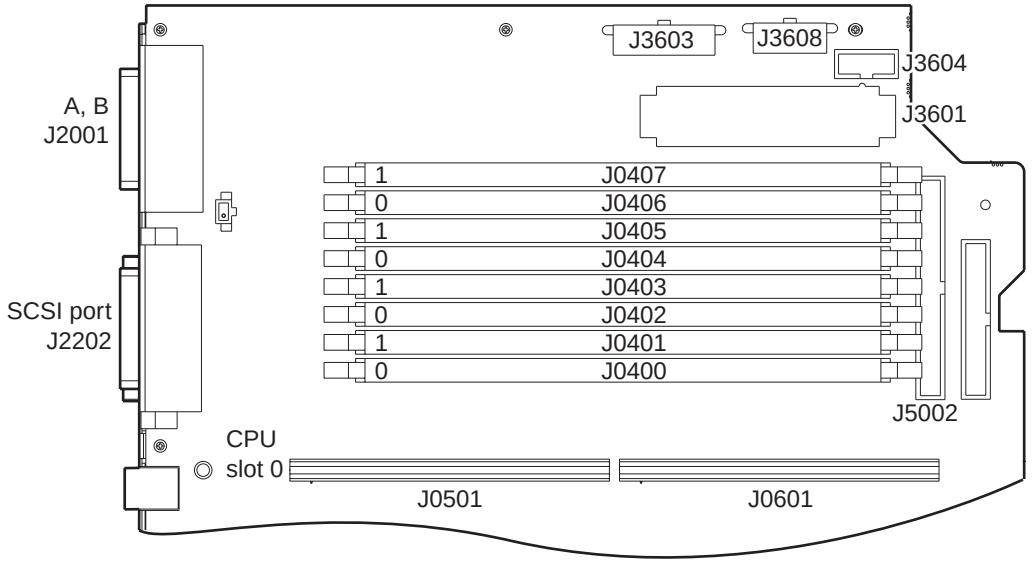


FIGURE 10-6 DIMM Mapping

10.2.2.2 Memory Configuration

The following table describes the valid memory configurations:.

TABLE 10-1 Valid Memory Configurations

Total Configured Memory Density	Even Bank 0 DIMMs	Odd Bank 1 DIMMs	Interleaving
512 MByte	128 MByte	empty	2-way
512 MByte	empty	128 MByte	2-way
1.0 GByte	128 MByte	128 MByte	2-way / 4-way
1.0 GByte	256 MByte	empty	2-way
1.0 GByte	empty	256 MByte	2-way
1.5 GByte	256 MByte	128 MByte	2-way
	128 MByte	256 MByte	2-way
2.0 GByte	256 MByte	256 MByte	2-way / 4-way
	512 MByte	empty	2-way
	empty	512 MByte	2-way
2.5 GByte	512 MByte	128 MByte	2-way
	128 MByte	512 MByte	2-way

TABLE 10-1 Valid Memory Configurations *(Continued)*

Total Configured Memory Density	Even Bank 0 DIMMs	Odd Bank 1 DIMMs	Interleaving
3.0 GByte	512 MByte	256 MByte	2-way
	256 MByte	512 MByte	2-way
4.0 GByte	512 Mbyte	512 MByte	2-way / 4-way
	1 GByte	empty	2-way
	empty	1 GByte	2-way
4.5 GByte	1 GByte	128 MByte	2-way
	128 MByte	1 GByte	2-way
5.0 GByte	1 GByte	256 MByte	2-way
	256 MByte	1 GByte	2-way
6.0 GByte	1 GByte	512 MByte	2-way
	512 MByte	1 GByte	2-way
8.0 GByte	1 GByte	1 GByte	2-way / 4-way

10.2.2.3 Interleaving

The main memory supports interleaving on 64-byte boundaries. The memory system supports from one to four logical banks. The DIMMs support two banks. For interleaving purposes, all banks are treated identically regardless of their physical location. Two successive accesses to distinct logical banks located in the same group of DIMMs are processed the same as accesses to logical banks that are in separate groups of DIMMs.

The memory controller for the Netra T4 system supports 2-way and 4-way interleaving.

The main memory is accessed only on 64-byte block reads or writes. The interleaving is based on a 64-byte addressing and the four low-order bits of a block physical address (PA[9:6]) determine the bank within a memory segment. The stride on which banks are interleaved is 64 bytes (no interleaving), 128 bytes (2-way interleaving), 256 bytes (4-way interleaving).

In only one configuration is it possible to interleave by four. Both groups must be populated with DIMMs of the same size supporting two banks.

10.2.2.4 Memory Timing

The CPU module memory controller is programmable so that different SDRAM speeds can be accommodated at different system clock frequencies and different processor clock ratios. The memory bus timing is controlled by a set of four memory timing control registers.

Memory Timing Values

The timing values for a given configuration depend on the following factors:

- Speed of the SDRAM

  The frequency of the SDRAM chip is indicated in the serial ID EEPROM on each DIMM. When two groups of four DIMMs are present, the SDRAM speed is considered the speed of the slowest SDRAM chip in the group.

- DIMM implementation

  The implementation of the DIMM influences the timing parameters, in the same way that the traces on the DIMM board define the memory bus topology. The DIMM also supports a buffer for the address and control signals. The serial ID PROM identifies the DIMM and by default defines a given implementation.

- System clock frequency (Sun CrossBar Interconnect frequency)

  The memory bus clock generated by the CPU module is half the system clock frequency. The timing parameters are relative to this clock.

- System implementation

  The memory subsystem implementation also defines the timing parameters. The term “implementation” refers to the motherboard and all the chips that are part of the memory bus. A given implementation of a Netra T4 system defines a set of timing parameters.

- Processor clock ratio

  The UltraSPARC III module clock speed is a multiple x4, x5, or x6 of the system clock. Timing parameters are defined in terms of processor clocks, which means that the processor frequency must be adjusted before programming the memory timing control registers.

10.2.3 I/O Subsystem

The I/O subsystem is designed around two bridge ASICs—system bus controller (SBC) and PCIO-2. SBC is the bridge between the Sun CrossBar Interconnect bus and the two PCI buses. PCIO-2 is the bridge between the 33MHz PCI bus and USB, 10/100-Mbit Ethernet, and EBus. The graphics slot (UPA64S) is not used on the Netra T4 system.

10.2.3.1 SBC ASIC

The SBC ASIC supports the full Sun CrossBar Interconnect protocol. The CPU module interface to the 288-bit Sun CrossBar Interconnect data bus is through a 144-bit private data bus at 150MHz for a maximum bandwidth of 2.4Gbyte/sec.

SBC is composed of a Sun CrossBar Interconnect interface block and two leaf blocks (the UPA64S leaf block is not used in the Netra T4 system):

- PCI A leaf block
- PCI B leaf block

The following figure depicts the micro architecture of the SBC ASIC:

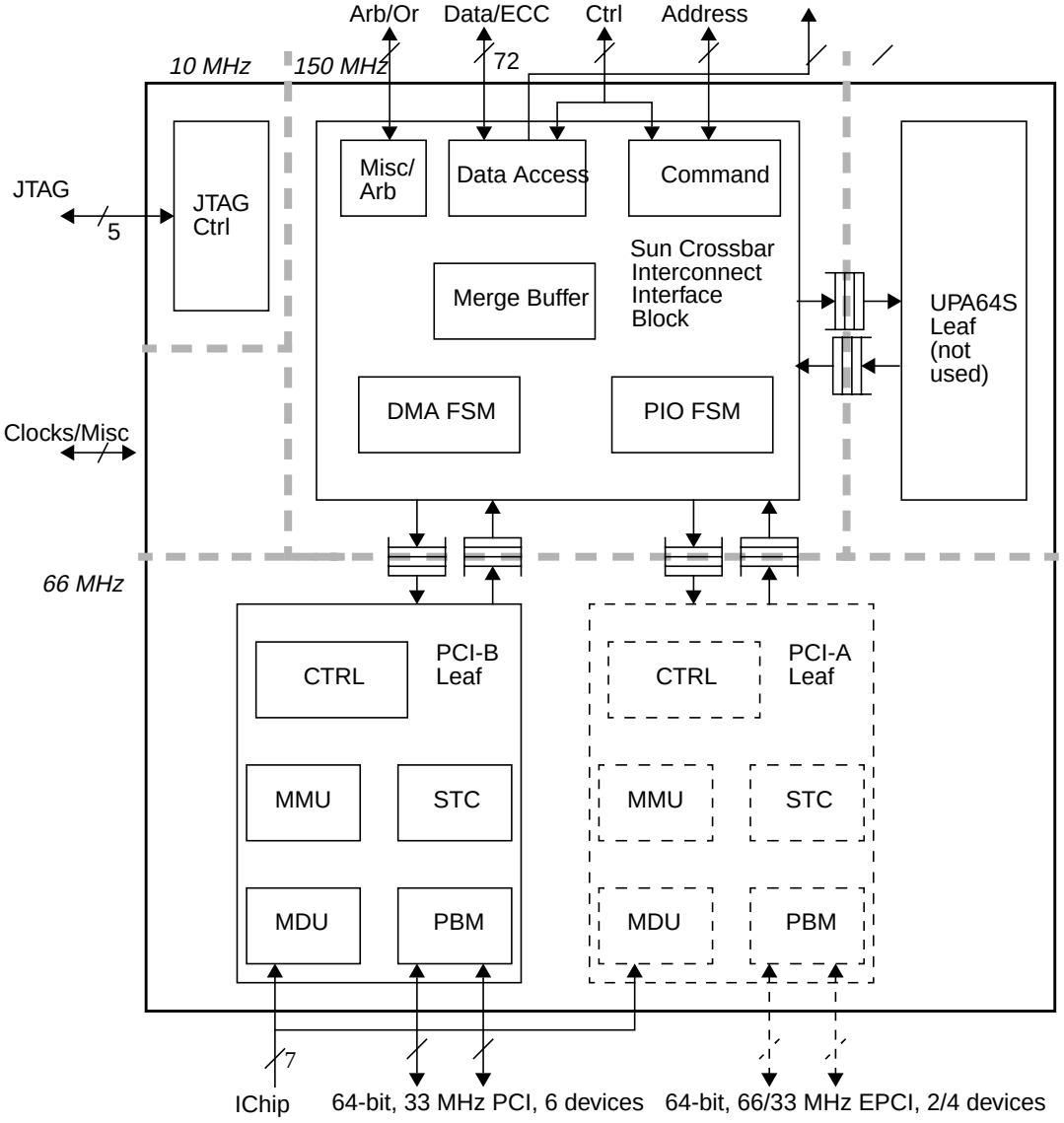


FIGURE 10-7 SBC Block Diagram

The internal interface between the Sun CrossBar Interconnect interface block and the leaf blocks is fully asynchronous. This enables the frequency of Sun CrossBar Interconnect to be tuned according to the limitations of the system. There is no relative frequency limitation, and the frequency of a leaf can be higher than the Sun CrossBar Interconnect frequency.

EPCI A Leaf Block

The extended PCI (EPCI) is the 64-bit, 66 MHz PCI. The PCI A leaf is the host controller for the EPCI. It supports 3.3V signalling only.

The PCI A leaf can support four master devices. The Netra T4 system only includes two—the EPCI slot and the FC-AL disk controller.

The micro architecture of both PCI leaves is almost identical and the PCI A leaf also supports the logic blocks mentioned above to comply with the Sun4u/Sun5 architecture.

The EPCI high-bandwidth pluggable I/O interface sustains up to 500 Mbps in streaming Direct Virtual Memory Access (DVMA) mode. See Section 10.2.7, “PCI Bus” on page 10-22 for details.

PCI B Leaf Block

The term *PCI* refers to the 33 MHz PCI bus (PCI specification revision 2.1). The PCI B leaf is the host controller for the 64-bit wide/33 MHz PCI bus. It supports both 5V and 3.3V signalling, and 32-bit devices.

The PCI B leaf supports six master devices. The Netra T4 system includes only five devices: PCIO-2, three slots, and the 876 SCSI controller.

10.2.3.2 Peripheral Component IO

The Peripheral Component IO (PCIO-2) contains a multi-function PCI interface and three leaves for each of the supported interfaces: Ethernet (10/100 Mbit), USB, and EBus (the 1394 leaf is not used). FIGURE 10-8 is a block diagram of the PCIO-2 ASIC.

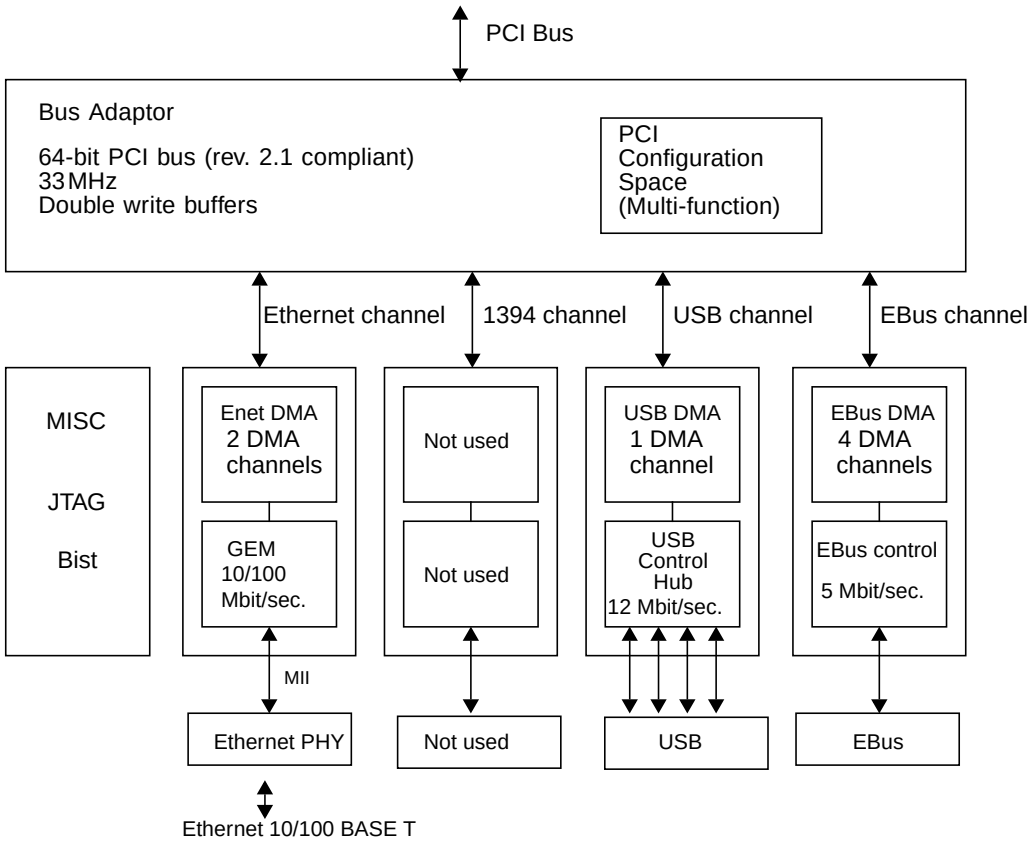


FIGURE 10-8 PCIO-2 Block Diagram

PCI Interface

The PCI-B interface is 64-bit wide at 33 MHz. It supports slave (for PIO) and master (for DMA) transactions on the PCI bus. Master transactions use 256-byte burst transfers.

Note – The byte burst rate is programmable and can vary.

The PCIO-2 is a multi-function PCI device as defined by the PCI specification, and it supports a separate configuration space for each of the three interfaces. See Section 10.2.7, “PCI Bus” on page 10-22 for details.

Ethernet Leaf

The Ethernet interface supports two DMA channels for full duplex. the PCIO-2 Ethernet interfaces through PHY 6612 and COMBO magnetics and RJ45 connector. See Section 10.2.13, “Ethernet” on page 10-31 for details.

USB Leaf

USB (Universal Serial Bus) is a standard defined for the PC industry that provides connectivity to low-cost low-bandwidth peripherals.

USB defines a tree topology through hub devices although logically it behaves as a bus. The USB standard defines two data transfer rates: 1.5 and 12 Mbit/sec. USB supports live connect and disconnect of devices (hot plugging).

The PCIO-2 USB channel engine has a single DMA engine with 1Kbit of internal buffering. It serves as the USB host controller and a hub with four ports. As a host controller it manages control flow, data flow and connections. The PCIO-2 USB host controller programming model is Open HCI compatible.

10.2.3.3 EBus Leaf

EBus is a byte-wide I/O bus that provides the ability to interface to instruction set architecture devices. In a Netra T4 system there are four devices on this bus (the audio module is not used):

- Boot PROM (Flash memory)
  - OpenBoot PROM (OBP) prompt
  - Power On Self Test (POST)
  - OpenBoot Diagnostics (OBDiag)
- Synchronous serial controller (RS-232/RS-423 ports)
- SuperI/O chip
  - Parallel port
  - TOD clock (socketed 3V lithium battery)
- I2C controller

The TOD clock function is implemented by the real time clock inside the SuperI/O ASIC. The nonvolatile RAM is implemented by a I2C serial EEPROM and part of the boot PROM.

The EBus channel engine also supports four DMA controllers with programmable transfer size and chained and unchained mode. Only one device supports slave DMA transfers on EBus: SuperI/O for the parallel port (single DMA engine).

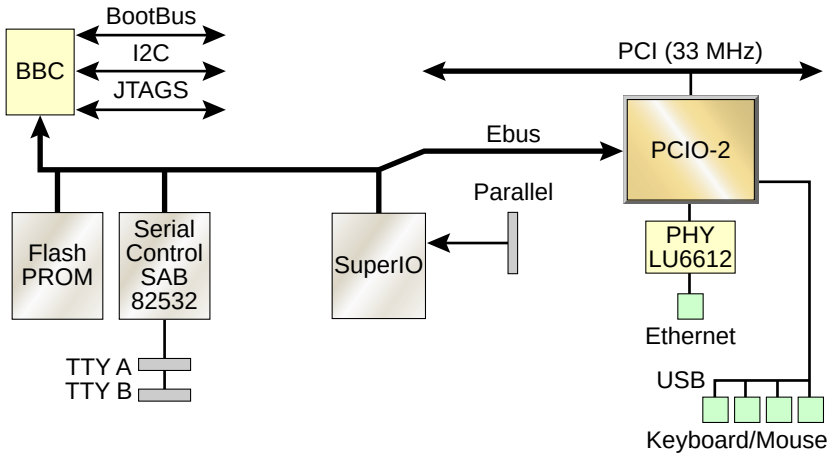


FIGURE 10-9 Ebus

10.2.4 Interrupts

The interrupt model in a Netra T4 system follows the Sun4u/Sun5 architecture. Interrupts are delivered to the processor(s) as Mondo vectors. The CPU receives interrupt packets that are issued over the Sun CrossBar Interconnect bus. The processors can issue interrupts to each other (called cross-calls). They are issued by SBC for I/O interrupts. All interrupts that are not cross-called are referred to as I/O interrupts.

I/O interrupts are issued on separate lines by the various on-board devices, the PCI cards, and UPA cards. The interrupts are routed to an interrupt concentrator: the I-chip that encodes the interrupts and delivers them to the SBC. The SBC issues a single Sun CrossBar Interconnect interrupt transaction for each active interrupt.

FIGURE 10-10 shows the overall interrupt organization in the Netra T4 system:

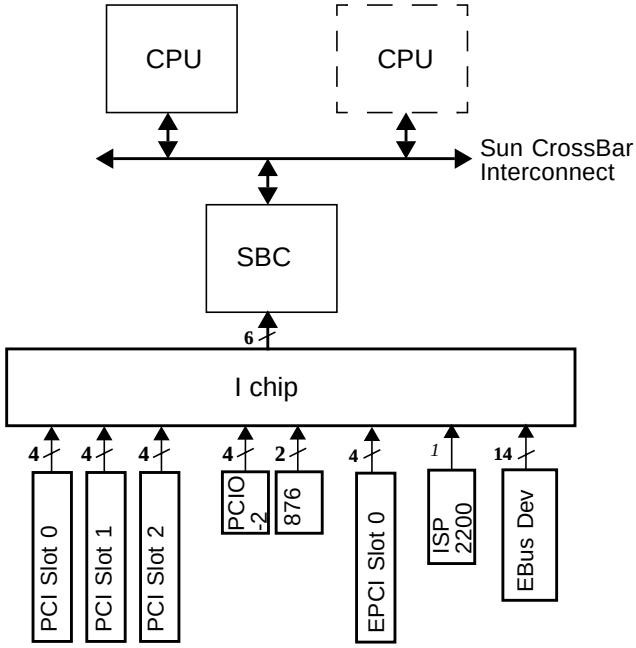


FIGURE 10-10 System Interrupt Block Diagram

10.2.5 BootBus

The CPU modules support an alternate 8-bit bus (the BootBus) used after a reset to fetch the first instruction they execute.

The address space of the BootBus corresponds to the boot PROM addressing space as defined by the Sun4u/Sun5 architecture. The CPU issues its SPARC V9 RED_MODE trap vectors from this address space.

FIGURE 10-11 shows how the CPUs access the boot PROM through the BootBus, the BBC, and EBus:

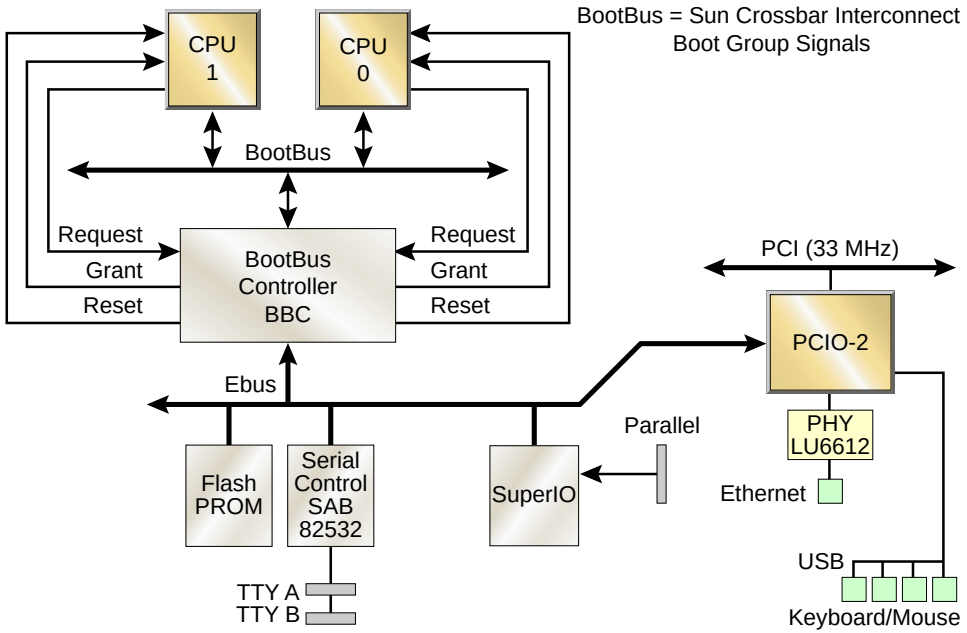


FIGURE 10-11 Netra T4 Boot Bus

10.2.5.1 BootBus Controller (BBC) ASIC

The BootBus controller provides access to the boot PROM by bridging the Sun CrossBar Interconnect BootGroup signals (the BootBus) and the EBus. The boot PROM connects directly to the EBus.

The PCIO-2 is also a master on the EBus. Full arbitration between the PCIO-2 and the BBC controls access to the EBus. The EBus is accessed from the BBC only during the boot sequence that is, during the execution of POST and OpenBoot PROM.

Note – When the system is running Solaris software, the kernel has no knowledge of the BootBus space.

Access to the boot PROM through the BBC is optimized for 16-byte master accesses performed by the CPU on the BootBus.

BBC is also a slave on the EBus and all its internal registers are accessible through the PCIO-2. Thus software drivers running on Solaris software can access the necessary resources such as the thermal management driver.

BBC also supports many other functions that are briefly introduced in the following subsections.

Reset Controller

The BBC is the reset controller in the Netra T4 system. The controller receives the reset source lines and is responsible for generating the reset signals for the CPU module(s) and the overall system. The external sources for reset include the Power Up reset from the power supply, the reset buttons on the motherboard, the SuperI/O watchdog timer, and fatal error conditions.

The reset controller also includes registers that a processor uses to generate an external reset to itself or another processor.

JTAG Controller

BBC is the host for the JTAG+ controller that includes a programmable master tap controller. This enables processors to access the JTAG scan rings in the system by simply executing programmed I/O operations to the BBC master tap controller registers. The processor(s) can access the internal scan chain of all the ASICs and perform different levels of testing (boundary scan, internal scan for ATPG, RAM tests, and BIST if available).

The JTAG+ controller enables an external JTAG master to be connected to the motherboard for controlling all scan rings including the processor(s) scan ring(s) and the BBC internal scan ring.

I2C Buses

The BBC supports five master I2C buses and a single multi-master I2C bus.

Small I2C serial EEPROMs make it possible to identify pluggable modules that cannot be identified easily through their regular data path. The DIMMs include an I2C serial EEPROM that contains information relative to the size and the speed of the DRAM. The CPU modules include an I2C EEPROM, which indicates the size of the second level cache and the speed of the processor.

Sensors on the CPU modules provide temperature data that is read through an analog-to-digital converter with an I2C interface.

The multimaster I2C bus is used in the Netra T4 system to connect to the SCCR interface. The SCCR performs a 3.3VDC to 5VDC voltage translation to interface with the PDB I2C devices. The LOMlite2 module connects into the I2C bus at the PDB and is the second I2C multimaster device.

See also Section 10.2.6, “I2C Bus” on page 10-20.

Clock Synthesizers

The BBC ASIC supports another serial interface to access the clock synthesizers. Synthesizers allow frequency margining on the system clock.

After a power-on reset, the clock frequency for the system is set at a default low frequency (100 MHz). The multiplier in the CPU modules also are set at their lower value. The POST/OpenBoot PROM software determines the optimal system frequency by reading the I2C EEPROMs on the module and the motherboard. The POST/OpenBoot PROM software programs the new multiplier values in the CPU processors and adjusts the frequency of the synthesizers. A subsequent reset will activate the new multiplier values inside the processors.

Note – The Netra T4 system can accommodate two processors running at different speeds.

10.2.6 I2C Bus

The main purposes of the I2C buses are:

- Environmental control
- Configuration identification
- Remote system monitoring
- Remote system management

At boot time, the I2C bus is used by POST and OBP to identify the current configuration. POST and OBP access the SEEPROM on each processor board to determine:

- System configuration
- CPU clock ratio
- Ecache size
- Processor module version
- DIMM sizes
- SCC contents

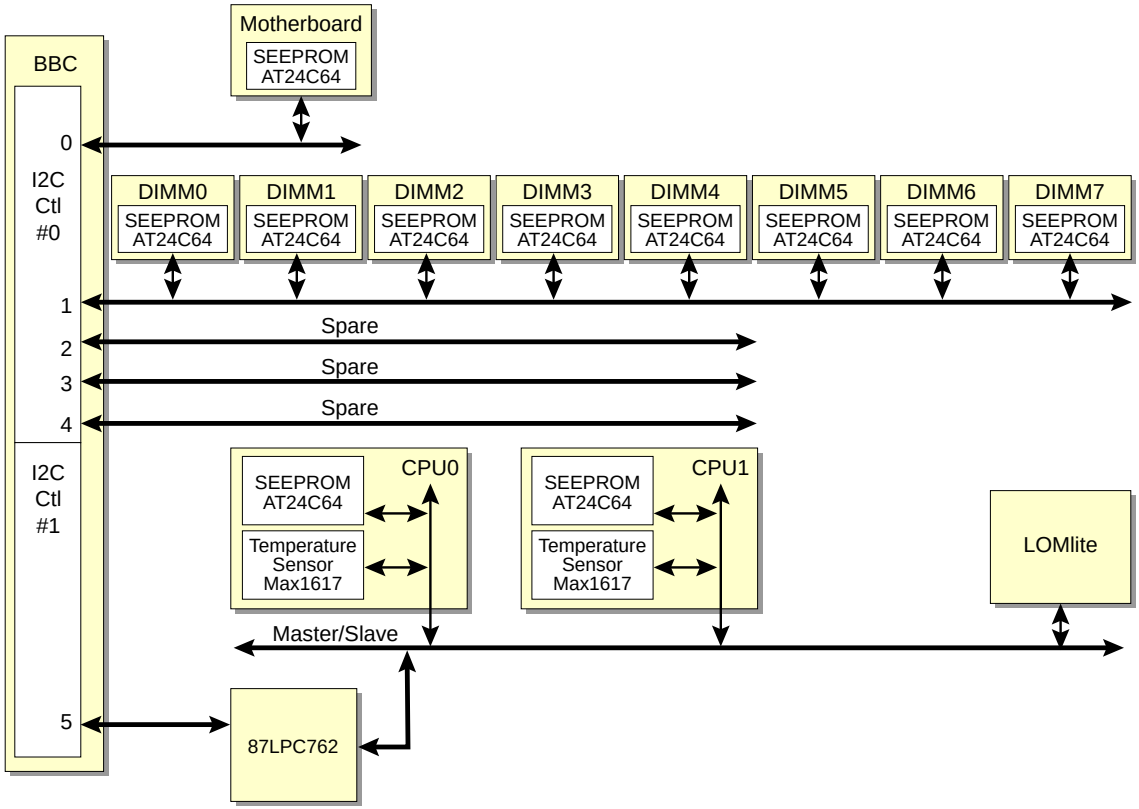


FIGURE 10-12 I2C Bus

In addition, located on the motherboard is a soldered I2C SEEPROM containing the FRU ID structure.

POST and OBP also access the SEEPROMs in each of the DIMMs, which indicate their density and type. This data can be used to configure the active memory controller. The Ethernet address and host ID can be transferred to another system (in case of motherboard failure) by using the system configuration card and reader to overwrite the EEPROM contents with the original motherboard's identification parameters.

The I2C bus is also used to monitor CPU die temperatures through sensors in each CPU chip and on the processor board. The I2C bus monitors the fan speed, using LM80s on the PDB, and power supply status.

The I2C multimaster bus interfaces with the following devices:

- System configuration card reader (SCCR)
- FC-AL backplane
- Power distribution board (PDB)
- Lights Out Management board
- LED and switch board
- Power Supply Unit

The I2C bus supports a Lights Out Management (LOMlite2) board through the I2C connector to the PDB. The LOMlite 2 board is a remote support feature that provides remote monitoring and system administration.

The LOMlite2 board is powered by a 5V standby supply that enables the board to remain powered after the host has shut down.

10.2.7 PCI Bus

The peripheral component interconnect (PCI) bus is a 32-bit or 64-bit bus with multiplexed address and data lines. The PCI bus provides electrical interconnect between highly integrated peripheral controller components, peripheral add-on devices, and the processor/memory system.

There are two PCI buses in the Netra T4 system:

- One-slot, 3.3VDC, 64-bit or 32-bit, 66MHz or 33MHz bus
- Three-slot, 5.0VDC, 64-bit or 32-bit, 33MHz bus

Both buses are controlled by the SBC ASIC. There are two on-board PCI devices, the SCSI controller and the PCIO-2 ASIC, on the 33MHz PCI bus. The ISP2200A FC-AL disk controller is located on the 64-bit, 66MHz PCI bus.

10.2.7.1 PCI Cards

PCI cards come in a variety of configurations. Not all cards fit or operate in all PCI slots, so it is important to know the specifications of your PCI cards and the types of cards supported by each PCI slot in the system.

Some PCI cards are as short as 174.6mm (6.88in.) in length—called *short* cards—while the maximum length of PCI cards is 311.9mm (12.28in.)—called *long* cards. Slots 0, 1 and 2 in the Netra T4 system can accommodate either a long or a short card, but slot 3 is restricted by the FC-AL drive assembly and can accommodate only a short card.

Older PCI cards communicate over 32-bit PCI buses, while many newer cards communicate over wider 64-bit buses.

Older PCI cards operate at 5VDC, while newer cards are designed to operate at 3.3VDC. Cards that require 5VDC will not operate in 3.3-volt slots, and 3.3-volt cards will not operate in 5-volt slots. “Universal” PCI cards are designed to operate at either 3.3VDC or 5VDC, so these cards can be inserted into either type of slot. The system provides three slots for 5-volt cards and one slot for a 3.3-volt card. All four PCI slots accept universal cards.

Most PCI cards operate at clock speeds of 33MHz, while newer EPCI cards operate at 66MHz. All four PCI slots can accept 33-MHz cards.

Note – Installing a 33-MHz card into a 66-MHz EPCI slot will slow system performance.

66-MHz cards are restricted to the slot labelled EPCI 1. The following table lists the mapping of the PCI slots to the two PCI buses, and the type of PCI cards supported in each slot.

TABLE 10-2 PCI Slot-to-PCI Bus Mapping

Connector Label	Conn. No.	PCI Bus	Slot Width (bits)/ Card Type (bits)	Clock Rates (MHz)	DC Voltage (VDC)/ Card Type
PCI 4	J2601	B	64/32 or 64	33	5/universal
PCI 3	J2501	B	64/32 or 64	33	5/universal
PCI 2	J2401	B	64/32 or 64	33	5/universal
PCI 66 1	J2301	A	64/32 or 64	66	3.3/universal

10.2.7.2 PCI Bus ASICs

SCSI Controller

The SCSI controller ASIC provides an interface between the 33-MHz PCI bus and the internal and external SCSI buses. The dual SCSI bus controller provides separate connections to internal and external devices. SCSI channel A is used for internal devices and supports the SCSI fast and narrow mode. SCSI channel B is used for external devices and supports the SCSI ultra-wide mode.

FC-AL Disk Controller

The FC-AL disk controller ASIC provides an interface between the 64-bit, 66-MHz PCI bus, the two FC-AL hard drives, and an external FC-AL connector. The FC-AL controller provides connection to internal and external devices through one channel. The FC-AL loop supports up to 125 devices. See Section 10.2.14, “FC-AL Subsystem” on page 10-32.

10.2.8 Peripherals

The following peripherals are supported by the Netra T4 system:

- Section 10.2.8.1, “DVD-ROM and DAT Drives” on page 10-24
- Section 10.2.8.2, “Hard Drives” on page 10-24
- Section 10.2.8.3, “System Configuration Card Reader” on page 10-25

10.2.8.1 DVD-ROM and DAT Drives

The DVD-ROM, and back-up devices (tape drive) are interfaced through a SCSI controller. The Netra T4 system uses a SCSI host controller on the PCI bus. This controller is used only in fast narrow mode.

Note – The DVD-ROM drive is factory set to SCSI target ID 6. Refer to the installation documentation for the DVD-ROM to change the target ID address.

10.2.8.2 Hard Drives

The system supports two internal hot-swap FC-AL hard drives. Each hard drive has a single connector configuration. A drive bracket is used to mount the drives. The following table lists the features of the Netra T4 hard drives.

TABLE 10-3 Internal Hard Drive Features

Form Factor Dimension	Hard Drive Capacity	RPM	Seek Time(read/write) (average)
1.0 inch (2.54 cm)	36GBytes	10K	7.5 ms / 8.5 ms

10.2.8.3 System Configuration Card Reader

The SCCR is attached to the I2C bus. This is a system identity device, comprising a card reader and a programmed system configuration card. The card has two functions:

- It contains the system identity parameters for the server—information such as the Ethernet MAC address, HostID and other configuration parameters
- It replaces the NVRAM for the storage of configuration variables and other non volatile data.

If a system configuration card is not present in the SCCR, the OBP initialization sequence will abort and a fatal error message is displayed. If the card is removed while Solaris is running, LOMlite2 detects its absence and initiates an orderly shutdown after 60s.

10.2.9 Other Peripheral Assembly Options

The system supports other peripheral assembly options that can be installed in the system. These options can include the DVD-ROM drive and DAT drive.

10.2.10 USB Ports

Four USB ports enable you to connect USB peripherals.

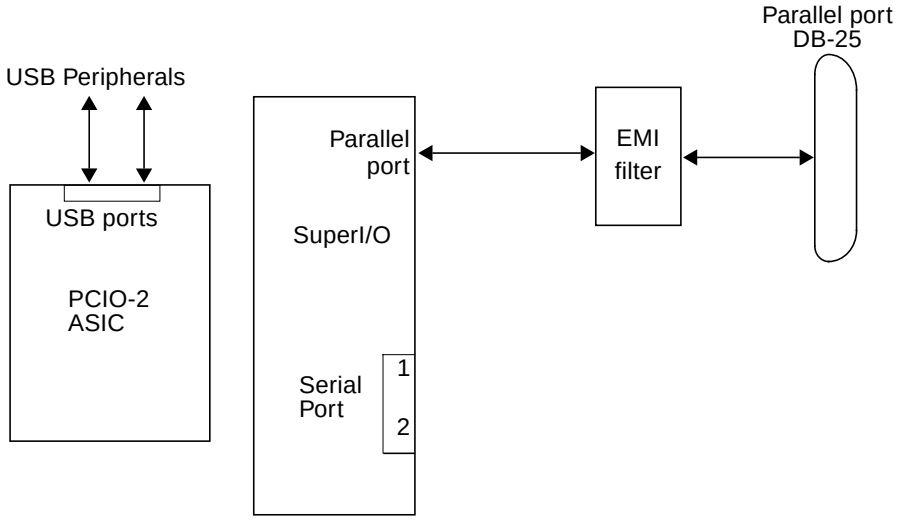


FIGURE 10-13 USB and Parallel Port Functional Block Diagram

10.2.11 Parallel Port

The parallel port is managed by the SuperI/O component.

The parallel port is supported by an IEEE 1284-compliant parallel port controller located on the SuperI/O ASIC. The parallel port controller is a PC industry-standard controller that achieves a 2-Mbits/sec. (Mbps) data transfer rate. The parallel port controller interface supports the ECP protocol as well as the following:

- Centronics—Provides a widely accepted parallel port interface.
- Compatibility—Provides an asynchronous, byte-wide forward (host to peripheral) channel with data and status lines used according to their original definitions.
- Nibble mode—Provides an asynchronous, reverse (peripheral-to-host) channel, under control of the host. Data bytes are transmitted as two sequential, four-bit nibbles using four peripheral-to-host status lines.

Parallel Port Cables

The parallel port cable is IEEE 1284-compliant and consists of 18 pairs of signal wires that are double shielded with braid and foil. The maximum length of the parallel port cable is 2 m (6.6 feet).

Electrical Characteristics

Drivers operate at nominal 5 VDC TTL levels. The maximum open circuit voltage is 5.5 VDC and the minimum is -0.5 VDC. A logic high-level signal is at least 2.4 VDC at a source current of 0.32 mA, and a logic low-level signal is no more than 0.4 VDC at a sink current of 14 mA.

Receivers also operate at nominal 5-VDC TTL levels and can withstand peak voltage transients between –2 VDC and 7 VDC without damage or improper operation. The high-level threshold is less than or equal to 2.0 VDC and the low-level threshold is at least 0.8 VDC. Sink current is less than or equal to 0.32 mA at 2.0 VDC, and source current is less than or equal to 12 mA at 0.8 VDC.

10.2.12 Serial Port

The Netra T4 server has three serial ports:

- Two ports, ttya and ttyb, are incorporated in the motherboard
- A single serial port, lom-console, is incorporated in the LOMlite2 board.

10.2.12.1 `ttya` and `ttyb`

The motherboard serial ports are synchronous and asynchronous with full modem controls. Motherboard serial port functions are controlled by a serial port controller that is electrically connected to the system through the EBus. Line drivers and line receivers control the serial port signal levels and provide RS-232 and RS-423 compatibility. Each motherboard serial port interfaces through its own DB-25 connector.

The major features of each motherboard serial port include:

- Two fully functional synchronous and asynchronous serial ports
- DB-25 connectors
- Increased baud rate (to 384 Kbaud synchronous, 460.8 Kbaud asynchronous)
- Variable edge rate for greater performance
- EBus interface

The following figure shows a functional block diagram of the serial port:

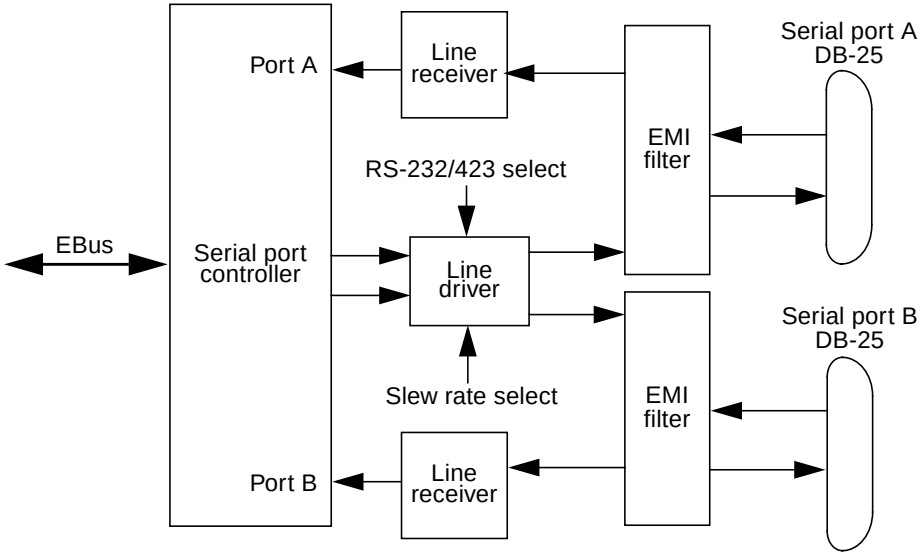


FIGURE 10-14 Serial Port Functional Block Diagram

Serial Port Components

Serial port components include a serial port controller, line drivers, and receivers.

The serial port controller contains sixty-four-byte input and output buffers that are used to reduce the CPU bandwidth requirements of the serial port controller.

Note – Interrupts are generated when the buffer reaches 32 bytes or half full.

The line drivers and line receivers are compatible with both RS-232 and RS-423 protocols. Software control sets the line drivers and line receivers to either RS-232 or RS-423 protocols. The line driver slew rate is also programmable. For rates over 100Kbaud, the slew rate is set to 10VDC/µsec. For rates under 100Kbaud, the slew rate is set to 5VDC/µsec.

Serial Port Functions

Modem connection to the serial port enables access to the Internet. Synchronous X.25 modems are used for telecommunications in Europe. An ASCII text window is accessible through the serial port on non-graphic systems. Low speed printers, button boxes (for CAD/CAM applications), and devices that function like a mouse

are also accessible through the serial port. The additional speed of the serial port can be used to execute communications with a CSU/DSU for a partial T1 line to the Internet at 384Kbaud.

EIA Levels

Each serial port supports both RS-232 and RS-423 protocols. RS-232 signaling levels are between –3VDC and –15VDC and +3VDC and +15VDC. A binary 1 (001_2) is anything greater than +3VDC and a binary 0 (000_2) is anything less than –3VDC. The signal is undefined in the transition area between –3VDC and +3VDC. The line driver switches at –10VDC and +10VDC, with a maximum of –12VDC and +12VDC in RS-232 mode.

RS-423 support is similar except that signaling levels are between –4VDC to –6VDC and +4VDC to +6VDC. The line driver switches at –5.3VDC and +5.3VDC with a maximum of –6V and +6VDC.

The preferred signaling protocol is RS-423. The higher voltages of RS-232 makes it more difficult to switch at the higher baud rates. The maximum rate for RS-232 is approximately 64Kbaud while the maximum rate for RS-423 is 460.8Kbaud. The system default is set to RS-232.

Note – The serial port protocol is changed using the OBP, not by changing a jumper setting.

Synchronous Rates

The serial synchronous ports operate at any rate from 50Kbaud to 256Kbaud when the clock is generated from the serial port controller. When the clock is generated from an external source, the synchronous ports operate at up to 384Kbaud. Clock generation is accurate within one percent for any rate that is generated between 50Kbaud and 256Kbaud.

Asynchronous Rates

The serial asynchronous ports support twenty baud rates that are all exact divisors of the crystal frequency (with the exception of 110, which is off by less than one percent). Baud rates are 50, 75, 110, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200, 38400, 57600, 76800, 115200, 153600, 230400, 307200, and 460800.

Slew Rate and Cable Length

The maximum RS-423 cable length is 30.0m (98.4ft) and the maximum RS-232 cable length is 15.24m (50.0ft). The slew rate changes depending on the speed. For speeds less than 100Kbaud, the slew rate is set at 5VDC/ms. For rates greater than 100Kbaud, the slew rate is increased to 10/ms. This enables maximum performance for the greater baud rates and better signal quality at the lesser baud rates.

10.2.12.2 `lom-console` Serial Port

The LOMlite2 serial port interfaces through an RJ45 connector on the board plate.

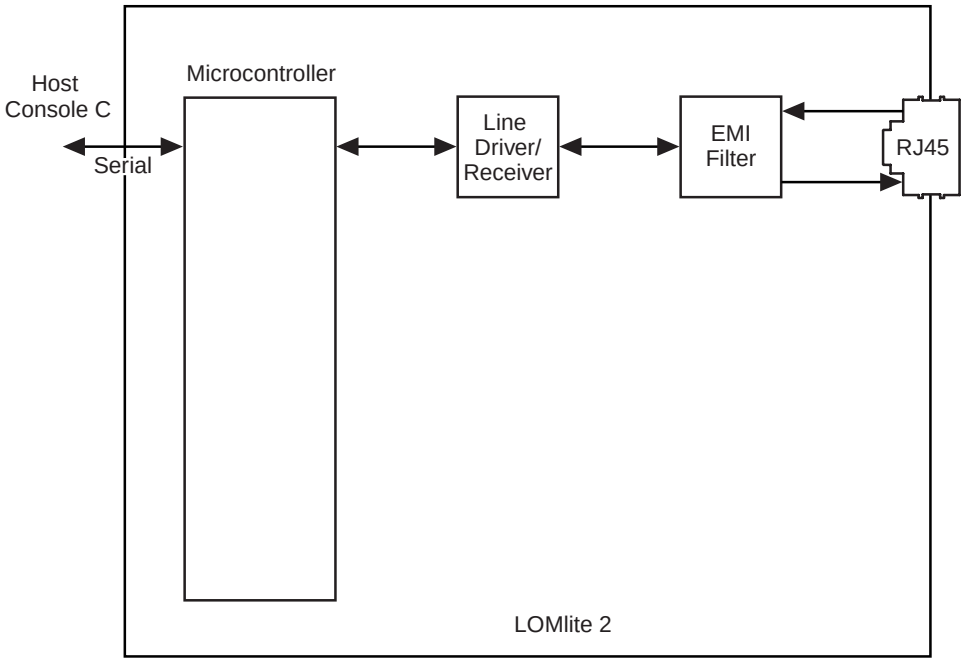


FIGURE 10-15 LOMlite2 Serial Port Functionality

The major features of the LOMlite2 serial port include:

- Single asynchronous port, switchable from LOMlite2 to console
- Single rate, 9600Baud
- 8 bit, No Parity, 1 Stop Bit
- RS232/RS423 compatibility
- RTS/CTS flow control

10.2.13 Ethernet

The system supports 10-Mbps, 10BASE T; twisted-pair Ethernet; and 100-Mbps, 100BASE T. Twisted-pair Ethernet is provided through an 8-pin RJ45 connector. The Ethernet circuitry design is based on a Lucent PHY.

The PHY chip integrates a 100BASE-T physical coding sub-layer (PCS) and a complete 10BASE-T module in a single chip.

The 100BASE-X portion of the PHY IC consists of the following functional blocks:

- Transmitter
- Receiver
- Clock generation module
- Clock recovery module

The 10BASE-T section of the PHY IC consists of the 10-Mbps transceiver module with filters.

The 100BASE-X and 10BASE-T sections share the following functional characteristics:

- PCS control
- IEEE 802.3u auto negotiation

The following sections provide brief descriptions of the following:

- Automatic negotiation
- Connectors

10.2.13.1 Automatic Negotiation

Automatic negotiation controls the cable when a connection is established to a network device. It detects the various modes that exist in the linked partner and advertises its own abilities to automatically configure the highest performance mode of inter-operation, namely, 10BASE-T, 100BASE-TX, or 100BASE-T4 in half- and full-duplex modes.

The Ethernet port supports automatic negotiation. At power up, an on-board transceiver advertises 100BASE-TX in half-duplex mode, which is configured by the automatic negotiation to the highest common denominator based on the linked partner.

10.2.13.2 External Cables

The RJ45 Ethernet port supports a Category 5, STP cable for the 100BASE-T, and a Category 3, 4, or 5 STP cable for the 10BASE-T operation.

Note – The maximum cable segment lengths for the 100BASE-TX and 10BASE-TX are 100 m (328 ft) and 1000 m (3282 ft), respectively.

10.2.14 FC-AL Subsystem

The Netra T4 system supports FC-AL (Fibre Channel-Arbitrated Loop) as the interface for internal and external hard drives. The physical medium is copper. Optical links are not supported.

The disk drives are connected to the loop through a hub chip. The hub supports two internal connectors and the external connector. Internal signal detect circuitry automatically detects the presence of a device at the external connector that enables or disables the external port. The individual ports can also be bypassed manually by a software probe and programming a GPIO register in the FC-AL controller.

TABLE 10-4 ISP2200A GPIO Bits

ISP2200A GPIO Bits	Drive Control	Input/Output Type	Default/Reset Value
<0>	External drive	Output	1*
<1>	Internal drive 1	Output	1*
<2>	Internal drive 2	Output	1*
<3>	External port detect	Input	0**
			**0 means bypass *1 means enable

The FC-AL host controller ASIC has a 64-bit, 66 MHz PCI (EPCI) interface. The controller contains the serializer / deserializer (SERDES) and the transceivers on-chip. The host controller implements the Fiber Channel protocol through a microcoded engine. The memory for the firmware is external and is implemented with synchronous 128 kByte SRAM. This memory also keeps the context data for outstanding I / Os.

The figure below shows the Netra T4 disk subsystem architecture:

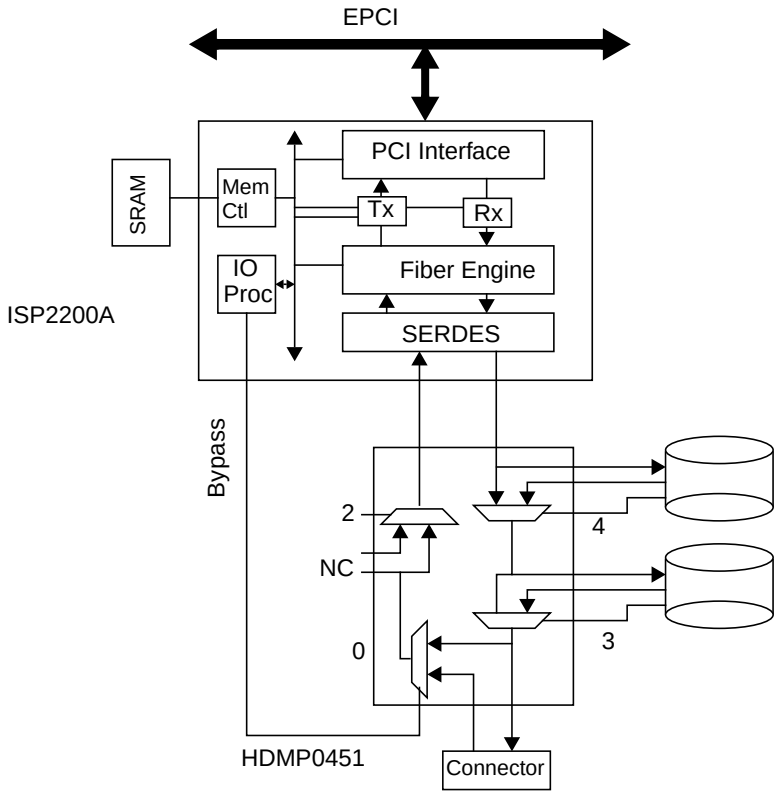


FIGURE 10-16 FC-AL Disk subsystem

10.2.15 SCSI

The system implements a small computer system interface (SCSI) for Ultra SCSI, 40 Mbps parallel interface bus. Ultra SCSI provides the following:

- Efficient peer-to-peer I/O bus devices
- Mechanical, electrical, and timing specification definition that support transfer rates of 20 Mbytes/s or 40 Mbytes/s (corresponding to the data path width of an 8-bit, or 16-bit bus, respectively)
- Peak bandwidth of 40 Mbytes/s (with implemented 16-bit bus width)

The internal SCSI bus is terminated at each end. One set of terminators is located close to the DVD-ROMOM drive connector on the DVD-ROM SCSI cable. A second set of terminators is located close to the internal SCSI connector. The following figure shows the SCSI bus configuration.

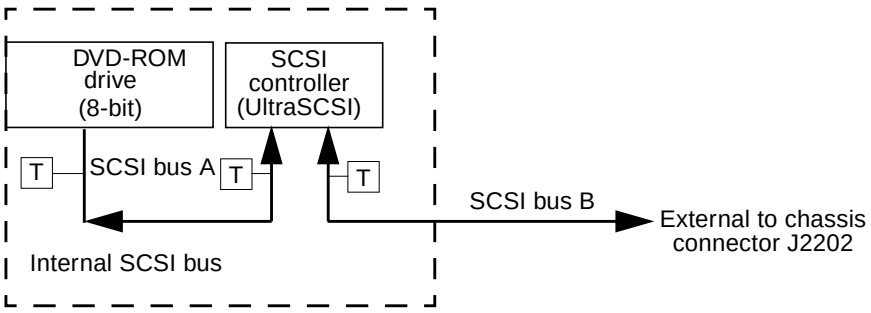


FIGURE 10-17 Configuration for the SCSI Bus

10.2.15.1 Host Adapter

The host adapter is a QLogic PCI-SCSI ASIC. The host adapter and all target devices comply with the Ultra SCSI single-ended drivers and receivers characteristics. The electrical characteristics of the output buffers include:

- V_{ol} (output low) equals 0VDC to 0.5VDC with I_{ol} at 48mA (signal asserted)
- V_{oh} (out high) equals 2.5VDC to 3.7VDC (signal negated)
- t_{rise} (rising slew rate) equals 520mV/ns maximum (0.7VDC to 2.3VDC)
- t_{fall} (falling slew rate) equals 520mV/ns maximum (2.3VDC to 0.7VDC)

The Ultra SCSI electrical characteristics for the host adapter and target device include:

- V_{il} (input low) equals 1.0VDC maximum (signal true)
- V_{ih} (input high) equals 1.9VDC minimum (signal false)
- I_{il} (input low current) equals +/- 20µA when V_i equals 0.5VDC
- I_{ih} (input high current) equals +/- 20 µA when V_i equals 2.7VDC
- Minimum input hysteresis equals 0.3VDC

10.2.15.2 Supported Target Devices

The SCSI subsystem supports a maximum of three internal devices, including the host adapter, DVD-ROM drive and DAT drive. The external SCSI bus supports up to 16 UltraSCSI devices.

10.2.15.3 External Cables

External Ultra SCSI-compliant SCSI cables have an impedance of 90 ohm (+/- 6 ohm) and are required for Ultra SCSI interface. The Sun implementation of Ultra SCSI requires that the total SCSI bus length be limited to no more than approximately 6 m (20 ft) with up to twelve Sun compensated devices.

Owing to the considerably short bus length, two Ultra SCSI-compliant external cables are supported, 800 mm (32 in.) and 2 m (6.6 ft).

Note – Consult your authorized Sun sales representative or service provider to order Ultra SCSI-compliant external cables.

There is also an external SCSI connector on the rear panel for legacy peripheral devices.

10.2.16 SuperI/O

The Netra T4 system uses a SuperI/O ASIC to interface to the parallel port. The SuperI/O ASIC also:

- Provides the TOD/ID SEEPROM
- Interfaces with the power supply

10.3 Power Supply

10.3.1 AC100 PSU

The 500 W autosensing AC power supply has a voltage range of 90 V_{rms} to 254 V_{rms} and a frequency range of 47 Hz to 63 Hz. The maximum input current is 9 A at 100 V.

The power supply output voltages are listed in TABLE 10-5. The power supply continues to regulate all outputs for 20 ms after AC power is removed.

TABLE 10-5 AC Power Supply Output Values

Output	Voltage (VDC)	Max Current (A)	Regulation Band (V)
1	3.3	38.0	3.23 to 3.43
2	5.0	48.0	4.85 to 5.25
3	12.0	10.0	11.40 to 12.60
4	–12.0	0.5	–12.60 to –11.40
5	5.0_Standby	1.25	4.75–5.25

10.3.2 DC100 PSU

The maximum continuous output power rating is 500 W for single or dual input supply. The maximum continuous rating per output is shown in TABLE 10-6.

TABLE 10-6 DC Power Supply Output Values

Output	Voltage (V)	Current (A)	Regulation Band (V)
1	3.3	38.0	3.23 to 3.43
2	5.0	48.0	4.85 to 5.25
3	12	10.0	11.40 to 12.60
4	–12	0.5	–12.60 to –11.65
5	5.0	1.5	4.75 to 5.25

10.3.3 Control Signals

All power supply control signals are at signal levels shown in TABLE 10-7.

TABLE 10-7 Power Supply Control Signal Levels

Parameter	Min	Max
V_{OH} (high-level output voltage)	3.4VDC	
V_{OL} (low-level output voltage)		0.4VDC
V_{IH} (high-level input voltage)	2.4VDC	
V_{IL} (low-level input voltage)		0.8VDC

10.4 Motherboard

FIGURE 10-18 shows a block diagram of the Netra T4 motherboard. TABLE 10-8 describes the functions of the connectors and jumpers.

Note – Unnumbered connectors in FIGURE 10-18 are not used by the Netra T4 system.

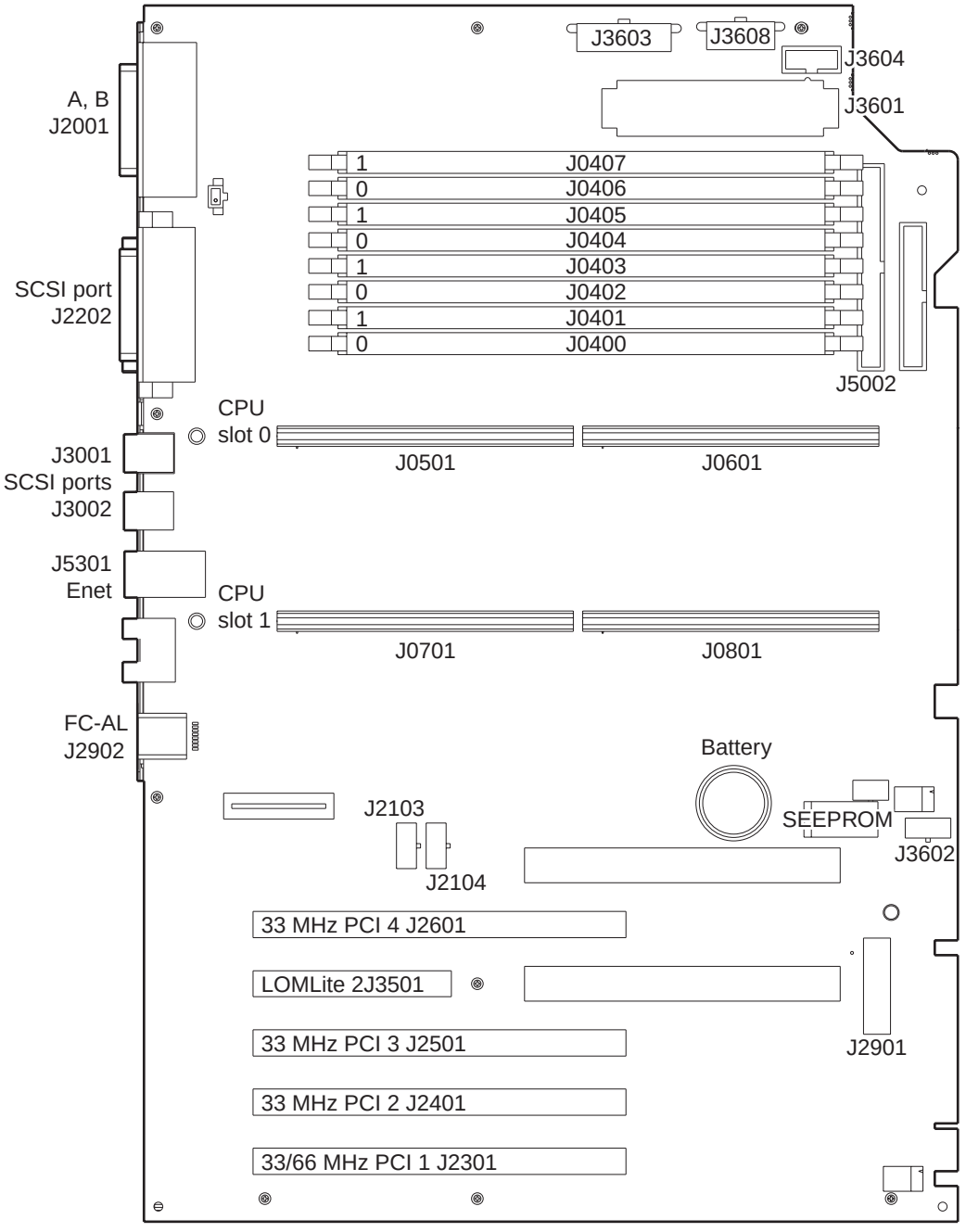


FIGURE 10-18 System Motherboard Block Diagram

Note – In FIGURE 10-18, unnumbered connectors are not used by the Netra T4 system

TABLE 10-8 Motherboard Component Functions

Designation	Function
J0100	DIMM
J0101	DIMM
J0202	DIMM
J0203	DIMM
J0304	DIMM
J0305	DIMM
J0406	DIMM
J0407	DIMM
J0501	CPU connector
J0601	CPU connector
J0701	CPU connector
J0801	CPU connector
J1801	Not used
J2001	Serial ports A, B rear panel connector
J2103	Jumper PROM R/W See Section 10.5, “Jumper Descriptions” on page 10-40
J2104	Jumper PROM Select See Section 10.5, “Jumper Descriptions” on page 10-40
J2202	SCSI, Parallel rear panel connector
J2301	66 MHz PCI 1 connector
J2401	33 MHz PCI 2 connector
J2501	33 MHz PCI 3 connector
J2601	33 MHz PCI 4 connector
J2901	FC-AL internal connector
J2902	FC-AL rear panel connector
J3001	USB rear panel connector
J3002	USB rear panel connector
J3202	Not used

TABLE 10-8 Motherboard Component Functions *(Continued)*

Designation	Function
J3203	Not used
J3302	Not used
J3303	Not used
J3501	Server RSC connector
J3601	Power supply connector
J3602	Combined cable connector
J3603	Power supply connector
J3604	Smart card reader connector
J3605	Not used
J3608	Peripheral power cable connector
J4301	Not used
J4401	Not used
J4501	Not used
J5002	SCSI connector
J5301	Ethernet rear panel connector

10.5 Jumper Descriptions

Jumper configurations can be changed from the default settings by setting jumper switches on the motherboard.

A jumper switch is *closed* (sometimes referred to as *shorted*) with the plastic cap inserted over two pins of the jumper. A jumper is *open* with the plastic cap inserted over one or no pin(s) of the jumper.

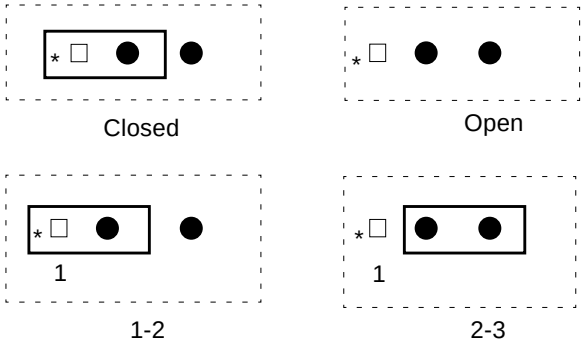


FIGURE 10-19 Selected Jumper Settings

Jumper descriptions include brief overviews of flash PROM jumpers and additional system board jumper and connector blocks.

Jumpers are identified on the system board by J designations. Jumper pins are located immediately adjacent to the J designator. Pin 1 is marked with an asterisk in any of the positions shown in the figure below.

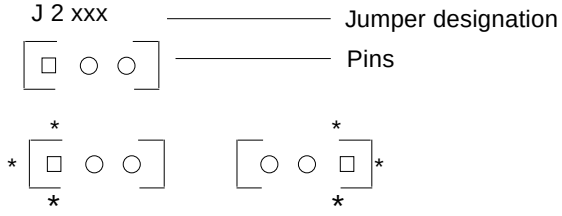


FIGURE 10-20 Identifying Jumper Pins

10.5.1 Flash PROM Jumpers

Flash PROM jumpers J2103 and J2104 are for reprogramming specific code blocks and remote programming of the flash PROM. The following figure shows the flash PROM jumper locations.

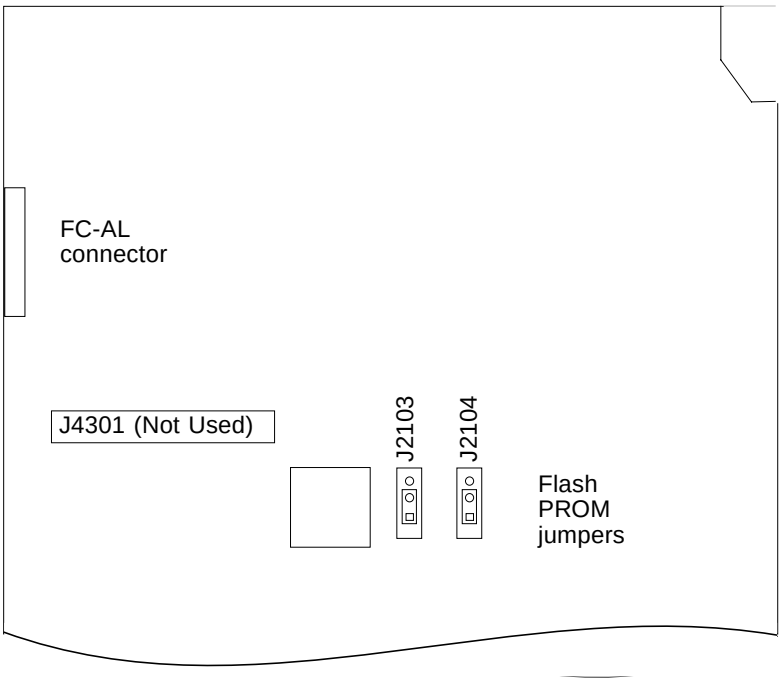


FIGURE 10-21 Flash PROM Jumper Locations

TABLE 10-9 Flash PROM Jumper Settings

Jumper	Pins 1 + 2 Select	Pins 2 +3 Select	Default Jumper on Pins	Signal Controlled
J2103	Write protect	Write enable	1 + 2	FLASH PROM PROG ENABLE
J2104	Select	No select	1 + 2	XOR LOGIC SET

CHAPTER **11**

External I/O Connectors

This chapter provides information about the external I/O connectors.

FIGURE 11-1 shows the locations of the Netra T4 system back panel connectors.

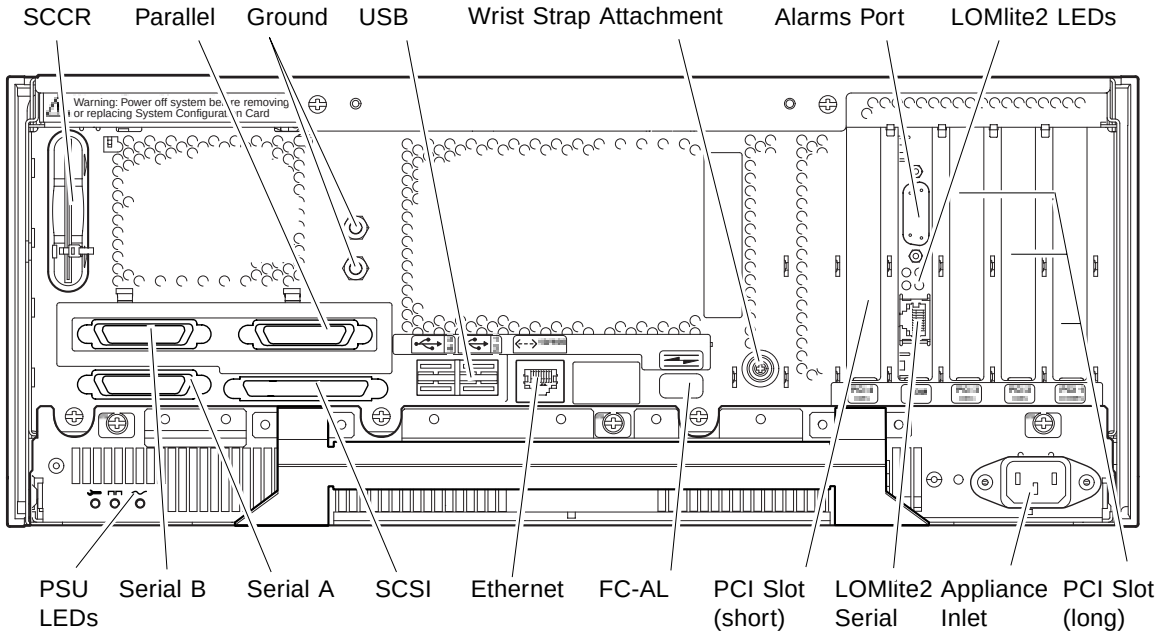


FIGURE 11-1 Back Panel Connectors (AC100 Shown)

11.1 Parallel Connector

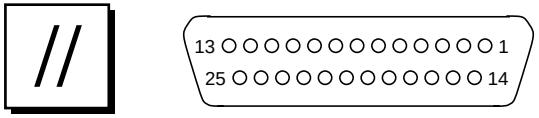


FIGURE 11-2 DB-25 Parallel Connector

TABLE 11-1 Parallel Connector Pinout

Pin	Signal Name	I/O	Service
1	DATA_STROBE_L		Data Strobe (active LOW)
2	DAT(0)		Data Bit 0
3	DAT(1)		Data Bit 1
4	DAT(2)		Data Bit 2
5	DAT(3)		Data Bit 3
6	DAT(4)		Data Bit 4
7	DAT(5)		Data Bit 5
8	DAT(6)		Data Bit 6
9	DAT(7)		Data Bit 7
10	ACK_L		Acknowledge (active LOW)
11	BSY		Busy (active HIGH)
12	PERROR		Paper End (active HIGH)
13	SELECT_L		Select (active LOW)
14	AFXN_L		Auto Line Feed (active LOW)
15	ERROR_L		Error (active LOW)
16	RESET_L		Initialize Printer (prime active LOW)
17	IN_L		Select Input (active LOW)
18	GND		Ground
19	GND		Ground
20	GND		Ground
21	GND		Ground

TABLE 11-1 Parallel Connector Pinout *(Continued)*

Pin	Signal Name	I/O	Service
22	GND		Ground
23	GND		Ground
24	GND		Ground
25	GND		Ground

11.2 Serial Connectors

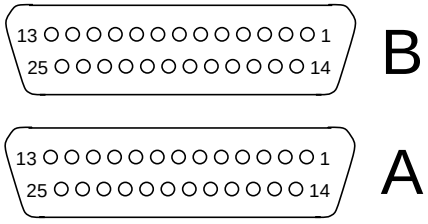


FIGURE 11-3 DB-25 Serial Connectors

TABLE 11-2 Serial Connector Pinout, RS423/RS232

Pin	Function	I/O	Signal Description
1			Not connected
2	TxD	O	Transmit Data
3	RxD	I	Receive Data
4	RTS	O	Ready To Send
5	CTS	I	Clear To Send
6	DSR	I	Data Set Ready
7	Gnd		Signal Ground
8	DCD	I	Data Carrier Detect
9–14			Not connected
15	TRxC	I	Transmit Clock
16			Not connected
17	RTxC	I	Receive Clock

TABLE 11-2 Serial Connector Pinout, RS423/RS232 *(Continued)*

Pin	Function	I/O	Signal Description
18–19			Not connected
20	DTR	O	Data Terminal Ready
21-23			Not connected
24	TxC	O	Transmit Clock
25			Not connected

Note: For information about serial port jumpers on the Netra T4 system main logic board, see the *Netra T4 System Reference Manual*.

11.3 SCSI Connector

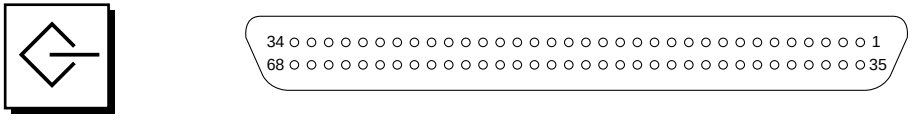


FIGURE 11-4 68-Pin SCSI Connector

TABLE 11-3 68-Pin SCSI Connector Pinout

Pin	Signal Name	Pin	Signal Name
1	GND	21	GND
2	GND	22	GND
3	GND	23	GND
4	GND	24	GND
5	GND	25	GND
6	GND	26	GND
7	GND	27	GND
8	GND	28	GND
9	GND	29	GND
10	GND	30	GND
11	GND	31	GND
12	GND	32	GND

TABLE 11-3 68-Pin SCSI Connector Pinout *(Continued)*

Pin	Signal Name	Pin	Signal Name
13	GND	33	GND
14	GND	34	GND
15	GND	35	–DB<12>
16	GND	36	–DB<13>
17	TERMPWR	37	–DB<14>
18	TERMPWR	38	–DB<15>
19	Not connected	39	–PAR<1>
20	GND	40	–DB<0>
41	–DB<1>	55	–ATN
42	–DB<2>	56	GND
43	–DB<3>	57	–BSY
44	–DB<4>	58	–ACK
45	–DB<5>	59	–RST
46	–DB<6>	60	–MSG
47	–DB<7>	61	–SEL
48	–PAR<0>	62	–CD
49	GND	63	–REQ
50	TERM.DIS	64	–IO
51	TERMPWR	65	–DB<8>
52	TERMPWR	66	–DB<9>
53	Reserved	67	–DB<10>
54	GND	68	–DB<11>

Note – All signals shown in TABLE 11-3 are active low.

11.3.1 SCSI Implementation

- SCSI-3 Fast-20 (UltraSCSI) parallel interface
- 16-bit SCSI bus
- 40Mbps data transfer rate
- Support for 16 SCSI addresses:
  - Target 0 to 6 and 8 to F for devices
  - Target 7 reserved for SCSI host adapter on main logic board
- Support for up to seven internal SCSI devices (including the host adapter):
  - Fast-20 SCSI disk drive target 0 (left-most drive slot)
  - Fast-20 SCSI disk drive target 1
  - Fast-20 SCSI disk drive target 2
  - Fast-20 SCSI disk drive target 3 (right-most drive slot)
  - Fast-10 SCSI removable media device target 4
  - Fast-10 SCSI removable media device target 6
- Support for external 8-bit and 16-bit SCSI devices via 68-pin SCSI connector mounted on an adapter board

11.3.2 SCSI Cabling and Configuration

The SCSI-3 Fast-20 (UltraSCSI) specification requires that the external SCSI bus length be limited to 3m (10ft) for less than five devices (internal and external), and 1.5m (5ft) for five to eight devices. When SCSI-3 and SCSI-2 devices are connected to the Netra T4 system SCSI bus, the system enables each device to operate at its respective data transfer rate. The last external SCSI device in a daisy-chain must be terminated internally (active termination) or with an external terminator according to Forced-Perfect Termination (FPT) technology.

11.3.2.1 SCSI Cabling Procedure

1. **Count the number of SCSI devices on the system SCSI bus. Be sure to count the host adapter as a SCSI device.**

2. **Determine the total SCSI bus length.**

TABLE 11-4 Determining SCSI Bus Length

SCSI Implementation	Bus Width	Data Transfer Rate, Mb/s	Number of Devices	SCSI Bus Length
SCSI-2, Fast	8 bits	10	1–8	6.0 m
SCSI-2, Fast / Wide	16 bits	20	1–8	6.0 m
SCSI-3 Parallel Interface, Fast-20 Wide (UltraSCSI) (WideUltra)	16 bits	40	1–4	3.0 m
SCSI-3 Parallel Interface, Fast-20 Wide (UltraSCSI) (WideUltra)	16 bits	40	5–8[1]	1.5 m

1. The maximum number of single-ended / differential SCSI devices is 16.

3. **Verify the cable type used to connect external SCSI devices. You must use Fast-20 SCSI cable(s).**

Ensure that the total SCSI cable length does not exceed the permissible total SCSI bus length.

11.3.2.2 SCSI-2 (Fast Wide SCSI) External Devices

If you connect SCSI-2 (Fast Wide SCSI, 20Mb data transfer rate) external devices to a Netra t 1400 / 1405 system, follow these cabling and configuration guidelines (as shown in FIGURE 11-5) to ensure proper device addressing and operation:

- If all external mass storage devices use 68-pin connectors, connect all non-Sun devices to the Netra T4 system first and follow them with Sun devices. Sun devices use auto-termination.
- If external mass storage devices consist of 68-pin Sun devices and 50-pin devices, connect the Sun 68-pin devices to the Netra T4 system first and terminate the daisy chain with the 50-pin device and its terminator.
- The total SCSI bus length for all external SCSI devices is 6.0m (19.7ft), including the internal cabling.

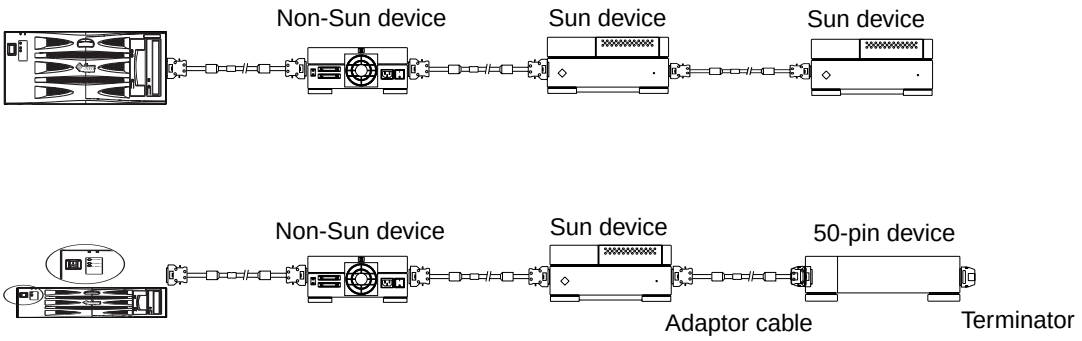


FIGURE 11-5 Connecting External Mass Storage Devices

11.4 Ethernet Connector

FIGURE 11-6 RJ45 TPE Socket

TABLE 11-5 TPE Connector Pinout

Pin	Description	Pin	Description
1	Transmit Data +	5	Common Mode Termination
2	Transmit Data –	6	Receive Data –
3	Receive Data +	7	Common Mode Termination
4	Common Mode Termination	8	Common Mode Termination

TPE Cable-Type Connectivity

The following types of twisted-pair Ethernet cable can be connected to the 8-pin TPE connector:

- For 10BASE-T applications, shielded twisted-pair (STP) cable:
  - Category 3 (STP-3, *voice* grade)
  - Category 4 (STP-4)
  - Category 5 (STP-5, *data* grade)
- For 100BASE-T applications, shielded twisted-pair category 5 (STP-5, *data* grade) cable.

TABLE 11-6 TPE STP-5 Cable Lengths

Cable Type	Application(s)	Max Length (Metric)	Max Length (Imperial)
Shielded twisted pair category 5 (STP-5, *data* grade)	10BASE-T	1000m	3281ft
Shielded twisted pair category 5 (STP-5, *data* grade)	100BASE-T	100m	328ft

11.5 FC-AL Connector

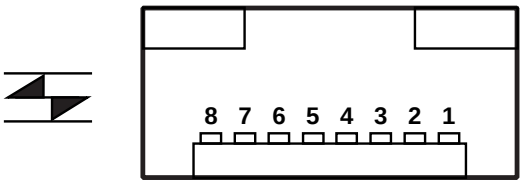


FIGURE 11-7 FC-AL Connector

TABLE 11-7 FC-AL Connector Pinout

Pin	Description	Pin	Description
1	Transmit Data TX_P	5	NC
2	GND	6	Receive Data TX_N
3	Transmit DataTX_N	7	GND
4	NC	8	Receive Data TX_P

11.6 USB Connectors

Four USB connectors (two twin Series A) are located between the SCSI port and FC-AL port.

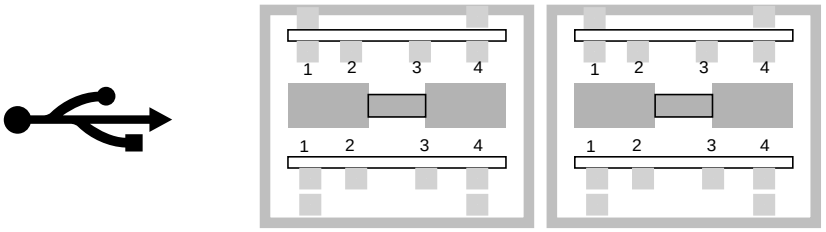


FIGURE 11-8 Twin Series A USB Connector

TABLE 11-8 USB Connector Pinout

Pin	Description	Pin	Description
A1	USB0_VCC +5VDC	C1	USB2_VCC +5VDC
A2	Port0Data -	C2	Port2Data -
A3	Port0Data +	C3	Port2Data +
A4	GND	C4	GND
B1	USB1_VCC +5VDC	D1	USB3_VCC +5VDC
B2	Port1Data -	D2	Port3Data -
B3	Port1Data +	D3	Port3Data +
B4	GND	D4	GND

11.7 Alarms Ports

The alarms service port connector (male DB-15) and LOM port connector (RJ45) are located on the alarms card. TABLE 11-9 lists the pinouts for the alarms service port connector.

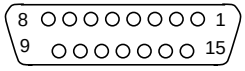


FIGURE 11-9 DB-15 (Male) Alarms Service Port Connector

TABLE 11-9 Alarms Service Port Connector Pinout

Pin	Signal Name	Pin	Signal Name
1	Not connected	9	ALARM1_NC
2	Not connected	10	ALARM1_COM
3	Not connected	11	ALARM2_NO
4	Not connected	12	ALARM2_NC
5	SYSTEM_NO	13	ALARM2_COM
6	SYSTEM_NC	14	Not connected
7	SYSTEM_COM	15	Not connected
8	ALARM1_NO	Shell	CHGND

The remote Lights Out Management serial port is located below the alarms port. The connector is a shielded RJ45 and TABLE 11-10 lists the connector pinouts.

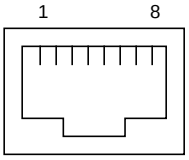


FIGURE 11-10 RJ45 Lights Out Management Serial Connector

TABLE 11-10 Lights Out Management Serial Connector Pinout

Pin	Signal Name	Pin	Signal Name
1	RTS	5	REF (0V)
2	DTR	6	RXD
3	TXD	7	DSR
4	REF (0V)	8	CTS
Shell	CHGND		

11.8 System Configuration Card Reader

The slot for system configuration card is located at the extreme left hand side of the rear panel (see FIGURE 11-1).

CHAPTER 12

Modem Setup

Any modem compatible with CCITT V.24 can be connected to the Netra T4 serial ports. Modems can be set up to function in one of three ways:

- Dial out only
- Dial in only
- Bidirectional calls.

12.1 To Set Up the Modem

To set up your modem:

1. **Become root and type `admintool`.**

```
% su
Password:
# admintool
```

2. **Click on Serial Port Manager.**
3. **Select Port a or Port b for your modem connection.**
4. **Click on Edit.**

   The Serial Port Manager: Modify Service window is displayed.

5. **Choose the Expert level of detail.**

6. **From the Use Template menu, choose one of the following:**

   a. **Modem – Dial-Out only**

   b. **Modem – Dial-In only**

   c. **Modem – Bidirectional**

7. **Click on Apply.**

8. **Set your modem auto-answer switch to one of the following:**
   - Off – Dial-Out Only
   - On – Dial-In Only
   - On – Bidirectional

12.2 Serial Port Speed Change

To change the speed of a serial port, you must edit the `/etc/remote` file as follows:

1. **Become super user, and type `cd /etc`.**

```
% su
Password:
# cd /etc
```

2. **Type `vi remote`.**

3. **Type `tip` *speed device-name*.**
   Typical speeds are 9600, 19200 to 38400 bps.
   The device name is the serial port name, for example,
   `/dev/tty[a,b]` or `/dev/term/[a,b]`.

4. **Press `<Esc>` and type `:wq` to save your file change(s) and to exit from the `vi` text editor.**

12.3 Recommendations

For a modem-to-host (system) connection, use an RS423/RS232 straight-through cable with DB-25 male connectors at both ends.

APPENDIX **A**

Illustrated Parts List

This appendix lists the authorized replaceable parts for the Netra T4 system unit. FIGURE A-1 is an exploded view of the system unit with numerical references that correlate to the replaceable components listed in TABLE A-1 and TABLE A-2. A brief description of each listed component is also given and, where appropriate, a reference to the section in this manual containing the replacement procedure.

The part numbers listed in TABLE A-1 and TABLE A-2 were correct at the time of publication of this manual, but are subject to change without notice. Consult your authorized Sun sales representative or service provider to confirm a part number before ordering the replacement part.

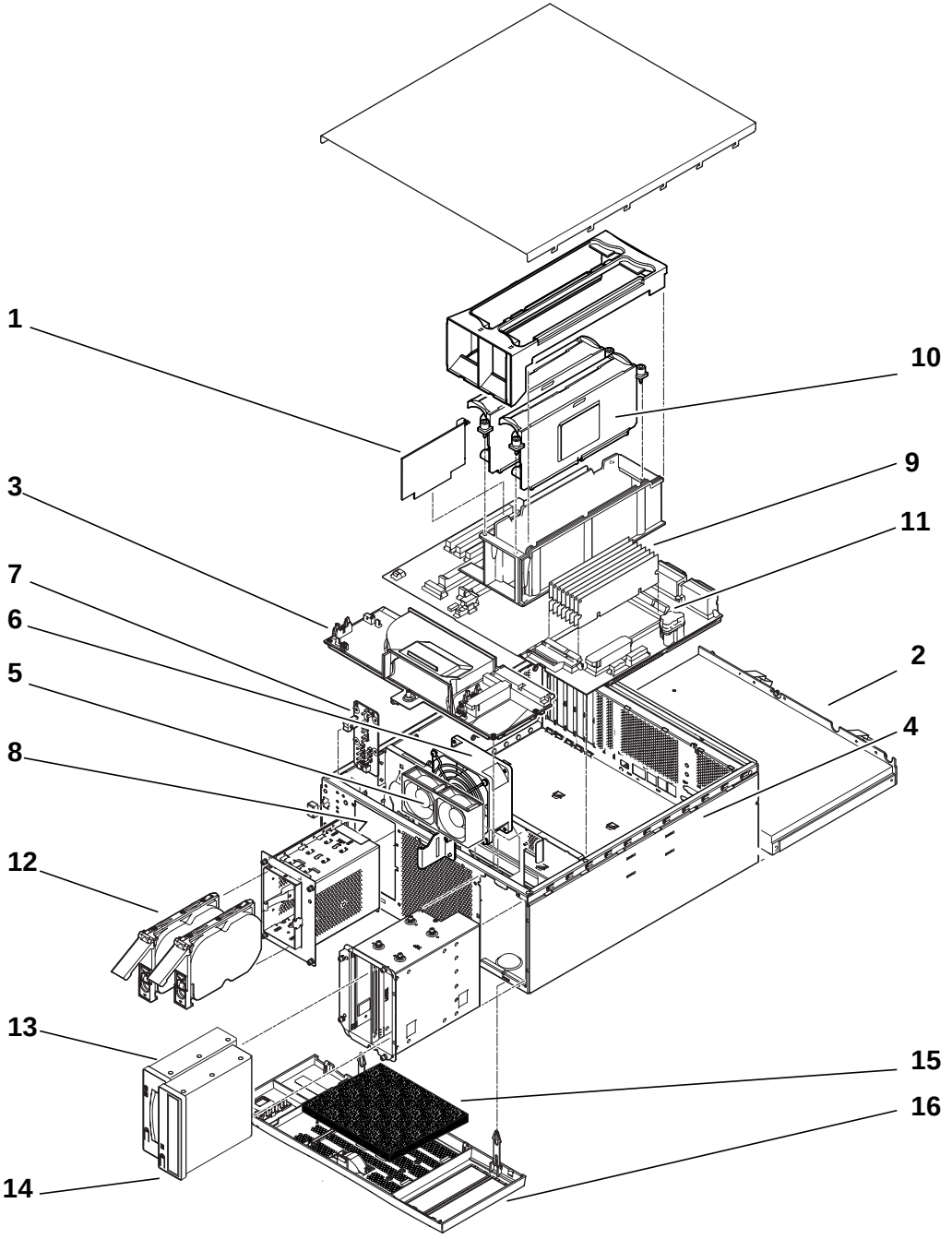


FIGURE A-1 Exploded View of the Netra T4 System Unit

TABLE A-1 Netra T4 Field Replaceable Units

Ref	FRU Number	Description
1	#501-5893	LOMlite2 Module
2	#300-1496	AC PSU (AC100)
3	#540-4795	Power Distribution Board (PDB)
4	#501-5965	System Configuration Card Reader (SCCR)
5	#540-5023	Fan Assembly, 80 mm (PSU)
6	#370-4360	Fan Assembly, 127 mm (CPU)
7	#501-5915	LED Card and Switch Assembly
8	#540-4794	FC-AL Backplane
9	#501-5938	Motherboard
10	#501-5675[1]	Processor, 750 MHz
11	#501-4489[1]	Memory Module, 128 MByte
11	#501-5401[1]	Memory Module, 256 MByte
11	#501-5030[1]	Memory Module, 512 MByte
11	#501-5031[1]	Memory Module, 1 GByte
12	#540-4525[1]	FC-AL Disk Drive, 36 GByte
13	#390-0028[1]	DDS-4 DAT Drive
14	#390-0025[1]	DVD Drive
Not shown	#501-5656[1]	PCI Card, 10/100BaseT Fast/Wide UltraSCSI
Not shown	#501-5019[1]	PCI Card, 10BaseT FastEthernet
Not shown	#375-0006[1]	PCI Card, Dual Differential SCSI
Not shown	#370-2728[1]	PCI Card, HSI/P 2.0
Not shown	#375-0100[1]	PCI Card, SAI/P 3.0
Not shown	#501-3028[1]	PCI Card, ATM-155MMF P/4.0
Not shown	#501-3027[1]	PCI Card, ATM-155-UTP P/4.0
Not shown	#501-5406[1]	PCI Card, Quad Fast Ethernet II
Not shown	#501-5373[1]	PCI Card, Gigabit Ethernet P/2.0
Not shown	#501-5901[1]	PCI Card, Gigabit Ethernet MMF P/3.0
Not shown	#501-5902[1]	PCI Card, Gigabit Ethernet UTP P/3.0

TABLE A-1 Netra T4 Field Replaceable Units *(Continued)*

Ref	FRU Number	Description
Not shown	#501-5426[1]	PCI Card, Combined FC-AL and Gigabit Ethernet
Not shown	#375-0130[1]	PCI Card, SSL Crypto Accelerator
Not shown	#375-3019[1]	PCI Card, Single FC Network Adaptor
Not shown	#370-3868[1]	PCI Card, Cluster SCI PCI-64 Adaptor
Not shown	#375-0078[1]	PCI Card, H/W RAID Controller
Not shown	#375-0005[1]	PCI Card, Dual Channel SE UltraSCSI
Not shown	#540-4372[1]	Redundant FC 8-Port Switch
Not shown	#560-2631	Cable Kit, Power
Not Shown	#560-2632	Cable Kit, Data
Not Shown	#530-3032	Power Cable

1. Also an optional component

TABLE A-2 Netra T4 Optional Components

Ref	Part Number	Description
10	X6990A	Processor, 750MHz
11	X7050A	512MByte Memory Expansion 4 x 128MByte DIMMs
11	X7053A	1GByte Memory Expansion 4 x 256MByte DIMMs
11	X7051A	2GByte Memory Expansion 4 x 512MByte DIMMS
11	X7052A	4GByte Memory Expansion 4 x 1GByte DIMMS
12	X6724A	36GByte FC-AL Disk Drive
13	X6295A	DDS-4 DAT Drive
14	X6168A	DVD-R Drive (10x)
Not shown	X1032A	PCI Card, 10/100BaseT Fast/Wide UltraSCSI
Not shown	X1033A	PCI Card, 10BaseT FastEthernet
Not shown	X6541A	PCI Card, Dual Differential SCSI
Not shown	X1155A	PCI Card, HSI/P 2.0
Not shown	X2156A	PCI Card, SAI/P 3.0
Not shown	X1157A	PCI Card, ATM-155MMF P/4.0
Not shown	X1158A	PCI Card, ATM-155UTP P/4.0
Not shown	X1034A	PCI Card, Quad Fast Ethernet

TABLE A-2 Netra T4 Optional Components *(Continued)*

Ref	Part Number	Description
Not shown	X1141A	PCI Card, Gigabit Ethernet P/2.0
Not shown	X1150A	PCI Card, Gigabit Ethernet UTP P/3.0
Not shown	X1151A	PCI Card, Gigabit Ethernet MMF P/3.0
Not shown	X6799A	PCI Card, Single FC Network Adaptor
Not shown	X1133A	PCI Card, SSL Crypto Accelerator
Not shown	X2069A	PCI Card, Combined FC-AL and GBE
Not shown	X1074A	PCI Card, Cluster SCI PCI-64 Adaptor
Not shown	X6542A	PCI Card, H/W RAID Controller
Not shown	X6540A	PCI Card, Dual Channel SE UltraSCSI
Not shown	X6746A	Redundant FC 8-Port Switch
15	X7006A	Filter Pack (10)
16	X7007A	Front Bezel

APPENDIX **B**

Product Specification

This appendix defines the physical, electrical and environmental requirements for installing the Netra T4 AC100 system.

The appendix contains the following sections:

- Section B.1, “Physical Specification” on page B-1
- Section B.2, “Electrical Specification” on page B-2
- Section B.3, “Environmental Specification” on page B-4

B.1 Physical Specification

B.1.1 Dimensions

Dimension include the front fascia and PSU handle.

- Width: 445.2 mm (17.53 in.)
- Depth: 508.1 mm (20.00 in.)
- Height: 176.6 mm (6.95 in.)—4RU

B.1.2 Mounting Flanges

- 19-inch
- 23-inch
- 24-inch
- 600-mm
- Slide adaptor

B.2 Electrical Specification

B.2.1 Netra T4 AC100 System

B.2.1.1 Operating Voltage and Frequency

TABLE B-1 AC Power Supply Input Requirements

	Minimum	Maximum
Voltage	90 V_{rms}	264 V_{rms}
Frequency	47 Hz	63 Hz

B.2.1.2 Current

Inrush

The maximum inrush current is 25 A_{peak} upon start up or restart after power has been removed for 60 s or longer. Circuit breakers must not be tripped by an inrush current of 25 A lasting 200 ms.

Operating

The maximum normal input line current is less than 7.2 A_{rms} at 100 VAC under standard test conditions.

Power Off Mode

The maximum input power of the system in power off or remote off state is less than 30 VA.

B.2.1.3 Overcurrent Protection

The AC outlet socket should be protected by a 15 A double-pole double-throw circuit breaker.

B.2.2 Netra T4 DC100 System

B.2.2.1 DC Input

TABLE 12-1 DC Power Supply Input Requirements

Electrical Element	Requirement
Voltage[1]	-48 VDC / -60 VDC
Max. operating current	12 A @ -48 VDC / 10 A @ -60 VDC
Max. inrush current	30 A @ -48 VDC / 24 A @ -60 VDC

1. The DC power supply range is -40 VDC to -75 VDC.

B.2.2.2 Source Site Requirements

The DC source must be:

- –48 VDC or –60 VDC nominal centralized DC power system
- Electrically isolated from any AC power source
- Reliably connected to earth (that is, the battery room positive bus is connected to the grounding electrode)
- Rated for a minimum of 20 A per feed pair

Note – The Netra T4 DC100 system must be installed in a *restricted access location*. The IEC, EN and UL 60950 define a restricted access location as an area intended for qualified or trained personnel only and having access controlled by a locking mechanism, such as a key lock or an access card system.

B.2.2.3 Overcurrent Protection Requirements

- Overcurrent protection devices must be provided as part of each host equipment rack.
- Two 20 A single-pole, fast trip, DC-rated circuit breakers (one per ungrounded supply conductor) must be located in the negative supply conductor between the DC power source and the Netra T4 DC100 system.
- Circuit breakers must not trip when presented with inrush current of 20 A lasting 250 ms.

B.3 Environmental Specification

This section defines the principal operating requirements and limitations.

B.3.1 Operating and Storage

Normal Ambient Temperature

Operating	5˚C to 45˚C
Storage	–40˚C to 70˚C

Normal Ambient Humidity

Operating	5% to 85% (non-condensing) subject to a maximum absolute humidity of $0.024 kg_{water} / kg_{dry\ air}$ (5 to 90% for a maximum of 96 consequtive hours)
Storage	10% to 95% subject to a maximum absolute humidity of $0.024 kg_{water} / kg_{dry\ air}$

Temperature Variation

Operating	30˚C / hr maximum
Storage	30˚C / hr maximum

Altitude

Operating	0 to +3000 m
Storage	0 to +12000 m

B.3.2 Acoustic Noise

Less than 6.0 Bels in tests performed in accordance with ISO 9295:1988, International Standard on Acoustics—Measurement of high-frequency Noise Emitted by Computer and Business Equipment.

B.3.3 Earthquake

The system conforms to the NEBS requirements for earthquake zone 4.

B.3.4 Electro-Magnetic Compatibility

Immunity	Conforms to GR-1089-CORE and EN55024-1
Emissions	Conforms to GR-1089-CORE and EN55022 Class A and FCC-A

APPENDIX **C**

Tool Requirements

This appendix lists the tools you will require to service the Netra T4 system:

- Phillips No. 1 screwdriver, 10cm (4in.)
- Phillips No. 2 screwdriver, 15cm (6in.)
- Phillips No. 2 screwdriver, stubby
- 6mm (0.25in.) flat blade screwdriver, 10cm (4in.)
- Antistatic wrist strap
- Antistatic mat
- Long-nose pliers
- Digital voltage meter (DVM)
- Torque tool (calibrated to 5lbf-in., 3mm square drive)[1]

Place components sensitive to electrostatic discharge (ESD), such as system boards, disk drives and memory modules on an antistatic mat.

1. Located inside the system , at the front of the chassis on the left-hand side panel.

APPENDIX **D**

Motherboard Connectors

This sppendix describes the system motherboard connector signals and pin assignments.

The appendix contains the following sections:

- Section D.1, “SCCR Connector” on page D-1
- Section D.2, “Internal SCSI Connector” on page D-3
- Section D.3, “Internal FC-AL Connector” on page D-4
- Section D.4, “Power Connectors” on page D-5

D.1 SCCR Connector

The SCCR connector J3604 is located on the motherboard.

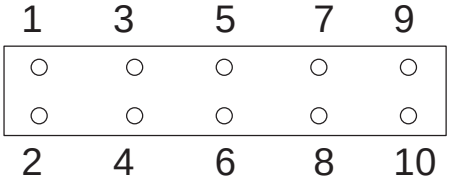
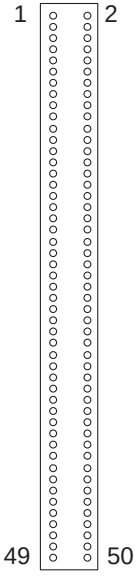


FIGURE D-1 Smart Card Reader Connector, J3604, Pin Assignments

TABLE D-1 SCCR, J3604, Pin Assignments

Pin	Signal Name	Description
1	+12 VDC	+12VDC power
2	GND	Ground
3	GND	Ground
4	I2C_SCL	I2C bus clock
5	+5 VDC	+5 VDC power
6	I2C_SDA	I2C bus data
7	GND	Ground
8	GND	Ground
9	Int_L	
10	NC	No connection

D.2 Internal SCSI Connector



Internal SCSI Connector, J5002

TABLE D-2 Internal SCSI Connector, J5002

Pin	Signal Name
1-19, 20-22, 24, 29-31, 33-35, 37, 39, 41, 43, 45, 47, 49	GND
2, 4, 6, 8, 10, 12, 14, 16	SCSI data bus
18	SCSI_A_PAR<0>
26	Termpowr_A
32	SCSI_A_ATN_L
36	SCSI_A_BSY_L
38	SCSI_A_ACK_L
40	SCSI_A_RESET_L

TABLE D-2 Internal SCSI Connector, J5002 *(Continued)*

Pin	Signal Name
42	SCSI_A_MSG_L
44	SCSI_A_SEL_L
46	SCSI_A_CD_L
48	SCSI_A_REQ_L
50	SCSI_A_IO_L

D.3 Internal FC-AL Connector

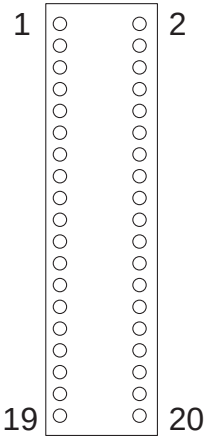


FIGURE D-2 Internal FC-AL Connector, J2901

TABLE D-3 Internal FC-AL Connector, J2901

Pin	Signal Name
1	Dr1_PB1_F_1
2	DR2PB2_F_1
3, 4, 7, 8, 11, 12, 15, 16, 19, 20	GND

TABLE D-3 Internal FC-AL Connector, J2901 *(Continued)*

Pin	Signal Name
5	T_DR2_PORT2IN_P
6	T_DR2_PORT2IN_N
9	DR2_PORT2OUT_P
10	DR2_PORT2OUT_N
13	T_DR1_PORT1IN_P
14	T_DR1_PORT1IN_N
17	DR1_PORT1OUT_P
18	DR1_PORT1OUT_N

D.4 Power Connectors

The motherboard has seven power connectors. The following table lists these power connectors, the connector use, and the supporting figure and table. xx identifies the motherboard connector location.

TABLE D-4 Power Connectors

Connector	Use	Supporting Figure	Supporting Table
J3603	Power from power supply	FIGURE D-3	TABLE D-5
J3601	Power from power supply	FIGURE D-4	TABLE D-6
J3303	Power to CPU fan		
J3602	Power to combined cable assembly		
J3608	Power to peripheral power cable assembly		

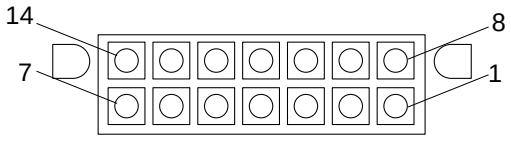


FIGURE D-3 Power Supply Connector J3603

TABLE D-5 Power Supply Connector J3603 Pin Description

Pin	Signal	Description
1	POWERON_L	Power on
2	-12 VDC	-12 VDC
3	+5 VDC Return (SENSE)	+5 VDC Return
4	+3.3 VDC Return (SENSE)	+3.3 VDC Return
5	RETURN	Return
6	RETURN	Return
7	Spare	Spare
8	POWER_OK	Power OK
9	PS_FAN	Fan power
10	+5 VDC (SENSE)	+5 VDC (Sense)
11	+3.3 VDC (SENSE)	+3.3 VDC (Sense)
12	+12 VDC	+12 VDC
13	+12 VDC	+12 VDC
14	+5 VDC_STBY	+5 VDC standby

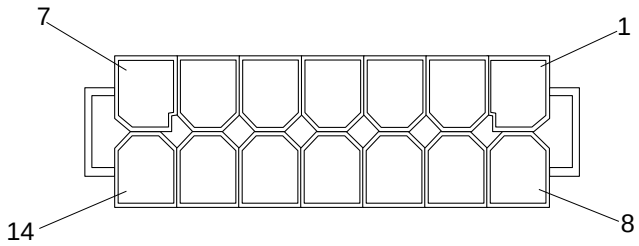


FIGURE D-4 Power Supply Connector J3601

TABLE D-6 Power Supply Connector J3601 Pin Description

Pin	Signal	Description
1	+3.3VDC	+3.3VDC
2	+3.3VDC	+3.3VDC
3	+3.3VDC	+3.3VDC
4	+3.3VDC	+3.3VDC
5	+5VDC	+5VDC
6	+5VDC	+5VDC
7	+5VDC	+5VDC
8	RETURN +3.3VDC	+3.3VDC Return
9	RETURN +3.3VDC	+3.3VDC Return
10	RETURN +3.3VDC	+3.3VDC Return
11	RETURN +3.3VDC	+3.3VDC Return
12	RETURN +5VDC	+5VDC Return
13	RETURN +5VDC	+5VDC Return
14	RETURN +5VDC	+5VDC Return

APPENDIX **E**

Example POST Diagnostic Output

This appendix provides examples of the POST output to serial port A. If POST fails to complete, compare the last message output with the example. The next line in the example may help to identify the cause of the problem.

CODE EXAMPLE E-1 is a typical POST output for a system with two 750 MHz CPUs and 4 GByte of memory, and with the `diag-level` variable set to `max`.

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(1 of 17)*

```
@(#)OBP 4.2.3 2001/04/23 17:48 Sun Netra T4
Clearing TLBs Done
Power-On Reset
Executing Power On SelfTest
{0}
{0}@(#)POST, v4.1.7  01/22/2001 06:55 PM
           {1}Transfered from OBP or Unknown source of reset
{0}PLL reset
{0}* Configure I2C controller 0
{0}* Configure I2C controller 1
{0}* I2C Controller Loopback Test
{0}* Read JTag IDs of all ASICs
{0} BBCJTag ID: 1483203b
{0} SCSIJTag ID: 15060045
{0} I chipJTag ID: d1e203b
{0} RIOJTag ID: 13e5d03b
{0} SchizoJTag ID: 1824c06d
{0} CPMSJTag ID: 1142903b
{0} CPMSJTag ID: 1142903b
{0} CPMSJTag ID: 1142903b
{0} CPMSJTag ID: 1142903b
{0} CPMSJTag ID: 1142903b
{0} CPMSJTag ID: 1142903b
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(2 of 17)*

```
{0}* Read JTag ID of FCAL
{0} FC-ALJTag ID: 1000a12f
{0}* Probing Seeprom on DIMMs and CPU modules
{0}CPU0 Sensor package temperature 44 oC
{0}CPU1 Sensor package temperature 44 oC
{0}WARNING: Temperature sensor on UPA0 missing
{0}WARNING: Temperature sensor on UPA1 missing
{0}WARNING: Smart card reader missing
{0}* Read parameters from seeproms
{0}        Size/bank(MB)Number of banks
{0}DIMM 0:2562
{0}DIMM 1:2562
{0}DIMM 2:2562
{0}DIMM 3:2562
{0}DIMM 4:2562
{0}DIMM 5:2562
{0}DIMM 6:2562
{0}DIMM 7:2562
{0}Bank 0 is  present, size = 00000000.40000000
{0}Bank 1 is  present, size = 00000000.40000000
{0}Bank 2 is  present, size = 00000000.40000000
{0}Bank 3 is  present, size = 00000000.40000000
{0}* Setup CPUs and system frequency
{0}CPU 0 ratio: 5
{0}CPU 1 ratio: 5
{0}System frequency: 150 MHz
{0}* Load PLL and reset
           {1}PLL reset
{0}PLL reset
           {1}* SoftInt & Interrupt
{0}* Configure I2C controller 0
           {1}Test walking 1 through softint register
{0}* Configure I2C controller 1
           {1}Test walking 0 through softint register
{0}* SoftInt & Interrupt
           {1}Verify interrupt occurs for each level
{0}Test walking 1 through softint register
           {1}Verify interrupt occurs at the right PIL
{0}Test walking 0 through softint register
           {1}* Tick & Tick-Compare Reg
{0}Verify interrupt occurs for each level
           {1}Walk 1/0 TICK Compare register
{0}Verify interrupt occurs at the right PIL
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(3 of 17)*

```
            {1}Verify TICK register is counting
{0}* Tick & Tick-Compare Reg
            {1}Verify TICK register Overflow
{0}Walk 1/0 TICK Compare register
            {1}Verify TICK Interrupt
{0}Verify TICK register is counting
{0}Verify TICK register Overflow
{0}Verify TICK Interrupt
            {1}* Stick & Stick-Compare Reg
            {1}Walk 1/0 STICK Compare register
            {1}Verify STICK register is counting
{0}* Stick & Stick-Compare Reg
            {1}Verify STICK register Overflow
{0}Walk 1/0 STICK Compare register
            {1}Verify STICK Interrupt
{0}Verify STICK register is counting
{0}Verify STICK register Overflow
{0}Verify STICK Interrupt
            {1}* Measure CPU Clock
{0}* Measure CPU Clock
{0}AFT pin is high
{0}Setup Memory Controller
{0}* IMMU Registers
            {1}* IMMU Registers
{0}Testing I-TSB
            {1}Testing I-TSB
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Test walking 0 through the register
            {1}Test walking 0 through the register
{0}Testing I-TLB Tag Access
            {1}Testing I-TLB Tag Access
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Test walking 0 through the register
            {1}Test walking 0 through the register
{0}* DMMU Registers
            {1}* DMMU Registers
{0}Testing Primary Context
            {1}Testing Primary Context
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Testing Secondary Context
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(4 of 17)*

```
            {1}Testing Secondary Context
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Testing D-TSB
            {1}Testing D-TSB
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Testing D-TLB Tag Access
            {1}Testing D-TLB Tag Access
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Testing Virtual Watchpoint
            {1}Testing Virtual Watchpoint
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Testing Physical Watchpoint
            {1}Testing Physical Watchpoint
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}* 4M DTLB RAM
            {1}* 4M DTLB RAM
{0}Test address up
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}Test data reliability
            {1}Test data reliability
{0}Test address line transitions
            {1}Test address line transitions
{0}* 8K DTLB RAM
            {1}* 8K DTLB RAM
{0}Test address up
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}Test data reliability
            {1}Test data reliability
{0}Test address line transitions
            {1}Test address line transitions
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(5 of 17)*

```
{0}* 4M DTLB TAG
{0}Test address up
{0}Test address down
           {1}* 4M DTLB TAG
{0}Test cell disturbance
           {1}Test address up
{0}Test data reliability
           {1}Test address down
{0}Test address line transitions
           {1}Test cell disturbance
{0}* 8K DTLB TAG
           {1}Test data reliability
{0}Test address up
           {1}Test address line transitions
           {1}* 8K DTLB TAG
{0}Test address down
           {1}Test address up
{0}Test address line transitions
           {1}Test address down
{0}* 4M ITLB RAM
{0}Test address up
{0}Test address down
           {1}Test address line transitions
{0}Test cell disturbance
{0}Test data reliability
           {1}* 4M ITLB RAM
{0}Test address line transitions
           {1}Test address up
{0}* 8K ITLB RAM
           {1}Test address down
{0}Test address up
           {1}Test cell disturbance
{0}Test address down
           {1}Test data reliability
{0}Test cell disturbance
           {1}Test address line transitions
           {1}* 8K ITLB RAM
{0}Test data reliability
           {1}Test address up
           {1}Test address down
           {1}Test cell disturbance
{0}Test address line transitions
           {1}Test data reliability
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(6 of 17)*

```
{0}* 4M ITLB TAG
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
           {1}Test address line transitions
{0}* 8K ITLB TAG
           {1}* 4M ITLB TAG
{0}Test address up
           {1}Test address up
{0}Test address down
           {1}Test address down
{0}Test address line transitions
           {1}Test cell disturbance
{0}* IMMU Init
           {1}Test data reliability
{0}* DMMU Init
           {1}Test address line transitions
{0}Mapping done. MMU enabled
           {1}* 8K ITLB TAG
{0}* Memory address selection Initial area
           {1}Test address up
           {1}Test address down
           {1}Test address line transitions
           {1}* IMMU Init
           {1}* DMMU Init
           {1}Mapping done. MMU enabled
           {1}* Memory address selection Initial area
{0}* Memory marching Initial area
           {1}* Memory marching Initial area
{0}* E-Cache Global Vars Init
{0}* E-Cache Quick Verification
           {1}* E-Cache Global Vars Init
           {1}* E-Cache Quick Verification
{0}* Ecache TAGS
{0}Test address up
           {1}* Ecache TAGS
           {1}Test address up
{0}Test address down
           {1}Test address down
{0}Test cell disturbance
           {1}Test cell disturbance
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(7 of 17)*

```
{0}Test data reliability
           {1}Test data reliability
{0}Test address line transitions
           {1}Test address line transitions
{0}* Ecache Address Line
           {1}* Ecache Address Line
{0}* Partial Ecache Init
           {1}* Partial Ecache Init
{0}* BBC E-Star Registers
           {1}* I-Cache RAM
{0}* I-Cache RAM
           {1}Test address up
{0}Test address up
           {1}Test address down
{0}Test address down
           {1}Test cell disturbance
{0}Test cell disturbance
           {1}Test data reliability
{0}Test data reliability
           {1}Test address line transitions
{0}Test address line transitions
           {1}* I-Cache TAGS
           {1}Testing I-Cache Tag
{0}* I-Cache TAGS
           {1}Test address up
{0}Testing I-Cache Tag
{0}Test address up
           {1}Test address down
{0}Test address down
           {1}Test cell disturbance
{0}Test cell disturbance
           {1}Test data reliability
{0}Test data reliability
           {1}Test address line transitions
{0}Test address line transitions
           {1}Testing I-Cache Micro Tag
           {1}Test address up
{0}Testing I-Cache Micro Tag
{0}Test address up
           {1}Test address down
{0}Test address down
           {1}Test cell disturbance
{0}Test cell disturbance
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(8 of 17)*

```
            {1}Test data reliability
{0}Test data reliability
            {1}Test address line transitions
{0}Test address line transitions
            {1}* I-Cache Snoop Tags
            {1}Test address up
{0}* I-Cache Snoop Tags
{0}Test address up
            {1}Test address down
{0}Test address down
            {1}Test cell disturbance
{0}Test cell disturbance
            {1}Test data reliability
{0}Test data reliability
            {1}Test address line transitions
{0}Test address line transitions
            {1}* I-Cache Init
{0}* I-Cache Init
            {1}* D-Cache RAM
            {1}Test address up
{0}* D-Cache RAM
{0}Test address up
            {1}Test address down
{0}Test address down
            {1}Test cell disturbance
{0}Test cell disturbance
            {1}Test data reliability
{0}Test data reliability
            {1}Test address line transitions
{0}Test address line transitions
            {1}* D-Cache TAGS
            {1}Test address up
{0}* D-Cache TAGS
{0}Test address up
            {1}Test address down
{0}Test address down
            {1}Test cell disturbance
{0}Test cell disturbance
            {1}Test data reliability
{0}Test data reliability
            {1}Test address line transitions
{0}Test address line transitions
            {1}* D-Cache MicroTags
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(9 of 17)*

```
            {1}Test address up
{0}* D-Cache MicroTags
{0}Test address up
            {1}Test address down
{0}Test address down
            {1}Test cell disturbance
{0}Test cell disturbance
            {1}Test data reliability
{0}Test data reliability
            {1}Test address line transitions
{0}Test address line transitions
            {1}* D-Cache SnoopTags
            {1}Test address up
{0}* D-Cache SnoopTags
{0}Test address up
            {1}Test address down
{0}Test address down
            {1}Test cell disturbance
{0}Test cell disturbance
            {1}Test data reliability
{0}Test data reliability
            {1}Test address line transitions
{0}Test address line transitions
            {1}* D-Cache Init
{0}* D-Cache Init
            {1}* W-Cache RAM
            {1}Test address up
{0}* W-Cache RAM
{0}Test address up
            {1}Test address down
{0}Test address down
            {1}Test cell disturbance
{0}Test cell disturbance
            {1}Test data reliability
{0}Test data reliability
            {1}Test address line transitions
{0}Test address line transitions
            {1}* W-Cache TAGS
            {1}Test address up
{0}* W-Cache TAGS
            {1}Test address down
{0}Test address up
            {1}Test cell disturbance
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(10 of 17)*

```
{0}Test address down
           {1}Test data reliability
{0}Test cell disturbance
{0}Test data reliability
           {1}Test address line transitions
{0}Test address line transitions
           {1}* W-Cache SnoopTAGS
{0}* W-Cache SnoopTAGS
           {1}Test address up
{0}Test address up
           {1}Test address down
{0}Test address down
           {1}Test cell disturbance
{0}Test cell disturbance
           {1}Test data reliability
{0}Test data reliability
           {1}Test address line transitions
{0}Test address line transitions
           {1}* W-Cache Init
{0}* W-Cache Init
           {1}* P-Cache RAM
{0}* P-Cache RAM
           {1}Test address up
{0}Test address up
           {1}Test address down
{0}Test address down
           {1}Test cell disturbance
{0}Test cell disturbance
           {1}Test data reliability
{0}Test data reliability
           {1}Test address line transitions
{0}Test address line transitions
           {1}* P-Cache TAGS
           {1}Test address up
{0}* P-Cache TAGS
           {1}Test address down
{0}Test address up
           {1}Test cell disturbance
{0}Test address down
           {1}Test data reliability
{0}Test cell disturbance
           {1}Test address line transitions
{0}Test data reliability
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(11 of 17)*

```
            {1}* P-Cache SnoopTags
            {1}Test address up
{0}Test address line transitions
            {1}Test address down
{0}* P-Cache SnoopTags
            {1}Test cell disturbance
{0}Test address up
            {1}Test data reliability
{0}Test address down
{0}Test cell disturbance
            {1}Test address line transitions
{0}Test data reliability
            {1}* P-Cache Status Data
{0}Test address line transitions
            {1}Test address up
{0}* P-Cache Status Data
            {1}Test address down
{0}Test address up
            {1}Test cell disturbance
{0}Test address down
            {1}Test data reliability
{0}Test cell disturbance
            {1}Test address line transitions
{0}Test data reliability
            {1}* P-Cache Init
{0}Test address line transitions
            {1}* FPU Registers
{0}* P-Cache Init
            {1}Test walking 1/0 FPU registers
{0}* FPU Registers
{0}Test walking 1/0 FPU registers
            {1}Test register addressing
            {1}* FSR
{0}Test register addressing
            {1}Test walking 1 FSR register
{0}* FSR
{0}Test walking 1 FSR register
            {1}* Ecache RAM
{0}* Ecache RAM
            {1}Test address up
{0}Test address up
            {1}Test address down
{0}Test address down
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(12 of 17)*

```
            {1}Test cell disturbance
{0}Test cell disturbance
            {1}Test data reliability
{0}Test data reliability
            {1}Test address line transitions
{0}Test address line transitions
            {1}* Ecache Init
{0}* Ecache Init
            {1}* Correctable Ecache ECC Test
{0}* Correctable Ecache ECC Test
            {1}* Uncorrectable Ecache ECC Test
{0}* Uncorrectable Ecache ECC Test
            {1}* Correctable SW Ecache ECC Test
{0}* Correctable SW Ecache ECC Test
            {1}* Uncorrectable SW Ecache ECC Test
{0}* Uncorrectable SW Ecache ECC Test
            {1}* Correctable System ECC Test
{0}* Correctable System ECC Test
            {1}* Uncorrectable System ECC Test
{0}* Uncorrectable System ECC Test
            {1}* Memory address selection All Banks
{0}* Memory address selection All Banks
{0}* Memory marching All Banks
            {1}* Memory marching All Banks
{0}* Safari registers
{0}Safari ID reg fc000000.0011a954
            {1}* Map PCI B space
{0}* Map PCI A space
            {1}* Schizo reg test
{0}* Schizo reg test
            {1}PBM B registers
{0}PBM A registers
            {1}Iommu B registers
{0}Iommu A registers
            {1}Streaming Cache B registers
{0}Streaming Cache A registers
            {1}Mondo Interrupt B registers
{0}Mondo Interrupt A registers
            {1}* Schizo pci B id test
            {1}PCI B Vendor ID 108e
{0}* Schizo pci A id test
            {1}PCI B Device ID 8001
{0}PCI A Vendor ID 108e
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(13 of 17)*

```
            {1}* Schizo mem test
{0}PCI A Device ID 8001
            {1}memtst ram data port B
{0}* Schizo mem test
{0}memtst ram data port A
            {1}memtst cam data port B
{0}memtst cam data port A
            {1}memtst ram addr port B
{0}memtst ram addr port A
            {1}memtst cam addr port B
{0}memtst cam addr port A
            {1}memtst pnta     port B
{0}memtst pnta     port A
            {1}memtst lnta     port B
{0}memtst lnta     port A
            {1}memtst rnta     port B
{0}memtst rnta     port A
            {1}memtst enta     port B
{0}memtst enta     port A
            {1}memtst ln addr  port B
{0}memtst ln addr  port A
            {1}memtst pg addr  port B
{0}memtst pg addr  port A
            {1}memtst sbuf addr port B
{0}memtst sbuf addr port A
            {1}* Schizo merg test
{0}* Schizo merg test
            {1}merg_wr 8 byte port B
{0}merg_wr 8 byte port A
            {1}merg_wr 4 byte port B
{0}merg_wr 4 byte port A
            {1}merg_wr 2 byte port B
{0}merg_wr 2 byte port A
            {1}merg_wr 1 byte port B
{0}merg_wr 1 byte port A
            {1}merg_blkwr block  port B
{0}merg_blkwr block  port A
{0}* Map PCI B space for RIO
{0}* RIO Config
{0}* RIO EBus access
{0}* Icache Functional
            {1}* Icache Functional
{0}Verify cacheline fill on read miss
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(14 of 17)*

```
            {1}Verify cacheline fill on read miss
{0}* Dcache Functional
            {1}* Dcache Functional
{0}Verify no allocate on write miss
{0}Verify fetch from memory on read miss
            {1}Verify no allocate on write miss
{0}Verify write-through on write hit
            {1}Verify fetch from memory on read miss
{0}Verify write-through/fetch on read miss
            {1}Verify write-through on write hit
            {1}Verify write-through/fetch on read miss
{0}Verify set-associativity
{0}* Wcache Functional
{0}Verify cacheline fill on write miss
{0}Verify buffering
{0}Verify coalescing
            {1}Verify set-associativity
{0}* Pcache Functional
            {1}* Wcache Functional
{0}* FPU Functional
            {1}Verify cacheline fill on write miss
{0}Test single and double-precision addition
            {1}Verify buffering
{0}Test single and double-precision subtraction
            {1}Verify coalescing
{0}Test single and double-precision multiplication
            {1}* Pcache Functional
{0}Test single and double-precision division
            {1}* FPU Functional
{0}Test single and double-precision sqrt
            {1}Test single and double-precision addition
{0}Test single and double-precision abs
            {1}Test single and double-precision subtraction
{0}Test single and double-precision conversion
            {1}Test single and double-precision multiplication
{0}* FPU Move To Registers
            {1}Test single and double-precision division
{0}Moving SP fp value through all fp registers
            {1}Test single and double-precision sqrt
{0}Moving DP fp value through all fp registers
            {1}Test single and double-precision abs
{0}* FPU Branch
            {1}Test single and double-precision conversion
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(15 of 17)*

```
{0}Testing Branching on fcc0
           {1}* FPU Move To Registers
{0}Verify branching
           {1}Moving SP fp value through all fp registers
{0}Verify no branching
           {1}Moving DP fp value through all fp registers
{0}Testing Branching on fcc1
           {1}* FPU Branch
{0}Verify branching
           {1}Testing Branching on fcc0
{0}Verify no branching
           {1}Verify branching
{0}Testing Branching on fcc2
           {1}Verify no branching
{0}Verify branching
           {1}Testing Branching on fcc1
{0}Verify no branching
           {1}Verify branching
{0}Testing Branching on fcc3
           {1}Verify no branching
{0}Verify branching
           {1}Testing Branching on fcc2
{0}Verify no branching
           {1}Verify branching
{0}* Ecache Functional
           {1}Verify no branching
{0}Verify cacheline fill on read miss
           {1}Testing Branching on fcc3
{0}Verify write allocate on write miss
           {1}Verify branching
{0}Verify cacheline update on write hit
           {1}Verify no branching
{0}Verify write back
           {1}* Ecache Functional
           {1}Verify cacheline fill on read miss
           {1}Verify write allocate on write miss
           {1}Verify cacheline update on write hit
           {1}Verify write back
{0}* Xcall Test
{0}Sending Cross Calls to CPU AID 1
           {1}POST_END

@(#)OBP 4.2.3 2001/04/23 17:48 Sun Netra T4
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(16 of 17)*

```
Clearing TLBs Done
POST Results: Cpu 0
  %o0  0000.0000.0000.0000
  %o1  0000.07ff.f015.06b0
  %o2  0000.0000.0000.0000
POST Results: Cpu 1
  %o0  0000.0000.0000.0000
  %o1  0000.07ff.f015.06b0
  %o2  0000.0000.0000.0000
Membase: 0000.0000.0000.0000
MemSize: 0000.0000.0010.0000
Init CPU arrays Done
Init E$ tags Done
Setup TLB Done
MMUs ON
Copy Done
PC = 0000.07ff.f008.4200
PC = 0000.0000.0000.4278
Decompressing Done
Size = 0000.0000.0007.24b0
ttya initialized
Start Reason: Initialize Machine
Configuring the machine:
ú
@(#)OBP 4.2.3 2001/04/23 17:48 Sun Netra T4
Clearing TLBs Done
Loading Configuration
Membase: 0000.0000.0000.0000
MemSize: 0000.0001.0000.0000
Init CPU arrays Done
Init E$ tags Done
Setup TLB Done
MMUs ON
Block Scrubbing Done
Copy Done
PC = 0000.07ff.f008.4200
PC = 0000.0000.0000.4278
Decompressing Done
Size = 0000.0000.0007.24b0
ttya initialized
Start Reason: First start after Power On
System Reset: (SPOR) (PLL)
Probing gptwo at 0,0 SUNW,UltraSPARC-III (750 MHz @ 5:1, 8 MB)
```

CODE EXAMPLE E-1 `diag-level` Variable Set to `max` *(17 of 17)*

```
   memory-controller
Probing gptwo at 1,0 SUNW,UltraSPARC-III (750 MHz @ 5:1, 8 MB)
   memory-controller
Probing gptwo at 8,0 pci pci
Loading Support Packages: kbd-translator
Loading onboard drivers: ebus flashprom bbc power i2c dimm-fru
dimm-fru
   dimm-fru dimm-fru dimm-fru dimm-fru dimm-fru dimm-fru i2c cpu-
fru
   temperature cpu-fru hardware-monitor hardware-monitor
   hardware-monitor temperature fan-control ioexp fan-control
   motherboard-fru ioexp ioexp ioexp fcal-backplane scc-reader
   power-supply lomlite2 nvram idprom beep rtc gpio pmc parallel
lombus
   SUNW,lomc serial lomp lomv
Memory Configuration:
Segment @ Base:        0  Size:  4096 MB ( 4-Way)
SUNW,Netra-T4
Probing /pci@8,600000 Device 4  SUNW,qlc fp disk
Probing /pci@8,600000 Device 1  Nothing there
Probing /pci@8,700000 Device 5  network usb
Probing /pci@8,700000 Device 6  scsi disk tape scsi disk tape
Probing /pci@8,700000 Device 1  Nothing there
Probing /pci@8,700000 Device 2  Nothing there
Probing /pci@8,700000 Device 3  Nothing there
Probing /pci@8,700000 Device 4  Nothing there
```

CODE EXAMPLE E-2 is a typical POST output for a system with two 750 MHz CPUs and 4 GByte of memory, and with the `diag-level` variable set to `min`.

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(1 of 15)*

```
{0}@(#)POST, v4.1.7  01/22/2001 06:55 PM
           {1}Transfered from OBP or Unknown source of reset
{0}PLL reset
{0}* Configure I2C controller 0
{0}* Configure I2C controller 1
{0}* I2C Controller Loopback Test
{0}* Read JTag IDs of all ASICs
{0} BBCJTag ID: 1483203b
{0} SCSIJTag ID: 15060045
{0} I chipJTag ID: d1e203b
{0} RIOJTag ID: 13e5d03b
{0} SchizoJTag ID: 1824c06d
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(2 of 15)*

```
{0} CPMSJTag ID: 1142903b
{0} CPMSJTag ID: 1142903b
{0} CPMSJTag ID: 1142903b
{0} CPMSJTag ID: 1142903b
{0} CPMSJTag ID: 1142903b
{0} CPMSJTag ID: 1142903b
{0}* Read JTag ID of FCAL
{0} FC-ALJTag ID: 1000a12f
{0}* Probing Seeprom on DIMMs and CPU modules
{0}CPU0 Sensor package temperature 43 oC
{0}CPU1 Sensor package temperature 22 oC
{0}WARNING: Temperature sensor on UPA0 missing
{0}WARNING: Temperature sensor on UPA1 missing
{0}WARNING: Smart card reader missing
{0}* Read parameters from seeproms
{0}        Size/bank(MB)Number of banks
{0}DIMM 0:2562
{0}DIMM 1:2562
{0}DIMM 2:2562
{0}DIMM 3:2562
{0}DIMM 4:2562
{0}DIMM 5:2562
{0}DIMM 6:2562
{0}DIMM 7:2562
{0}Bank 0 is  present, size = 00000000.40000000
{0}Bank 1 is  present, size = 00000000.40000000
{0}Bank 2 is  present, size = 00000000.40000000
{0}Bank 3 is  present, size = 00000000.40000000
{0}* Setup CPUs and system frequency
{0}CPU 0 ratio: 5
{0}CPU 1 ratio: 5
{0}System frequency: 150 MHz
{0}* Load PLL and reset
           {1}PLL reset
{0}PLL reset
           {1}* SoftInt & Interrupt
{0}* Configure I2C controller 0
           {1}Test walking 1 through softint register
{0}* Configure I2C controller 1
           {1}Test walking 0 through softint register
{0}* SoftInt & Interrupt
           {1}Verify interrupt occurs for each level
{0}Test walking 1 through softint register
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(3 of 15)*

```
            {1}Verify interrupt occurs at the right PIL
{0}Test walking 0 through softint register
            {1}* Tick & Tick-Compare Reg
{0}Verify interrupt occurs for each level
            {1}Walk 1/0 TICK Compare register
{0}Verify interrupt occurs at the right PIL
            {1}Verify TICK register is counting
{0}* Tick & Tick-Compare Reg
            {1}Verify TICK register Overflow
{0}Walk 1/0 TICK Compare register
            {1}Verify TICK Interrupt
{0}Verify TICK register is counting
{0}Verify TICK register Overflow
{0}Verify TICK Interrupt
            {1}* Stick & Stick-Compare Reg
            {1}Walk 1/0 STICK Compare register
            {1}Verify STICK register is counting
{0}* Stick & Stick-Compare Reg
            {1}Verify STICK register Overflow
{0}Walk 1/0 STICK Compare register
            {1}Verify STICK Interrupt
{0}Verify STICK register is counting
{0}Verify STICK register Overflow
{0}Verify STICK Interrupt
            {1}* Measure CPU Clock
{0}* Measure CPU Clock
{0}AFT pin is high
{0}Setup Memory Controller
{0}* IMMU Registers
            {1}* IMMU Registers
{0}Testing I-TSB
            {1}Testing I-TSB
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Test walking 0 through the register
            {1}Test walking 0 through the register
{0}Testing I-TLB Tag Access
            {1}Testing I-TLB Tag Access
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Test walking 0 through the register
            {1}Test walking 0 through the register
{0}* DMMU Registers
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(4 of 15)*

```
            {1}* DMMU Registers
{0}Testing Primary Context
            {1}Testing Primary Context
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Testing Secondary Context
            {1}Testing Secondary Context
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Testing D-TSB
            {1}Testing D-TSB
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Testing D-TLB Tag Access
            {1}Testing D-TLB Tag Access
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Testing Virtual Watchpoint
            {1}Testing Virtual Watchpoint
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}Testing Physical Watchpoint
            {1}Testing Physical Watchpoint
{0}Test walking 1 through the register
            {1}Test walking 1 through the register
{0}* 4M DTLB RAM
            {1}* 4M DTLB RAM
{0}Test address up
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}* 8K DTLB RAM
            {1}* 8K DTLB RAM
{0}Test address up
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}* 4M DTLB TAG
{0}Test address up
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(5 of 15)*

```
            {1}* 4M DTLB TAG
{0}Test address down
            {1}Test address up
{0}Test cell disturbance
            {1}Test address down
{0}* 8K DTLB TAG
            {1}Test cell disturbance
{0}Test address up
            {1}* 8K DTLB TAG
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test address line transitions
            {1}Test address line transitions
{0}* 4M ITLB RAM
{0}Test address up
{0}Test address down
            {1}* 4M ITLB RAM
{0}Test cell disturbance
            {1}Test address up
{0}* 8K ITLB RAM
            {1}Test address down
{0}Test address up
            {1}Test cell disturbance
{0}Test address down
            {1}* 8K ITLB RAM
{0}Test cell disturbance
            {1}Test address up
            {1}Test address down
{0}* 4M ITLB TAG
{0}Test address up
            {1}Test cell disturbance
{0}Test address down
{0}Test cell disturbance
            {1}* 4M ITLB TAG
{0}* 8K ITLB TAG
            {1}Test address up
{0}Test address up
            {1}Test address down
{0}Test address down
            {1}Test cell disturbance
{0}Test address line transitions
            {1}* 8K ITLB TAG
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(6 of 15)*

```
{0}* IMMU Init
            {1}Test address up
{0}* DMMU Init
            {1}Test address down
{0}Mapping done. MMU enabled
            {1}Test address line transitions
{0}* Memory address selection Initial area
            {1}* IMMU Init
            {1}* DMMU Init
            {1}Mapping done. MMU enabled
            {1}* Memory address selection Initial area
{0}* E-Cache Global Vars Init
{0}* E-Cache Quick Verification
            {1}* E-Cache Global Vars Init
            {1}* E-Cache Quick Verification
{0}* Ecache TAGS
{0}Test address up
            {1}* Ecache TAGS
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}* Ecache Address Line
            {1}* Ecache Address Line
{0}* Partial Ecache Init
            {1}* Partial Ecache Init
{0}* BBC E-Star Registers
{0}* I-Cache RAM
            {1}* I-Cache RAM
{0}Test address up
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}* I-Cache TAGS
{0}Testing I-Cache Tag
            {1}* I-Cache TAGS
{0}Test address up
            {1}Testing I-Cache Tag
            {1}Test address up
{0}Test address down
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(7 of 15)*

```
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}Testing I-Cache Micro Tag
{0}Test address up
            {1}Testing I-Cache Micro Tag
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}* I-Cache Snoop Tags
{0}Test address up
            {1}* I-Cache Snoop Tags
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}* I-Cache Init
            {1}* I-Cache Init
{0}* D-Cache RAM
{0}Test address up
            {1}* D-Cache RAM
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}* D-Cache TAGS
{0}Test address up
            {1}* D-Cache TAGS
            {1}Test address up
{0}Test address down
            {1}Test address down
{0}Test cell disturbance
            {1}Test cell disturbance
{0}* D-Cache MicroTags
{0}Test address up
            {1}* D-Cache MicroTags
            {1}Test address up
{0}Test address down
            {1}Test address down
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(8 of 15)*

```
{0}Test cell disturbance
           {1}Test cell disturbance
{0}* D-Cache SnoopTags
{0}Test address up
           {1}* D-Cache SnoopTags
           {1}Test address up
{0}Test address down
           {1}Test address down
{0}Test cell disturbance
           {1}Test cell disturbance
{0}* D-Cache Init
           {1}* D-Cache Init
{0}* W-Cache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* W-Cache TAGS
           {1}* W-Cache RAM
{0}Test address up
           {1}Test address up
{0}Test address down
{0}Test cell disturbance
           {1}Test address down
{0}* W-Cache SnoopTAGS
{0}Test address up
           {1}Test cell disturbance
{0}Test address down
{0}Test cell disturbance
           {1}* W-Cache TAGS
{0}* W-Cache Init
           {1}Test address up
{0}* P-Cache RAM
           {1}Test address down
{0}Test address up
           {1}Test cell disturbance
{0}Test address down
           {1}* W-Cache SnoopTAGS
           {1}Test address up
{0}Test cell disturbance
           {1}Test address down
           {1}Test cell disturbance
{0}* P-Cache TAGS
           {1}* W-Cache Init
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(9 of 15)*

```
{0}Test address up
           {1}* P-Cache RAM
{0}Test address down
           {1}Test address up
{0}Test cell disturbance
           {1}Test address down
{0}* P-Cache SnoopTags
{0}Test address up
           {1}Test cell disturbance
{0}Test address down
{0}Test cell disturbance
           {1}* P-Cache TAGS
{0}* P-Cache Status Data
           {1}Test address up
{0}Test address up
           {1}Test address down
{0}Test address down
           {1}Test cell disturbance
{0}Test cell disturbance
           {1}* P-Cache SnoopTags
{0}* P-Cache Init
           {1}Test address up
{0}* FPU Registers
           {1}Test address down
{0}Test walking 1/0 FPU registers
           {1}Test cell disturbance
           {1}* P-Cache Status Data
           {1}Test address up
           {1}Test address down
           {1}Test cell disturbance
           {1}* P-Cache Init
           {1}* FPU Registers
           {1}Test walking 1/0 FPU registers
{0}Test register addressing
{0}* FSR
{0}Test walking 1 FSR register
{0}* Ecache RAM
{0}Test address up
           {1}Test register addressing
           {1}* FSR
           {1}Test walking 1 FSR register
           {1}* Ecache RAM
           {1}Test address up
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(10 of 15)*

```
{0}Test address down
           {1}Test address down
{0}Test cell disturbance
           {1}Test cell disturbance
{0}* Ecache Init
           {1}* Ecache Init
{0}* Correctable Ecache ECC Test
           {1}* Correctable Ecache ECC Test
{0}* Uncorrectable Ecache ECC Test
           {1}* Uncorrectable Ecache ECC Test
{0}* Correctable SW Ecache ECC Test
           {1}* Correctable SW Ecache ECC Test
{0}* Uncorrectable SW Ecache ECC Test
           {1}* Uncorrectable SW Ecache ECC Test
{0}* Correctable System ECC Test
           {1}* Correctable System ECC Test
{0}* Uncorrectable System ECC Test
           {1}* Uncorrectable System ECC Test
{0}* Memory address selection All Banks
           {1}* Memory address selection All Banks
{0}* Safari registers
{0}Safari ID reg fc000000.0011a954
           {1}* Map PCI B space
{0}* Map PCI A space
           {1}* Schizo reg test
{0}* Schizo reg test
           {1}PBM B registers
{0}PBM A registers
           {1}Iommu B registers
{0}Iommu A registers
           {1}Streaming Cache B registers
{0}Streaming Cache A registers
           {1}Mondo Interrupt B registers
{0}Mondo Interrupt A registers
           {1}* Schizo pci B id test
           {1}PCI B Vendor ID 108e
{0}* Schizo pci A id test
           {1}PCI B Device ID 8001
{0}PCI A Vendor ID 108e
           {1}* Schizo mem test
{0}PCI A Device ID 8001
           {1}memtst ram data port B
{0}* Schizo mem test
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(11 of 15)*

```
{0}memtst ram data port A
           {1}memtst cam data port B
{0}memtst cam data port A
           {1}memtst ram addr port B
{0}memtst ram addr port A
           {1}memtst cam addr port B
{0}memtst cam addr port A
           {1}memtst pnta     port B
{0}memtst pnta     port A
           {1}memtst lnta     port B
{0}memtst lnta     port A
           {1}memtst rnta     port B
{0}memtst rnta     port A
           {1}memtst enta     port B
{0}memtst enta     port A
           {1}memtst ln addr  port B
{0}memtst ln addr  port A
           {1}memtst pg addr  port B
{0}memtst pg addr  port A
           {1}memtst sbuf addr port B
{0}memtst sbuf addr port A
           {1}* Schizo merg test
{0}* Schizo merg test
           {1}merg_wr 8 byte port B
{0}merg_wr 8 byte port A
           {1}merg_wr 4 byte port B
{0}merg_wr 4 byte port A
{0}* Map PCI B space for RIO
{0}* RIO Config
{0}* RIO EBus access
{0}* Icache Functional
           {1}* Icache Functional
{0}Verify cacheline fill on read miss
           {1}Verify cacheline fill on read miss
{0}* Dcache Functional
           {1}* Dcache Functional
{0}Verify no allocate on write miss
{0}Verify fetch from memory on read miss
           {1}Verify no allocate on write miss
{0}Verify write-through on write hit
           {1}Verify fetch from memory on read miss
{0}Verify write-through/fetch on read miss
           {1}Verify write-through on write hit
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(12 of 15)*

```
            {1}Verify write-through/fetch on read miss
{0}Verify set-associativity
{0}* Wcache Functional
{0}Verify cacheline fill on write miss
{0}Verify buffering
{0}Verify coalescing
            {1}Verify set-associativity
{0}* Pcache Functional
            {1}* Wcache Functional
{0}* FPU Functional
            {1}Verify cacheline fill on write miss
{0}Test single and double-precision addition
            {1}Verify buffering
{0}Test single and double-precision subtraction
            {1}Verify coalescing
{0}Test single and double-precision multiplication
            {1}* Pcache Functional
{0}Test single and double-precision division
            {1}* FPU Functional
{0}Test single and double-precision sqrt
            {1}Test single and double-precision addition
{0}Test single and double-precision abs
            {1}Test single and double-precision subtraction
{0}Test single and double-precision conversion
            {1}Test single and double-precision multiplication
{0}* FPU Move To Registers
            {1}Test single and double-precision division
{0}Moving SP fp value through all fp registers
            {1}Test single and double-precision sqrt
{0}Moving DP fp value through all fp registers
            {1}Test single and double-precision abs
{0}* FPU Branch
            {1}Test single and double-precision conversion
{0}Testing Branching on fcc0
            {1}* FPU Move To Registers
{0}Verify branching
            {1}Moving SP fp value through all fp registers
{0}Verify no branching
            {1}Moving DP fp value through all fp registers
{0}Testing Branching on fcc1
            {1}* FPU Branch
{0}Verify branching
            {1}Testing Branching on fcc0
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(13 of 15)*

```
{0}Verify no branching
           {1}Verify branching
{0}Testing Branching on fcc2
           {1}Verify no branching
{0}Verify branching
           {1}Testing Branching on fcc1
{0}Verify no branching
           {1}Verify branching
{0}Testing Branching on fcc3
           {1}Verify no branching
{0}Verify branching
           {1}Testing Branching on fcc2
{0}Verify no branching
           {1}Verify branching
{0}* Ecache Functional
           {1}Verify no branching
{0}Verify cacheline fill on read miss
           {1}Testing Branching on fcc3
{0}Verify write allocate on write miss
           {1}Verify branching
{0}Verify cacheline update on write hit
           {1}Verify no branching
{0}Verify write back
           {1}* Ecache Functional
           {1}Verify cacheline fill on read miss
           {1}Verify write allocate on write miss
           {1}Verify cacheline update on write hit
           {1}Verify write back
{0}* Xcall Test
{0}Sending Cross Calls to CPU AID 1
           {1}POST_END

@(#)OBP 4.2.3 2001/04/23 17:48 Sun Netra T4
Clearing TLBs Done
POST Results: Cpu 0
  %o0  0000.0000.0000.0000
  %o1  0000.07ff.f015.06b0
  %o2  0000.0000.0000.0000
POST Results: Cpu 1
  %o0  0000.0000.0000.0000
  %o1  0000.07ff.f015.06b0
  %o2  0000.0000.0000.0000
Membase: 0000.0000.0000.0000
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(14 of 15)*

```
MemSize: 0000.0000.0010.0000
Init CPU arrays Done
Init E$ tags Done
Setup TLB Done
MMUs ON
Copy Done
PC = 0000.07ff.f008.4200
PC = 0000.0000.0000.4278
Decompressing Done
Size = 0000.0000.0007.24b0
ttya initialized
Start Reason: Initialize Machine
Configuring the machine:
ú
@(#)OBP 4.2.3 2001/04/23 17:48 Sun Netra T4
Clearing TLBs Done
Loading Configuration
Membase: 0000.0000.0000.0000
MemSize: 0000.0001.0000.0000
Init CPU arrays Done
Init E$ tags Done
Setup TLB Done
MMUs ON
Block Scrubbing Done
Copy Done
PC = 0000.07ff.f008.4200
PC = 0000.0000.0000.4278
Decompressing Done
Size = 0000.0000.0007.24b0
ttya initialized
Start Reason: First start after Power On
System Reset: (SPOR) (PLL)
Probing gptwo at 0,0 SUNW,UltraSPARC-III (750 MHz @ 5:1, 8 MB)
   memory-controller
Probing gptwo at 1,0 SUNW,UltraSPARC-III (750 MHz @ 5:1, 8 MB)
   memory-controller
Probing gptwo at 8,0 pci pci
Loading Support Packages: kbd-translator
Loading onboard drivers: ebus flashprom bbc power i2c dimm-fru
dimm-fru
   dimm-fru dimm-fru dimm-fru dimm-fru dimm-fru dimm-fru i2c cpu-
fru
   temperature cpu-fru hardware-monitor hardware-monitor
```

CODE EXAMPLE E-2 `diag-level` Variable Set to `min` *(15 of 15)*

```
    hardware-monitor temperature fan-control ioexp fan-control
    motherboard-fru ioexp ioexp ioexp fcal-backplane scc-reader
    power-supply lomlite2 nvram idprom beep rtc gpio pmc parallel
lombus
    SUNW,lomc serial lomp lomv
Memory Configuration:
Segment @ Base:        0  Size:  4096 MB ( 4-Way)
SUNW,Netra-T4
Probing /pci@8,600000 Device 4  SUNW,qlc fp disk
Probing /pci@8,600000 Device 1  Nothing there
Probing /pci@8,700000 Device 5  network usb
Probing /pci@8,700000 Device 6  scsi disk tape scsi disk tape
Probing /pci@8,700000 Device 1  Nothing there
Probing /pci@8,700000 Device 2  Nothing there
Probing /pci@8,700000 Device 3  Nothing there
Probing /pci@8,700000 Device 4  Nothing there
```

APPENDIX **F**

Updating LOMlite2 Firmware

This appendix explains how to update the Lights Out Management firmware.

1. **Connect a terminal to the LOMlite2 serial port as described in Appendix D of the** *Netra T4 AC100/DC100 Installation and User's Guide***.**

   Power up the system and boot to the Unix (#) prompt.

2. **Change to the** `/var/tmp` **directory.**

   This directory should contain the current patch (in the example, `110208-09`).

```
# cd /var/tmp
# ls
110208-09
110208-09.tar
#
```

Note – Your version number will probably be different.

3. **Remove the tar file and the directory and its contents.**

```
# rm 110208-09.tar
# rm -r 110208-09
```

4. **Remove the existing patch.**

```
# patchrm 110208-09
Checking installed patches...

Executing prebackout script...
prebackout: Starting ...
removing driver
prebackout: Finished
Backing out patch 110208-09...

Patch 110208-09 has been backed out.
```

5. **Reboot the system.**

6. **Copy the new patch into the** `/var/tmp` **directory.**

   From the `/var/tmp` directory, confirm that it contains the file `1102018-<version#>.tar` and then run a checksum to confirm that it has been copied correctly.

```
# cksum 110208-<version#>.tar
123456789 1076224 110208-<version#>.tar
#
```

Note – Your checksum will be different.

   If the checksum is not correct, the file is corrupt.

7. **Extract the files from the patch.**

```
# tar xf /var/tmp/110208-<version#>.tar
```

8. **Install the new patch.**

```
# patchadd 110208-<version#>
```

9. **Reboot the system.**

10. **To update the LOMlite2 firmware, at the Unix prompt (#) type:**

```
# lom -G default
```

Note – This process takes about five minutes. Do not turn off the system while the update is progressing.

Press Return to redisplay the Unix prompt.

11. **Enter `#.` to change to the LOMlite2 prompt.**

```
# #.
lom>
```

12. **Run the `ver` command to confirm that the firmware has been updated.**

```
lom> ver
```

13. **Finally, check the functionality by running the `env` command from the `lom>` prompt.**

```
lom> env
LEDs:
1 Power            ON
2 Fault            ON
3 Supply A         OFF
4 Supply B         OFF
5 PSU ok           ON
6 PSU fail         OFF

Alarms:
1 -                OFF
2 -                OFF
3 -                ON

PSUs:
1 AC               OK

Fans:
1 PSU1             OK speed 88%
2 PSU2             OK speed 86%
3 CPU              OK speed 94%

Temperature sensors:
1 Ambient          OK 21degC
2 CPU0 enclosure   OK 22degC
3 CPU0 die         OK 53degC
4 CPU1 enclosure   OK 21degC
5 CPU1 die         OK 50degC

Overheat sensors:
1 PSU              OK

Circuit breakers:
1 SCC              OK
2 PSU              OK
```

APPENDIX **G**

Connecting to the Netra T4 Server

This appendix describes how to connect a terminal and other equipment to the external ports on your Netra T4 server.

The appendix contains the following sections:

- "Connecting to the LOM Serial Port" on page 1
- "Connecting to the Serial Ports" on page 2

G.1 Connecting to the LOM Serial Port

The LOM serial port is the default console port. To connect a terminal to the LOM serial (RJ-45) port you require one of the following:

- RJ-45 (male) to DB-25 (male) cable, wired as shown in TABLE G-1
- CAT5 Ethernet cable RJ-45 (male) to RJ-45 (male), part no. 530-2961, and an RJ-45 (female) to DB-25 (male) adaptor, part no. 530-2889, wired as shown in TABLE G-1

TABLE G-1 LOM Serial Port Adaptor Pinouts

RJ-45 (LOM Port)	Signal	DB-25 (Terminal)
1	RTS/CTS	5
2	DTR/DSR	6
3	TXD/RXD	3
4	REF/GND	N/C or GND
5	REF/GND	N/C or GND

TABLE G-1 LOM Serial Port Adaptor Pinouts *(Continued)*

RJ-45 (LOM Port)	Signal	DB-25 (Terminal)
6	RXD / TXD	2
7	DSR / DTR	20
8	CTS / RTS	4

To communicate with your Netra T4 server, connect the cable from serial port A on your terminal to the LOM serial port on the Netra T4 server.

1. **Power on your terminal and open a window.**
2. **Connect your Netra T4 server to the mains power supply.**

   The `lom>` prompt is displayed on the terminal.
3. **Power on the server by pressing the ON switch until the server starts to power up and wait for the `ok` prompt to appear on the terminal.**

G.2 Connecting to the Serial Ports

You can also use the Netra T4 serial ports A and B (ttya and ttyb) as a console port. You require one of the following:

- DB-25 male to DB-25 (male) crossover cable wired as shown in TABLE G-2
- DB-25 (male) to DBV-25 (male) straight through cable with a crossover adaptor wired as shown in TABLE G-2

TABLE G-2 Netra T4 Serial Port Crossover Adaptor Pinouts

DB-25 (Netra T4)	Signal	DB-25 (Terminal)
1		1
2	RXD / TXD	3
3	TXD / RXD	2
4	RTS / CTS	5
5	CTS / RTS	4
6	DSR / DTR	20
7	GND / GND	7

TABLE G-2 Netra T4 Serial Port Crossover Adaptor Pinouts *(Continued)*

DB-25 (Netra T4)	Signal	DB-25 (Terminal)
8	DCD / DTR	20
20	DTR / DSR	6
20	DTR / DCD	8

You must also configure the Netra T4 serial port as the input and output device, and direct the diagnostic output to the console:

```
ok setenv diag-out-console true
ok setenv input-device ttya
ok setenv output-device ttya
```

Glossary

address (1) A number used by the system software to identify a storage location. (2) In networking, a unique code that identifies a node to the network.

ASIC Application-specific integrated circuit

Asynchronous An operation that is not synchronized with the timing of any other part of the system.

BBC BootBus controller

boot To load the system software into memory and start it running.

boot PROM In Sun workstations, the boot PROM contains a PROM monitor program, a command interpreter used for booting, resetting, low-level configuring, and simple testing.

CRC Cyclic redundancy check

DAT Digital audio tape

DIMM Dual in-line memory module. A small printed circuit card that contains dynamic random-access memory chips.

DMA Direct memory address

DRAM Dynamic random-access memory. Read / write dynamic memory in which the data can be read or written in approximately the same amount of time for any memory location.

DTAG Dual tag or data tag

DVD Digital video disk

DVM Digital voltage meter

EBus A slow byte-wide bus for low-speed devices.

EEPROM Electrically erasable programmable read only memory

EMI Electromagnetic interference. Electrical characteristic that directly or indirectly contributes to a degradation in performance of an electronic system.

EPCI Extended peripheral component interconnect, a 64bit, 66MHz PCI bus

ESD Electrostatic discharge

Ethernet A type of local area network that enables real-time communication between network devices, connected directly together through cables. A widely implemented network from which the IEEE 802.3 standard for contention networks was developed, Ethernet uses a bus topology (configuration) and relies on the form of access known as CSMA/CD to regulate traffic on the main communication line. Network nodes are connected by coaxial cable (in either of two varieties) or by twisted-pair wiring. See also **10BASE-T**, and **100BASE-T**.

FC-AL Fiber channel arbitrated loop

FIFO First-in, first-out

flash PROM A type of programmable read-only memory (PROM) that can be reprogrammed by a voltage pulse. See also **PROM**.

FRU Field-replaceable unit

Gbyte Gigabyte, 10^9 bytes

GUI Graphical user interface

HSI High speed serial interface

I/O Input/output

JTAG An interface from the Boot Bus Controller that enables testing of the ASICs on the motherboard.

Kbyte Kilobyte, 10^3 bytes

Leaf Any node (location in a tree structure) that is farthest from the primary node.

LED Light-emitting diode

LOM Lights Out Management

MBps Megabyte per second

Mbps Megabit per second

Mbyte Megabyte, one million bytes

MHz Megahertz

MII Media independent interface

Network A configuration of data processing devices and software connected together for information exchange.

NG-DIMM Next generation dual inline memory module

Node An addressable point on a network. Each node in a Sun network has a different name. A node can connect a computing system, a terminal, or various other peripheral devices to the network.

ns Nanosecond, 10^{-9} seconds

NVRAM Nonvolatile random-access memory. A type of RAM that retains information when power is removed from the system. In Sun systems, contains the system hostID number and Ethernet address. In Netra T4 systems, this information is stored on the system configuration card.

OBP OpenBoot PROM. A routine that tests the network controller, diskette drive system, memory, cache, system clock, network monitoring, and control registers.

PBM PCI bus module

PCI bus Peripheral component interconnect bus. A high-performance 32 or 64 bit-wide bus with multiplexed address and data lines.

PCIO PCI-to-EBus/Ethernet controller. An ASIC that bridges the PCI bus to the EBus, enabling communication between the PCI bus and all miscellaneous I/O functions, as well as the connection to slower on-board functions.

PDB power distribution board

Peripheral assembly Removable media assembly. Can include a card reader, CD-ROM drive, DVD-ROM drive, 4-mm tape drive, a diskette drive, and any other 3.5-inch device.

PID Process ID

POR Power on reset

POST Power on self-test. A series of tests that verify that system board components are operating properly. Initialized at system power-on or when the system is rebooted

PROM Programmable Read-Only Memory. A type of read-only memory (ROM) that allows data to be written into the device with hardware device called a PROM programmer. After the PROM has been programmed, it is dedicated to that data and cannot be reprogrammed.

PSU power supply unit

QFE Quad fast Ethernet

RAID Redundant array of inexpensive disks

RMM Removeable media module

SAI	Serial asynchronous interface
SBC	System bus controller
SBus	Serial bus
SCC	System configuration card
SCCR	System configuration card reader
SCSI	Small computer system interface
SERDES	Serializer / deserializer
SLVM	Sun Logical Volume Manager
SRAM	Static random access memory
STP	Shielded twisted-pair
Sun Crossbar Interconnect	A high speed, wide data path, super computing architecture that allows independent and simultaneous connections between major system components.
SunVTS	Validation Test Suite, a diagnostic application designed to test hardware.
Synchronization	The action of forcing certain points in the execution sequences of two or more asynchronous processes to coincide in time.
TIP	A connection that enables a remote shell window to be used as a terminal to display test data from a system.
TPE	Twisted-pair Ethernet
TOD	Time of day. A timekeeping integrated circuit.
TTL	Transistor-transistor logic
UPA	UltraSPARC port architecture. Provides graphics interconnection.
UTP	Unshielded twisted-pair
VRMS	Volts root-mean-square
10BASE-T	An evolution of Ethernet technology that succeeded 10BASE5 and 10BASE2 as the most popular method of physical network implementation. A 10BASE-T network has a data transfer rate of 10 megabits per second and uses unshielded twisted-pair wiring with RJ-45 modular telephone plugs and sockets.

100BASE-T Also known as Fast Ethernet, an Ethernet technology that supports a data transfer rate of 100 megabits per second over special grades of twisted-pair wiring. 100BASE-T uses the same protocol as 10BASE-T. There are three subsets of the 100BASE-T technology: 100BASE-TX defines digital transmission over two pairs of shielded twisted-pair wire. 100BASE-T4 defines digital transmission over four pairs of unshielded twisted-pair wire. 100BASE-TX defines digital transmission over fiber-optic cable.

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