Sun Blade™ 1000 Service Manual

Sun Microsystems, Inc.
901 San Antonio Road
Palo Alto, CA 94303
U.S.A. 650-960-1300

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Send comments about this document to: docfeedback@sun.com

Regulatory Compliance Statements

Your Sun product is marked to indicate its compliance class:

- Federal Communications Commission (FCC) — USA
- Department of Communications (DOC) — Canada
- Voluntary Control Council for Interference (VCCI) — Japan

Please read the appropriate section that corresponds to the marking on your Sun product before attempting to install the product.

FCC Class A Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy, and if it is not installed and used in accordance with the instruction manual, it may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Shielded Cables: Connections between the workstation and peripherals must be made using shielded cables to comply with FCC radio frequency emission limits. Networking connections can be made using unshielded twisted-pair (UTP) cables.

Modifications: Any modifications made to this device that are not approved by Sun Microsystems, Inc. may void the authority granted to the user by the FCC to operate this equipment.

FCC Class B Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

Shielded Cables: Connections between the workstation and peripherals must be made using shielded cables in order to maintain compliance with FCC radio frequency emission limits. Networking connections can be made using unshielded twisted pair (UTP) cables.

Modifications: Any modifications made to this device that are not approved by Sun Microsystems, Inc. may void the authority granted to the user by the FCC to operate this equipment.

ICES-003 Class A Notice - Avis NMB-003, Classe A

This Class A digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.

ICES-003 Class B Notice - Avis NMB-003, Classe B

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

VCCI 基準について

クラス A VCCI 基準について

クラス A VCCI の表示があるワークステーションおよびオプション製品は、クラス A 情報技術装置です。これらの製品には、下記の項目が該当します。

この装置は、情報処理装置等電波障害自主規制協議会 (VCCI) の基準に基づくクラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

クラス B VCCI 基準について

クラス B VCCI の表示  があるワークステーションおよびオプション製品は、クラス B 情報技術装置です。これらの製品には、下記の項目が該当します。

この装置は、情報処理装置等電波障害自主規制協議会 (VCCI) の基準に基づくクラス B 情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。取扱説明書に従って正しい取り扱いをしてください。

BSMI Class A Notice

The following statement is applicable to products shipped to Taiwan and marked as Class A on the product compliance label.

警告使用者：
這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻 干擾，在這種情況下，使用者 會被要求採取某些適當的對策。

Declaration of Conformity

Compliance Model Number: 180

Product Name: Sun Blade 1000

EMC

USA—FCC Class B

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

European Union

This equipment complies with the following requirements of the EMC Directive 89/336/EEC:

EN55022:1995/CISPR22:1997		Class B
EN550024:1998	EN61000-4-2	4 kV (Direct), 8 kV (Air)
	EN61000-4-3	3 V/m
	EN61000-4-4	1.0 kV Power Lines, 0.5 kV Signal Lines
	EN61000-4-5	1 kV Line-Line, 2 kV Line-GND Power Lines
	EN61000-4-6	3 V
	EN61000-4-8	3 A/m
	EN61000-4-11	Pass
EN61000-3-2:1995		Pass
EN61000-3-3:1995		Pass

Safety

This equipment complies with the following requirements of the Low Voltage Directive 73/23/EEC:

EC Type Examination Certificates:

EN60950:1992, 2nd Edition, Amendments 1,2,3,4	TUV Rheinland Certificate No. S 9872459
IEC 950:1991, 2nd Edition, Amendments 1,2,3,4	
Evaluated to all CB Countries	CB Scheme Certificate No. US/3009/UL

Supplementary Information

This product was tested and complies with all the requirements for the CE Mark.

Dennis P. Symanski DATE
Manager, Compliance Engineering

Sun Microsystems, Inc.
901 San Antonio Road, MPK15-102
Palo Alto, CA 94303-4900, USA

Tel: 650-786-3255
Fax: 650-786-3723

Peter Arkless DATE
Quality Manager

Sun Microsystems Scotland, Limited
Springfield, Linlithgow
West Lothian, EH49 7LR
Scotland, United Kingdom

Tel: 0506-670000
Fax: 0506 760011

Safety Agency Compliance Statements

Read this section before beginning any procedure. The following text provides safety precautions to follow when installing a Sun Microsystems product.

Safety Precautions

For your protection, observe the following safety precautions when setting up your equipment:

- Follow all cautions and instructions marked on the equipment.
- Ensure that the voltage and frequency of your power source match the voltage and frequency inscribed on the equipment's electrical rating label.
- Never push objects of any kind through openings in the equipment. Dangerous voltages may be present. Conductive foreign objects could produce a short circuit that could cause fire, electric shock, or damage to your equipment.

Symbols

The following symbols may appear in this book:

Caution – There is risk of personal injury and equipment damage. Follow the instructions.

Caution – Hot surface. Avoid contact. Surfaces are hot and may cause personal injury if touched.

Caution – Hazardous voltages are present. To reduce the risk of electric shock and danger to personal health, follow the instructions.

Modifications to Equipment

Do not make mechanical or electrical modifications to the equipment. Sun Microsystems is not responsible for regulatory compliance of a modified Sun product.

Placement of a Sun Product

Caution – Do not block or cover the openings of your Sun product. Never place a Sun product near a radiator or heat register. Failure to follow these guidelines can cause overheating and affect the reliability of your Sun product.

Caution – The workplace-dependent noise level defined in DIN 45 635 Part 1000 must be 70Db(A) or less.

SELV Compliance

Safety status of I/O connections comply to SELV requirements.

Power Cord Connection

Caution – Sun products are designed to work with single-phase power systems having a grounded neutral conductor. To reduce the risk of electric shock, do not plug Sun products into any other type of power system. Contact your facilities manager or a qualified electrician if you are not sure what type of power is supplied to your building.

Caution – Not all power cords have the same current ratings. Household extension cords do not have overload protection and are not meant for use with computer systems. Do not use household extension cords with your Sun product.

Caution – Your Sun product is shipped with a grounding type (three-wire) power cord. To reduce the risk of electric shock, always plug the cord into a grounded power outlet.

Lithium Battery

Caution – This system contains a replaceable lithium battery, part number 150-2850. Lithium batteries may explode if mishandled. Do not dispose of the battery in fire. Do not disassemble it or attempt to recharge it.

System Unit Cover

You must remove the cover of your Sun computer system unit to add cards, memory, or internal storage devices. Be sure to replace the cover before powering on your computer system.

Caution – Do not operate Sun products without top cover in place. Failure to take this precaution may result in personal injury and system damage.

Laser Compliance Notice

Sun products that use laser technology comply with Class 1 laser requirements.

Class 1 Laser Product
Luokan 1 Laserlaite
Klasse 1 Laser Apparat
Laser KLasse 1

CD-ROM or DVD-ROM

Caution – Use of controls, adjustments, or the performance of procedures other than those specified herein may result in hazardous radiation exposure.

Conformité aux normes de sécurité

Lisez attentivement la section suivante avant d'entamer une procédure quelconque. Le texte suivant énumère toutes les précautions de sécurité à observer lors de l'installation d'un produit Sun Microsystems.

Mesures de sécurité

Pour votre protection, observez les mesures de sécurité suivantes lors de la mise en marche de l'équipement :

- Observez tous les avertissements et consignes indiqués sur l'équipement.
- Assurez-vous que la tension et la fréquence de votre source d'alimentation électrique correspondent à la tension et à la fréquence indiquées sur l'étiquette de tension électrique nominale du matériel.
- N'insérez en aucun cas un objet quelconque dans les orifices d'aération de l'équipement. Des tensions potentiellement dangereuses peuvent être présentes dans l'équipement. Tout objet étranger conducteur risque de produire un court-circuit présentant un risque d'incendie ou de décharge électrique, ou susceptible d'endommager le matériel.

Symboles

Les symboles suivants peuvent figurent dans cet ouvrage :

Attention – Vous risquez d'endommager le matériel ou de vous blesser. Observez les consignes données.

Attention – Surface brûlante. Evitez tout contact. Ces surfaces sont brûlantes et risquent de vous blesser si vous les touchez.

Attention – Des tensions dangereuses sont présentes dans l'équipement. Pour réduire le risque de décharge électrique et de danger physique personnel, observez les consignes données.

Modifications de l'équipement

N'apportez aucune modification mécanique ou électrique à l'équipement. Sun Microsystems décline toute responsabilité quant à la non-conformité éventuelle d'un produit Sun modifié.

Lieu d’installation d'un produit Sun

Attention – Evitez de bloquer ou de couvrir les orifices d’aération de votre produit Sun. Ne placez jamais un produit Sun à proximité d’un radiateur ou d'une source de chaleur. Tout manquement à ces consignes peut entraîner une surchauffe de votre produit Sun, qui risque de nuire à sa fiabilité.

Attention – Le niveau de bruit électronique inhérent au lieu de travail, tel qu’il est défini par la norme DIN 45 635 – section 1000, doit être inférieur ou égal à 70Db(A).

Conformité aux normes SELV

Le niveau de sécurité des connexions E / S est conforme aux normes SELV.

Raccordement à la source d’alimentation électrique

Attention – Les produits Sun sont conçus pour être exploités avec des systèmes d’alimentation électrique monophasés avec prise de terre. Pour réduire le risque de décharge électrique, ne branchez jamais les produits Sun sur une source d’alimentation d'un autre type. Contactez le gérant de votre immeuble ou un électricien certifié si vous avez le moindre doute quant au type d’alimentation électrique fourni dans votre immeuble.

Attention – Tous les cordons d’alimentation n’ont pas la même intensité nominale. Les cordons d’alimentation d’usage domestique ne sont pas protégés contre les surtensions et ne sont pas conçus pour être utilisés avec des ordinateurs. N’utilisez jamais de cordon d’alimentation d’usage domestique avec votre produit Sun.

Attention – Votre produit Sun est livré avec un cordon d’alimentation avec raccord à la terre (à trois broches). Pour réduire le risque de décharge électrique, branchez toujours ce cordon sur une source d'alimentation électrique avec prise de terre.

Pile au lithium

Attention – Ce système est équipé d’une pile au lithium qui peut être remplacée, référence n° 150-2850. Les piles au lithium risquent d’exploser en cas de manipulation maladroite. Ne jetez en aucun cas la pile au feu. N’essayez en aucun cas de la démonter, ni de la recharger.

Couvercle du système

Vous devrez retirer le couvercle de votre ordinateur Sun pour ajouter des cartes, de la mémoire ou des unités de stockage internes. Veillez toujours à réinstaller le couvercle de l’ordinateur avant de le remettre sous tension.

Attention – Ne travaillez jamais avec un produit Sun sans en avoir réinstallé le couvercle. Tout manquement à cette mesure de sécurité risque d’endommager votre système et de provoquer des blessures physiques personnelles.

Avis de conformité des appareils laser

Les produits Sun qui mettent en oeuvre la technologie du laser sont conformes aux normes de sécurité des appareils laser de la classe 1.

Class 1 Laser Product
Luokan 1 Laserlaite
Klasse 1 Laser Apparat
Laser KLasse 1

Lecteur de CD-ROM ou de DVD-ROM

Attention – Tout usage des dispositifs de contrôle, tout réglage, ou toute exécution de procédures autres que ceux spécifiés dans ce document risque d’entraîner une exposition à des radiations potentiellement néfastes.

Einhaltung sicherheitsbehördlicher Vorschriften

Lesen Sie diesen Abschnitt sorgfältig durch, bevor Sie eine Installation vornehmen. Der folgende Text beschreibt die bei der Installation von Sun Microsystems-Geräten zu befolgenden Sicherheitsmaßnahmen.

Sicherheitsmaßnahmen

Zu Ihrem eigenen Schutz sollten Sie die folgenden Sicherheitsmaßnahmen bei der Installation befolgen:

- Befolgen Sie alle auf die Geräte aufgedruckten Anweisungen und Warnhinweise.
- Beachten Sie die Geräteaufschrift, um sicherzustellen, daß Netzspannung und -frequenz mit der Gerätespannung und –frequenz übereinstimmen.
- Führen Sie niemals Gegenstände in die Geräteöffnungen. Es könnten elektrische Spannungsfelder vorhanden sein. Leitende Fremdgegenstände können Kurzschlüsse, elektrische Schläge oder Feuer verursachen und somit Ihr Gerät beschädigen.

Symbole

Die folgenden Symbole werden in diesem Handbuch verwendet:

Achtung – Es besteht die Gefahr der Verletzung und der Beschädigung des Geräts. Befolgen Sie die Anweisungen.

Achtung – Heiße Oberfläche. Vermeiden Sie jede Berührung. Diese Oberflächen sind sehr heiß und können Verbrennungen verursachen.

Achtung – Elektrisches Spannungsfeld vorhanden. Befolgen Sie bitte die Anweisungen, um elektrische Schläge und Verletzungen zu vermeiden.

Modifikationen des Geräts

Nehmen Sie keine elektrischen oder mechanischen Gerätemodifikationen vor. Sun Microsystems ist für die Einhaltung der Sicherheitsvorschriften von modifizierten Sun-Produkten nicht haftbar.

Aufstellung der Sun-Geräte

Achtung – Blockieren und decken Sie nie die Öffnungen Ihres Sun-Geräts ab. Setzen Sie das Gerät nie direkter Sonnenbestrahlung aus, und stellen Sie es nicht in der Nähe eines Heizkörpers auf. Bei Nichtbeachtung dieser Empfehlungen kann das Gerät überhitzen und die Funktionstüchtigkeit beeinträchtigt werden.

Achtung – Der Geräuschpegel, definiert nach DIN 45 635 Part 1000, darf am Arbeitsplatz nicht 70Db(A) überschreiten.

SELV-Richtlinien

Alle Ein-/Ausgänge erfüllen die SELV-Anforderungen.

Netzanschlußkabel

Achtung – Sun-Geräte benötigen ein einphasiges Stromversorgungssystem mit eingebautem Erdleiter. Schließen Sie Sun-Geräte nie an ein anderes Stromversorgungsystem an, um elektrische Schläge zu vermeiden. Falls Sie die Spezifikationen der Gebäudestromversorgung nicht kennen, sollten Sie den Gebäudeverwalter oder einen qualifizierten Elektriker konsultieren.

Achtung – Nicht alle Netzanschlußkabel besitzen die gleiche Spannungsleistung. Normale Verlängerungskabel besitzen keinen Überstromschutz und sind nicht für Computersysteme geeignet. Benutzen Sie keine Haushaltverlängerungskabel für Sun-Geräte.

Achtung – Ihr Sun-Gerät wurde mit einem geerdeten (dreiadrigen) Netzanschlußkabel geliefert. Stecken Sie dieses Kabel immer nur in eine geerdete Netzsteckdose, um Kurzschlüsse zu vermeiden.

Lithium-Batterie

Achtung – Dieses System enthält eine austauschbare Lithiumbatterie, Teilenummer 150-2850. Die Batterien können bei falscher Handhabung explodieren. Entsorgen Sie die Batterien nicht im Feuer. Die Batterien dürfen nicht auseinandergenommen oder wieder aufgeladen werden.

Abdeckung des Systems

Sie müssen die Abdeckung des Sun-Computers entfernen, um zusätzliche Karten, Speichermodule oder interne Speicherlaufwerke einzubauen. Bevor Sie das System einschalten, müssen Sie die Abdeckung wieder anbringen.

Achtung – Sun-Geräte dürfen nicht ohne Abdeckung in Gebrauch genommen werden. Nichtbeachtung dieses Warnhinweis kann Verletzungen oder Systembeschädigungen zur Folge haben.

Laserrichtlinien

Alle Sun-Produkte, die Lasertechnologie nutzen, erfüllen die Laserrichtlinien der Klasse 1.

Class 1 Laser Product
Luokan 1 Laserlaite
Klasse 1 Laser Apparat
Laser KLasse 1

CD-ROM oder DVD-ROM

Achtung – Der Einsatz von in diesen Anleitungen nicht ausdrücklich enthaltenen Einstellungen, Änderungen oder Prozeduren kann zu Strahlungsschäden führen.

Conformità alle norme di sicurezza

Leggere questa sezione prima di iniziare qualsiasi procedura. Il testo seguente fornisce delle precauzioni di sicurezza da seguire quando si installa un prodotto della Sun Microsystems.

Precauzioni di sicurezza

Per protezione personale, seguire le precauzioni di sicurezza seguenti quando installa l'attrezzatura:

- Seguire tutte le avvertenze e le istruzioni indicate sull'attrezzatura.
- Accertarsi che la tensione e la frequenza della fonte di alimentazione elettrica utilizzata corrispondano alla tensione e frequenza indicata sull'etichetta presente sull'attrezzatura.
- Non inserire mai oggetti di qualsiasi natura attraverso le aperture dell'attrezzatura. Possono essere presenti delle tensioni pericolose. Degli oggetti esterni potrebbero causare un cortocircuito che può a sua volta causare un incendio, una scossa elettrica o danni all'attrezzatura.

Simboli

I simboli seguenti possono apparire in questa pubblicazione:

Attenzione – Esiste il rischio di lesioni personali e danni all'attrezzatura. Seguire le istruzioni.

Attenzione – Superficie calda. Evitare il contatto. Le superfici sono calde e possono ferirla se sono toccate.

Attenzione – Sono presenti tensioni pericolose. Per ridurre il rischio di scosse elettriche e pericoli per la propria salute, seguire le istruzioni.

Modifiche all'attrezzatura

Non apportare nessuna modifica meccanica o elettrica all'attrezzatura. La Sun Microsystems non è responsabile della conformità alle leggi in vigore di un prodotto Sun modificato.

Normativas de seguridad

Antes de comenzar cualquier procedimiento, lea esta sección. El texto que sigue explica medidas de seguridad a seguir al instalar un producto de Sun Microsystems.

Medidas de precaución

Para su propia seguridad, observe las siguientes medidas de precaución al instalar y configurar su equipo:

- Siga todas las medidas de precaución e instrucciones marcadas en el equipo.
- Cerciórese de que el voltaje y la frecuencia de su fuente de alimentación coinciden con el voltaje y la frecuencia indicada en la etiqueta de clasificación eléctrica del equipo.
- Nunca introduzca objeto alguno a través de las aberturas del equipo. Dentro puede haber voltajes peligrosos. Los objetos extraños conductores podrían producir un cortocircuito que podría provocar fuego, un shock eléctrico o daños a su equipo.

Símbolos

Los siguientes símbolos pueden aparecer en este libro:

Precaución – Existe el riesgo de provocar lesiones personales y daños al equipo. Siga las instrucciones.

Precaución – Superficie caliente. Evite el contacto. Las superficies están calientes y pueden causar lesiones personales al tocarlas.

Precaución – Voltaje peligroso presente. Para reducir el riesgo de shock eléctrico y de dañar su salud personal, siga las instrucciones.

Modificaciones al equipo

No realice modificaciones mecánicas o eléctricas al equipo. Sun Microsystems no se hará responsable del cumplimiento de las normas en el caso de un producto Sun que ha sido modificado.

Lugar y posición de un producto Sun

Precaución – No obstruya ni cubra las aberturas de su producto Sun. Nunca coloque un producto Sun junto a un radiador o un medidor de calor. La falta de cumplimiento con estas pautas puede provocar el recalentamiento de su equipo Sun y afectar la confiabilidad del mismo.

Precaución – Según se define en DIN 45 635, Parte 1000, el nivel de ruido que afecta al lugar de trabajo debe ser de 70Db(A) o menos.

Cumplimiento con normas SELV

El estado de seguridad de conexiones de E/S satisfacen los requerimientos de las normas SELV.

Conexión del cable de alimentación

Precaución – Los productos Sun han sido diseñados para trabajar con sistemas de alimentación monofásicos que tengan un conductor neutral a tierra. Para reducir el riesgo de shock eléctrico, no enchufe ningún producto Sun en ningún otro tipo de sistema de alimentación. Si no está seguro del tipo de alimentación del que dispone su edificio, comuníquese con la persona correspondiente o con un electricista calificado.

Precaución – No todos los cables de alimentación tienen la misma clasificación en cuanto a corriente eléctrica. Los cables de prolongación caseros no ofrecen protección contra sobrecargas y no están diseñados para ser utilizados con computadoras. No utilice cables de prolongación caseros con su producto Sun.

Precaución – Su producto Sun trae un cable de alimentación de tres hilos de conexión a tierra. Para reducir el riesgo de shock eléctrico, enchufe siempre el cable a una toma de corriente con conexión a tierra.

Batería de litio

Precaución – Este sistema contiene una batería de litio reemplazable, número de pieza 150-2850. Estas baterías pueden explotar si se las manipula incorrectamente. No tire baterías al fuego. No las desarme ni intente recargarlas.

Cubierta de la unidad del sistema

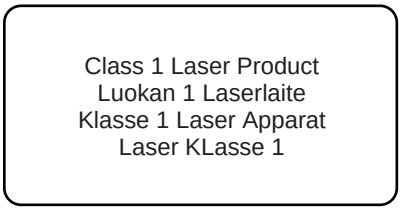
Es necesario retirar la cubierta de la unidad de su sistema Sun para poder añadir tarjetas, memoria o dispositivos internos de almacenamiento. Asegúrese de volver a colocar la cubierta antes de encender el sistema.

Precaución – No haga funcionar su producto Sun sin que la cubierta se encuentre en su lugar. De lo contrario, podrían producirse lesiones personales o daños al sistema.

Aviso de cumplimiento de las normas

para láser

Los productos Sun que utilizan tecnología láser satisfacen los requerimientos para láser de Clase 1.



GOST-R Certification Mark

CD-ROM o DVD-ROM

Precaución – El uso de controles, ajustes o la realización de procedimientos diferentes de los que se especifican aquí pueden resultar en exposición peligrosa a radiaciones.GOST-R Certification Mark

Nordic Lithium Battery Cautions

Norge

ADVARSEL – Litiumbatteri — Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

Danmark

ADVARSEL! – Litiumbatteri — Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

Suomi

VAROITUS – Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

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Figures

Tables

Preface

The *Sun Blade 1000 Service Manual* provides detailed procedures that describe the removal and replacement of components of the Sun Blade™ 1000 computer (the system). The service manual also includes information about the use and maintenance of the system. This book is written for technicians, system administrators, authorized service providers (ASPs), and advanced computer system end users who have experience in troubleshooting systems and replacing hardware.

About the Multimedia Links in this Manual

Removal and replacement procedures for selected system components are illustrated with interactive multimedia audio and video instructions in the Sun Blade 1000 ShowMe How multimedia documentation. This multimedia documentation is linked to the online version of this service manual. If necessary, when performing service procedures view any or all of the ShowMe How video clips located on the Sun Blade 1000 Hardware Documentation CD-ROM.

How This Book Is Organized

This document is organized into chapters and appendixes as follows. A glossary and index are included.

Chapter 1 describes the major components of the system.

Chapter 2 describes the execution of individual tests to verify hardware configuration and functionality.

Chapter 3 describes the execution of POST and provides examples of POST output patterns.

Chapter 4 provides troubleshooting advice and suggested corrective actions for hardware problems.

Chapter 5 explains how to prepare for removal and replacement of system components.

Chapter 6 provides step-by-step procedures for removing and replacing major subassemblies.

Chapter 7 provides step-by-step procedures for removing and replacing storage devices.

Chapter 8 provides step-by-step procedures for removing and replacing the motherboard and various components associated with motherboard operation.

Chapter 9 explains how to restore the system after replacing components.

Chapter 10 explains the OpenBoot Emergency Procedures for standard (non-USB) keyboards and for USB type keyboards.

Appendix A provides product specifications, system requirements about power and environment, system dimensions, weight, memory mapping, and PCI card slot specifications.

Appendix B provides signal descriptions and connector pin assignments.

Appendix C provides a functional description of the system.

Appendix D is a USB supplement that describes the interaction of the USB mouse and keyboard with the system.

UNIX Commands

This document may not contain information on basic UNIX® commands and procedures such as shutting down the system, booting the system, and configuring devices.

See one or more of the following for this information:

- *Solaris Handbook for Sun Peripherals*
- AnswerBook2™ online documentation for the Solaris™ software environment

- Other software documentation that you received with your system

Typographic Conventions

TABLE P-1 Typographic Conventions

Typeface or Symbol	Meaning	Examples
`AaBbCc123`	The names of commands, files, and directories; on-screen computer output.	Edit your `.login` file. Use `ls -a` to list all files. `% You have mail.`
`AaBbCc123`	What you type, when contrasted with on-screen computer output.	`% su` `Password:`
AaBbCc123	Book titles, new words or terms, words to be emphasized. Command-line variable; replace with a real name or value.	Read Chapter 6 in the *User's Guide*. These are called *class* options. You *must* be `root` to do this. To delete a file, type `rm` *filename*.

Shell Prompts

TABLE P-2 Shell Prompts

Shell	Prompt
C shell	*machine_name*%
C shell superuser	*machine_name*#
Bourne shell and Korn shell	$
Bourne shell and Korn shell superuser	#

Related Documentation

TABLE P-3 Related Documentation

Application	Title	Part Number
Configuration	*Solaris Handbook for Sun Peripherals*	805-7404
Configuration	*Solaris x.x Sun Hardware Platform Guide*	[1]
Diagnostics	*SunVTS™ 4.x User's Guide*	[1]
Diagnostics	*SunVTS 4.x Quick Reference Card*	[1]
Diagnostics	*SunVTS 4.x Test Reference Manual*	[1]
Installation	*14-Gbyte, 8-mm Tape Drive Installation Manual*	802-1849
Installation	*Elite3D Installation Guide*	805-4391
Installation	*Creator Frame Buffer Installation Guide*	802-6682
Installation	*Sun PGX32™ PCI Graphics Card Installation Guide*	805-7770
Installation / User	*12-24 Gbyte 4-mm DDS-3 Tape Drive Installation and User's Guide*	802-7791

TABLE P-3 Related Documentation *(Continued)*

Application	Title	Part Number
Installation	*Sun Blade 1000 Rackmount Installation Guide*	805-7959
Installation / user	*Sun StorEdge™ CD32 Installation and User's Guide*	805-4237
Specification	*Manual Eject Diskette Drive Specifications*	805-1133
Specification	*18 GB 10K rpm Disk Drive Specifications*	806-1057
Specification	*36 GB 10K rpm Disk Drive Specifications*	
Specification	*8-mm Tape Drive Specifications*	802-5775
Specification	*4-mm, DDS-2 Tape Drive Specifications*	802-7790
User	*21-Inch Premium (19.8-inch Viewable) Color Monitor Guide*	875-1844
User	*24-Inch Premium (22.5-inch Viewable) Color Monitor Guide*	875-1799
User	*14-Gbyte, 8-mm Tape Drive User's Guide*	802-1850

1. Dependent upon the version of Solaris in your system.

Ordering Sun Documentation

Fatbrain.com, an Internet professional bookstore, stocks select product documentation from Sun Microsystems™, Inc.

For a list of documents and how to order them, visit the Sun Documentation Center on Fatbrain.com at:

`http://www1.fatbrain.com/documentation/sun`

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docfeedback@sun.com

Please include the part number (805-4496-10 Revision A) of your document in the subject line of your e-mail.

CHAPTER 1

Product Description

This chapter contains an overview of the Sun Blade™ 1000 system including features, an illustration of the system, front and rear panel descriptions.

1.1 Product Overview

The Sun Blade 1000 workstation is a dual processor workstation that uses the UltraSPARC™ III family of processors. The workstation offers super-scalar processor technology, multiprocessing, high-performance memory interconnection, high-bandwidth input/output (I/O), and accelerated graphics.

The Sun Blade 1000 workstation electronics and peripherals contain, or may be upgraded to contain, the following features:

- Processors:
  - One or two UltraSPARC-III processor modules with either 4 megabytes (Mbytes) or 8 Mbytes of external cache
- Main memory:
  - 8 DIMM slots
  - Up to 8 Gbytes of main memory with stacked DRAM technology and 3.3-VDC SDRAM chips
- I/O extensions:
  - 2 UPA64S slots for frame buffers; supporting two Creator 3D Series 3 (single buffer or double buffer), two Elite 3D m3, or two Elite 3D m6 graphics cards.

- Four 64-bit peripheral component interconnect (PCI) slots.

Note – Three of the four long PCI slots at operate at 33 MHz and one of the four long PCI slots operates at 66 MHz.

  - Audio module (line-in, line-out, mic, headset, and speaker) chips
- Internal peripherals:
  - Two Fibre Channel-Arbitrated Loop (FC-AL) internal 3.5-inch hard drives (10,000 RPM) with an external FC-AL copper connector for expansion
  - 3.5-inch, 1.4-Mbyte, triple-density, manual-eject, diskette drive
  - Smart card reader (future support)
  - 1.6-inch bay for DVD-ROM drive, or tape drive with SCSI interface
- Rear Panel:
  - Ethernet 10BASE-T/100BASE-T twisted-pair connector
  - FC-AL copper connector for mass storage extension
  - Ultra wide SCSI connector
  - Four universal serial bus (USB) connectors for input devices up to 12 Mbits per second
  - Two IEEE 1394 serial bus connectors. Up to 400 Mbits per second
  - One Parallel port, DB25 connector
  - Two RS-232C/RS423 serial ports, 384 K Baud rate synchronous, 460.8 K Baud rate asynchronous
- Enclosure:
  - Custom tower

The Sun Blade 1000 system features include:

- Power and cooling requirements for a high-performance processor
- Modular internal design
- Improved disk, system, memory, and I/O performance and capacities
- High-performance PCI I/O expansion

The following illustrations show the system view and the front and back panels of the Sun Blade 1000 system.

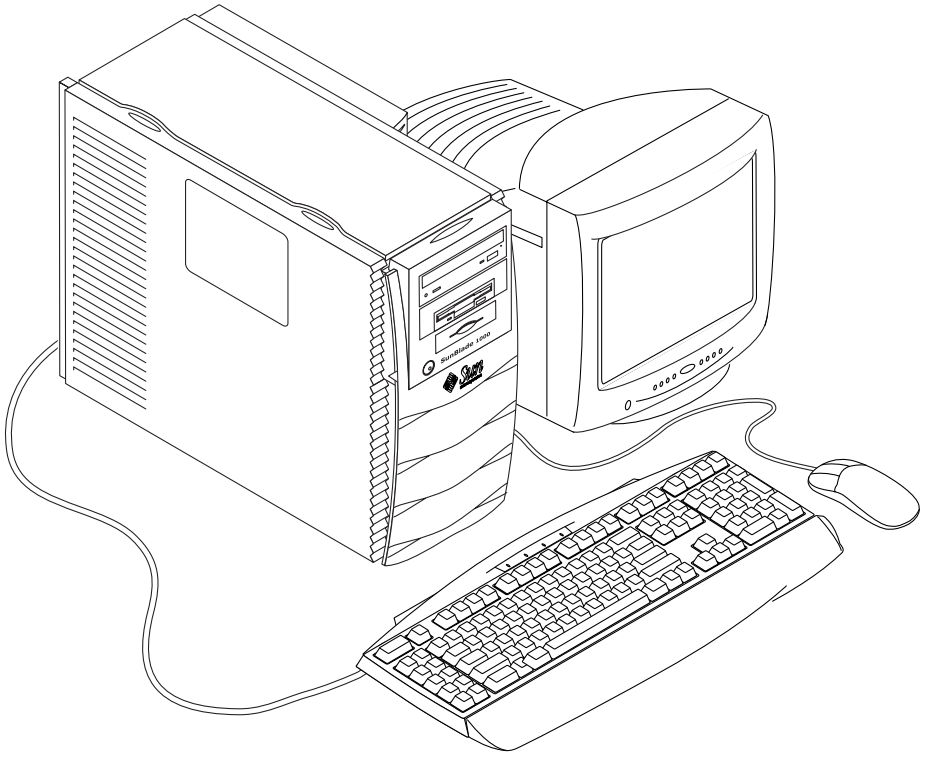

FIGURE 1-1 Sun Blade 1000 Workstation

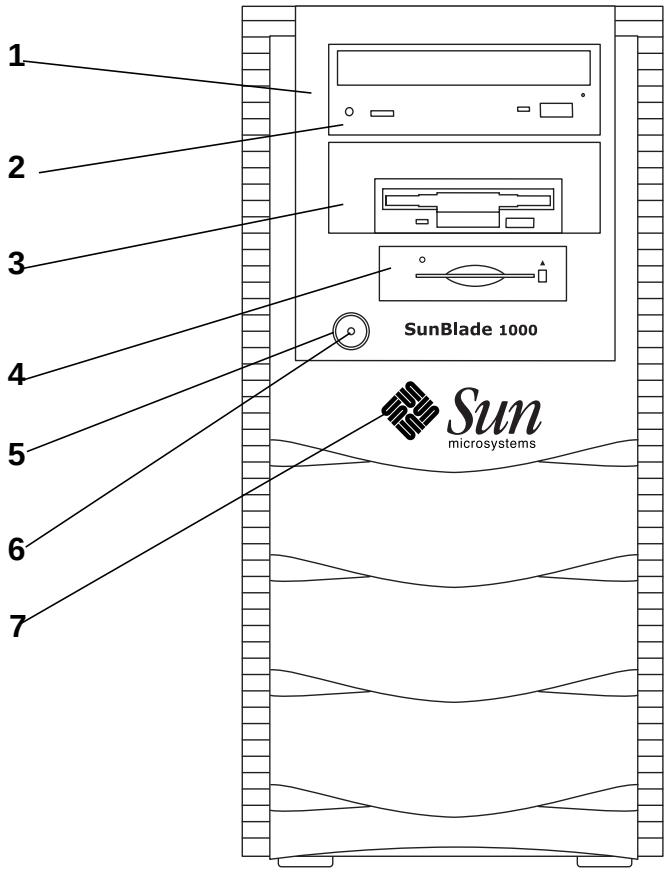

FIGURE 1-2 Front Panel Overview

1. Peripheral bezel
2. 5.25-inch drive bay (optional DVD-ROM drive shown)
3. 5.25- or 3.5-inch drive bay (optional diskette drive shown)
4. Smart card reader (future support)
5. Power switch
6. Power indicator LED
7. Back-lit Sun logo

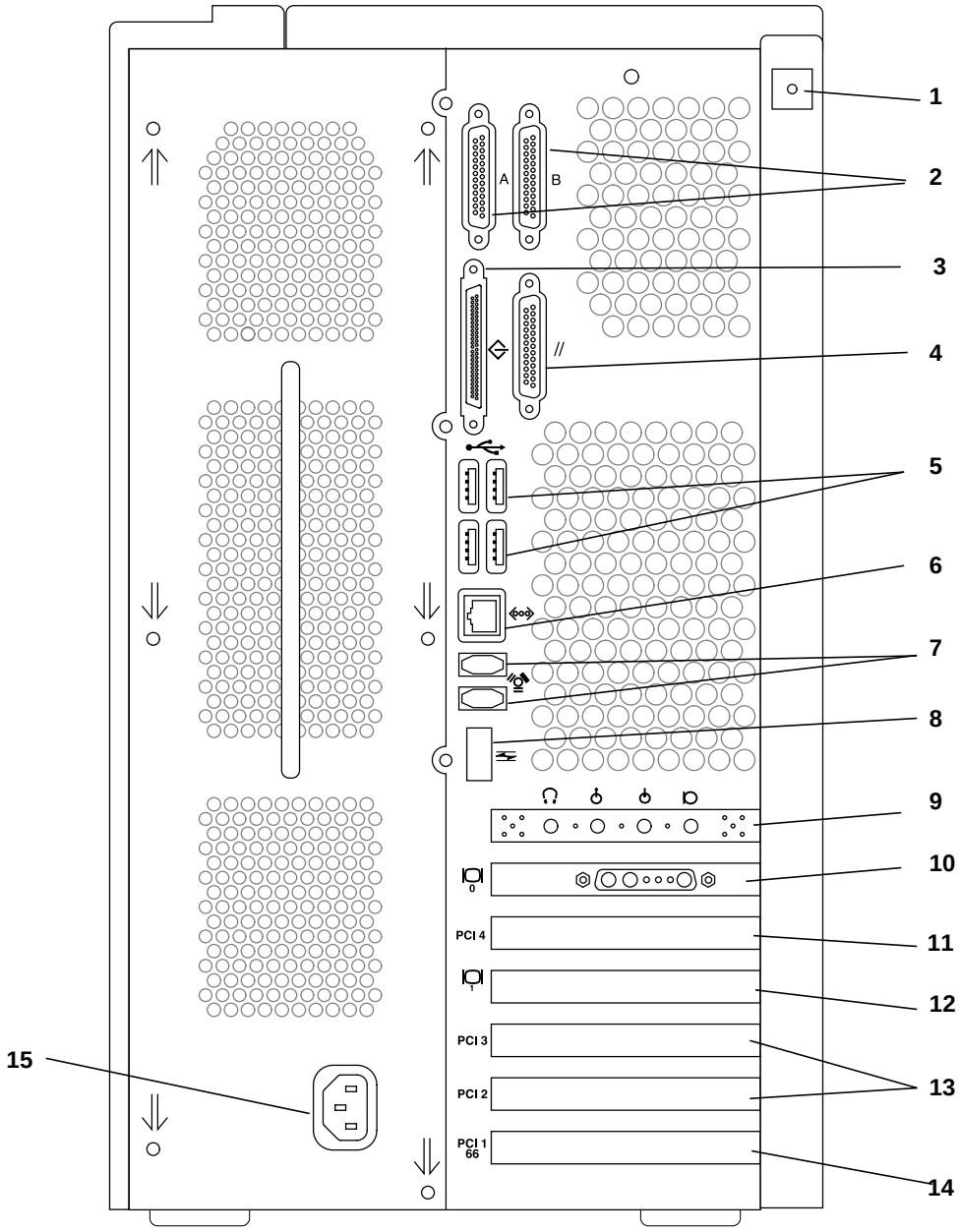

FIGURE 1-3 Back Panel Overview

TABLE 1-1 Back Panel Overview

Item in Figure 3	Explanation	Back Panel Symbol
1	Access panel lock block	None
2	Serial connectors A and B, DB-25 (can support RS-423 and RS-232 protocols)	A B
3	SCSI connector (Ultra SCSI, 68-pin)	
4	Parallel connector, DB-25	//
5	Universal serial bus (USB) connectors	
6	Twisted-pair Ethernet (TPE) connector	
7	IEEE 1394 connectors	
8	Fibre Channel-Arbitrated Loop (FC-AL) connector	
9	Audio module headphones connector	
9	Audio module line-in connector	
9	Audio module line-out connector	
9	Audio module microphone connector	
10	Graphics card / video connector (frame buffer 0)	
11	PCI card slot 4 (33 MHz)	PCI 4
12	Graphics card / video connector (frame buffer 1)	
13	PCI card slot 3 (33 MHz)	PCI 3
13	PCI card slot 2 (33 MHz)	PCI 2
14	PCI card slot 1 (66 MHz)	PCI 1 66
15	Power connector	None

1.2 Replaceable Components

This section lists the authorized replaceable parts for the system. FIGURE 1-4 illustrates an exploded view of the system. TABLE 1-2 on page 1-9 lists the system replaceable components. A brief description of each listed component is also provided.

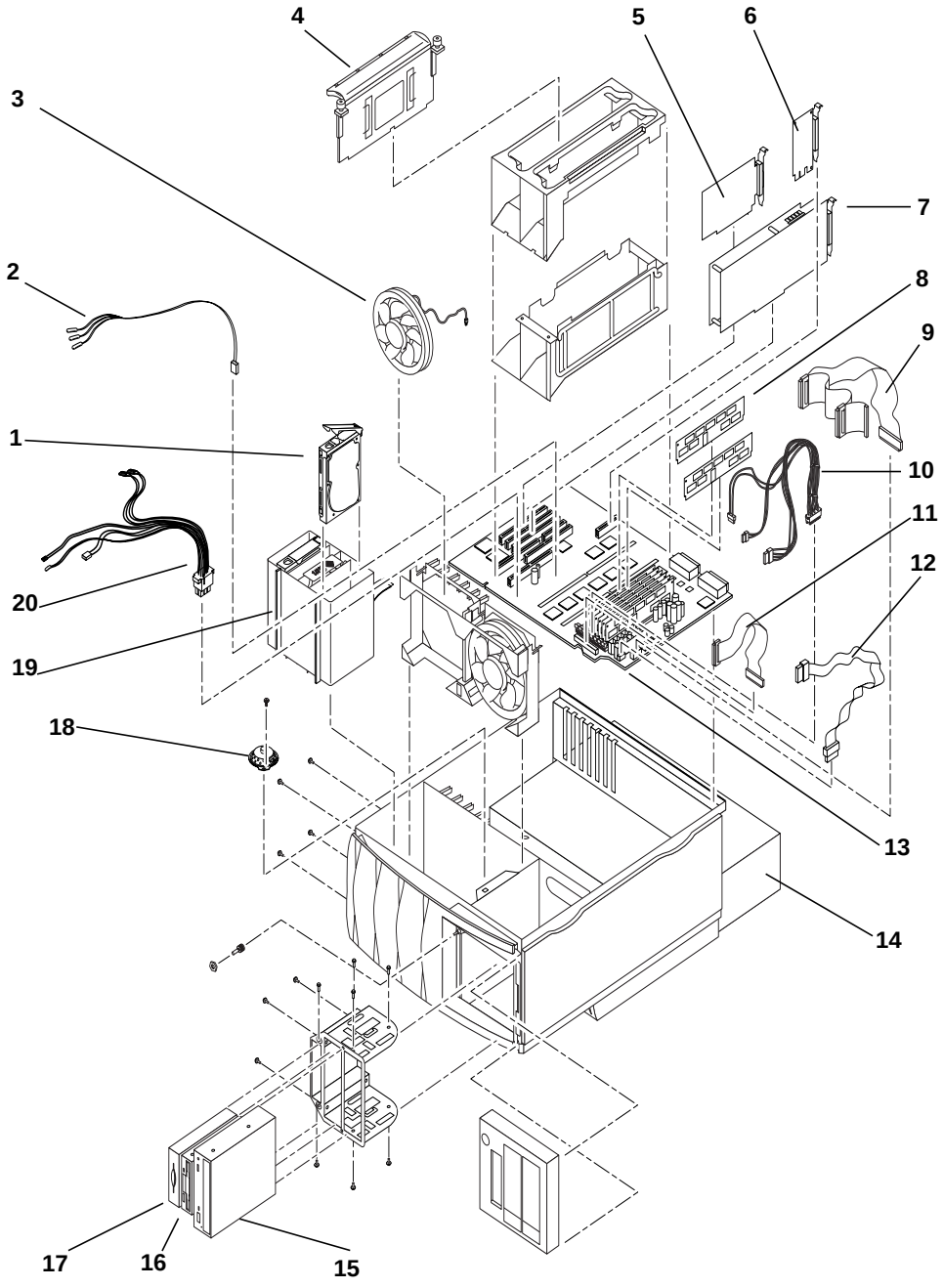

FIGURE 1-4 System Exploded View

Note – The replaceable components listed in the following table are correct as of the service manual publication date but are subject to change without notice. Consult your authorized Sun sales representative or service provider to confirm a part number prior to ordering a replacement part.

TABLE 1-2 Replaceable Components

Ref. No.	Component	Description
1	Hard drive, 18 GB[1]	18-GB, 10000 RPM hard drive
1	Hard drive, 36 GB[1]	36-GB, 10000 RPM hard drive
2	Logo LED cable assembly	Cable for logo LED
3	Fan	12 VDC variable speed fan
4	600 MHz/4 MB CPU module[1]	600-MHz UltraSPARC-III CPU module
4	750 MHz/8 MB CPU module[1]	750-MHz UltraSPARC III CPU module
5	PCI card[1]	PGX32™ 24-bit PCI card
6	Audio module assembly	Audio applications, 16-bit audio, 8 Hz to 48 kHz
7	Graphics card[1]	Creator 3D Series 3 graphics card
7	Graphics card[1]	Expert 3D graphics card
7	m3 graphics card[1]	Elite 3D m3 graphics card
7	m6 graphics card[1]	Elite 3D m6 graphics card
8	128-Mbyte DIMM[1]	128-Mbyte DIMM
8	256-Mbyte DIMM[1]	256-Mbyte DIMM
8	1-GB DIMM[1]	1-GB DIMM
9	SCSI cable assembly	Internal SCSI cable for removable bay
10	Peripheral power cable assembly	DC power cable assembly
11	Diskette drive cable assembly[1]	Diskette drive cable assembly
12	Smart card cable	20 inch, 10-pin, I2C cable
13	Motherboard assembly	System board

TABLE 1-2 Replaceable Components *(Continued)*

Ref. No.	Component	Description
14	Power supply assembly	Power supply, 670 watts
15	DVD-ROM drive[1]	DVD-ROM drive
16	Manual eject floppy assembly[1]	Diskette drive
17	Smart card reader (future support)	Smart card reader assembly (future support)
18	Speaker assembly	16-ohm speaker
19	FC-AL backplane assembly	Provides interface between hard drive(s) and motherboard
20	Combined cable assembly	Cable harness for the power switch, interlock, power indicator LED and speaker
Not illustrated	SEEPROM	With carrier and bar code
Not illustrated	Shroud cover, CPU	
Not illustrated	FC-AL backplane assembly	Includes FC-AL cable
Not illustrated	FC-AL cage assembly	Drive cage, backplane and cable
Not illustrated	Lithium battery	Provides voltage for TOD and ID SEEPROM
Not illustrated	Power switch	Provides main power to system
Not illustrated	Interlock switch	Provides power interlock
Not illustrated	Chassis feet	Kit, 5 per box (part of #560-2525, Ultra™ 30/60/80 accessory kit)
Not illustrated	TPE cable (category 5)	Twisted-pair Ethernet cable
Not illustrated	PCI filler panel	PCI filler panel (part of #560-2525, Ultra 30/60/80 accessory kit)

1. These are optional components. They may or may not be part of your system.

CHAPTER 2

SunVTS Overview

This chapter contains an overview of the SunVTS™ diagnostic tool. Use SunVTS to validate a system during development, production, receiving inspection, troubleshooting, periodic maintenance, and system or subsystem stressing.

This chapter contains the following topics:

2.1 SunVTS Description

SunVTS is the Sun online Validation Test Suite. SunVTS is a comprehensive software diagnostic package that tests and validates hardware by verifying the connectivity and functionality of most hardware controllers, devices, and platforms.

SunVTS can be tailored to run on various types of systems ranging from desktops to servers with many customizable features to meet the varying requirements of many diagnostic situations.

SunVTS executes multiple diagnostic tests from one graphical user interface (GUI) that provides test configuration and status monitoring. The user interface can run in the CDE or OPEN LOOK environments or through a TTY-mode interface for situations when running a GUI is not possible.

The SunVTS interface can run on one system to display the SunVTS test session of another system on the network.

SunVTS is distributed with each SPARC™ Solaris™ release. It is located on the Sun Computer Systems Supplement CD.

2.1.1 SunVTS Requirements

Your system must meet the following requirements to run SunVTS:

- The SunVTS packages must be installed. The main package is `SUNWvts`. There are additional supporting packages that differ based on the revision of the Solaris operating system that is installed. For specific details, refer to the corresponding SunVTS documentation.
- The system must be booted to the multiuser level (level 3).
- To run SunVTS with a GUI, that GUI must be installed. Otherwise, run SunVTS with the TTY-mode interface.

2.1.2 SunVTS References

To find out more information about the using SunVTS, refer to the SunVTS documentation that corresponds to the Solaris release that you are running.

The SunVTS documents are part of the Solaris on Sun Hardware AnswerBook™ collection. This AnswerBook collection is pre installed on the hard disk of new systems. It is also distributed on the Software Supplement CD that is part of each Solaris Media Kit release and is also accessible at `http://docs.sun.com`.

The following list describes the contents of each SunVTS document:

- *SunVTS User's Guide* describes how to install, configure, and run the SunVTS diagnostic software.
- *SunVTS Quick Reference Card* provides an overview of how to use the SunVTS CDE interface.
- *SunVTS Test Reference Manual* provides details about each individual SunVTS test.

CHAPTER 3

Power-On Self-Test

This chapter describes how to initiate power-on self-test (POST) diagnostics. POST is a firmware program that is useful in determining if a portion of the system has failed. POST verifies the core functionality of the system, including the CPU module(s), motherboard, memory, and some on-board I/O devices. POST can be run even if the system is unable to boot.

This chapter contains the following topics:

3.1 POST Overview

POST detects most system faults and is located in the system board OpenBoot™ PROM. POST will be invoked optionally at power up by the OpenBoot program, depending on the setting of two environment variables, the `diag-switch?` and the `diag-level` flag, which are stored in nonvolatile RAM (NVRAM).

POST diagnostic and error message reports are displayed on a console terminal.
How to Use POST

When the system power is applied, POST runs automatically if both of the following conditions apply:

- The `diag-switch?` NVRAM parameter is set to `true`.
- The `diag-level` is set to `min` or `max`.

In the event of an automatic system reset, POST runs if the `diag-switch?` NVRAM parameter is set to `true` and the `diag-level` flag is set to either `max` or `min`.

Note – If the `diag-switch` = false, POST is disabled. If `diag-switch` = true and `diag-level` = `max`, then POST runs in `max` mode. If `diag-switch` = true and diag-level = `min`, then POST runs in `min` mode.

3.2 Pre-POST Preparation

Pre-POST preparation includes:

- Setting up a terminal interface processor (TIP) connection to another system or terminal to view POST progress and error messages. See Section 3.2.1 “Setting Up a TIP Connection” on page 3-2.
- Verifying baud rates between a system and a monitor or a system and a terminal. See Section 3.2.2 “Verifying the Baud Rate” on page 3-3.

3.2.1 Setting Up a TIP Connection

A TIP connection enables a remote terminal window to be used as a terminal to display test data from a system. Serial port A of a tested system is used to establish the TIP connection between the system being tested and another Sun system monitor or TTY-type terminal. The TIP connection is used in a terminal window and provides features to help with the OpenBoot program.

To set up a TIP connection:

1. **Connect serial port A of the system being tested to serial port B of another Sun system using a serial null modem cable (connect cable pins 2-3, 3-2, 7-20, and 20-7).**

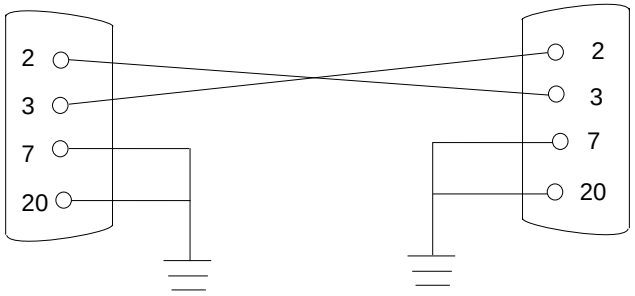

FIGURE 3-1 Setting Up a TIP Connection

2. **At the other Sun system, check the** `/etc/remote` **file by changing to the** `/etc` **directory and then editing the** `remote` **file:**

```
hardwire:\ dv=/dev/term/b:br#9600:el=^C^S^Q^U^D:ie=%$:oe=^D:
```

Note – The example shows connection to serial port B of the other Sun system.

---

3. **To use serial port A instead:**

   a. **Modify the /etc/**`remote` **file as follows:**

```
hardwire:\ dv=/dev/term/a:br#9600:el=^C^S^Q^U^D:ie=%$:oe=^D:
```

4. **In a shell window on the Sun system, type** `tip hardwire`**.**

```
hostname% tip hardwire
connected
```

Note – The shell window is now a TIP window directed to the serial port of the system being tested. When power is applied to the system being tested, POST messages will be displayed in this window.

---

5. **When POST is completed, disconnect the TIP window as follows:**

   a. **Open a shell window.**

   b. **Type** `ps -a` **to view the active TIP line and process ID (PID) number.**

   c. **Type the following to kill the TIP hardwire process.**

```
% kill -9 PID#
```

3.2.2 Verifying the Baud Rate

To verify the baud rate between the system being tested and a terminal or another Sun system monitor:

1. **Open a shell window.**

2. **Type** `eeprom`

3. **Verify the following serial port default settings as follows:**

```
ttyb-mode = 9600,8,n,1
ttya-mode = 9600,8,n,1
```

Note – Ensure that the settings are consistent with TTY-type terminal or system monitor settings.

3.3 Setup to run POST in an OBP environment

To run POST perform the following procedure:

- Set the `diag-switch?` to `true` and the `diag-level` to `max` or `min`.
- Power cycle the system.

Note – The default setting is `max`. See `Section 3.4 "Maximum and Minimum Levels of POST"` below to set POST to the `min` mode.

To set the `diag-switch?` to `true`:

1. **At the system prompt, type:**

```
ok setenv diag-switch? true
ok setenv diag-level = min, max, menus
```

Note – At the system prompt, type: `ok` **setenv diag-level** = "min" or "max" or "menus" Do not type "min", "max" and "menus".

2. **Press the power switch briefly to power cycle the system.**

3.4 Maximum and Minimum Levels of POST

Two levels of POST are available: maximum (`max`) level and minimum (`min`) level. The system initiates the selected level of POST based on the setting of `diag-level`, an NVRAM variable.

Various CPU configurations coupled with the amount of installed memory affect the amount of time required to complete the POST. The following table lists the approximate amount of time required to complete the POST with 2.5 GB of DIMM installed for the `diag-level` variable set to `max` and the `diag-level` variable set to `min` with regard to the various CPU configurations.

TABLE 3-1 POST Completion Times

CPU Configuration	`max` setting	`min` setting
2-way	3.5 minutes	3 minutes
Single	1.5 minutes	1.3 minutes

The default setting for `diag-level` is `max`. Examples of the `max`-level POST output on serial port A is provided in Section 3.4.1 “diag-level Variable Set to max”. Examples of the `min`-level POST output on serial port A is provided in Section 3.4.2 “diag-level Variable Set to min” on page 3-30.

To set the `diag-level` variable to `min`, type:

```
ok setenv diag-level min
```

To return to the default setting type:

```
ok setenv diag-level max
```

3.4.1 `diag-level` Variable Set to `max`

When the `diag-level` variable is set to `max`, POST enables an extended set of diagnostic-level tests. The following code examples identify typical serial port A POST output with the `diag-level` variable set to `max` for 2-way and single CPU configurations:

- `diag-level` variable set to `max` (2-way CPU) — CODE EXAMPLE 3-1 on page 3-7
- `diag-level` variable set to `max` (single CPU) — CODE EXAMPLE 3-2 on page 3-22

Note – The following POST examples are executed with 750-MHz CPUs and 512-MB of memory.

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(1 of 15)*

```
@(#)  4.0 Version 28 created 2000/06/27 18:05
Clearing TLBs Done
Power-On Reset
Executing Power On SelfTest
{0}@(#)POST, v4.1.1 06/30/2000 02:15 PM
                                  {1}
{0}* Test CPU present
               {1}@(#)POST, v4.1.1 06/30/2000 02:15 PM
               {1}* Test CPU present
{0}Soft POR to the whole system
               {1}Soft POR to the whole system
{0}* Configure I2C controller 0
{0}* Configure I2C controller 1
{0}* I2C Controller Loopback Test
{0}* Read JTag IDs of all ASICs
{0}     BBC     JTag ID: 1483203b
{0}     SCSI    JTag ID: 15060045
{0}     I chip  JTag ID: d1e203b
{0}     RIO     JTag ID: 3e5d03b
{0}     Schizo  JTag ID: 1024c06d
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}* Probing Seeprom on DIMMs and CPU modules
{0}WARNING: DIMM 0 missing
{0}WARNING: DIMM 2 missing
{0}WARNING: DIMM 4 missing
{0}WARNING: DIMM 6 missing
{0}CPU0 Sensor package temperature 32 oC
{0}CPU1 Sensor package temperature 29 oC
{0}WARNING: Temperature sensor on UPA0 missing
{0}WARNING: Temperature sensor on UPA1 missing
{0}Smart card reader present
{0}* Read parameters from seeproms
{0}             Size/bank(MB)           Number of banks
{0}DIMM 0:      0                               0
{0}DIMM 1:      64                              2
{0}DIMM 2:      0                               0
{0}DIMM 3:      64                              2
{0}DIMM 4:      0                               0
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(2 of 15)*

```
{0}DIMM 5:      64                                2
{0}DIMM 6:      0                                 0
{0}DIMM 7:      64                                2
{0}Bank 0 not present, size = 00000000.00000000
{0}Bank 1 is  present, size = 00000000.10000000
{0}Bank 2 not present, size = 00000000.00000000
{0}Bank 3 not present, size = 00000000.10000000
{0}* Setup CPUs and system frequency
{0}CPU 0 ratio: 5
{0}CPU 1 ratio: 4
{0}System frequency: 150 MHz
{0}* Load PLL and reset
              {1}
{0}
{0}PLL reset
              {1}PLL reset
{0}* Configure I2C controller 0
              {1}* SoftInt & Interrupt
{0}* Configure I2C controller 1
              {1}Test walking 1 through softint register
{0}* SoftInt & Interrupt
              {1}Test walking 0 through softint register
{0}Test walking 1 through softint register
              {1}Verify interrupt occurs for each level
{0}Test walking 0 through softint register
              {1}Verify interrupt occurs at the right PIL
{0}Verify interrupt occurs for each level
              {1}* Tick & Tick-Compare Reg
{0}Verify interrupt occurs at the right PIL
              {1}Walk 1/0 TICK Compare register
{0}* Tick & Tick-Compare Reg
              {1}Verify TICK register is counting
{0}Walk 1/0 TICK Compare register
              {1}Verify TICK register Overflow
{0}Verify TICK register is counting
              {1}Verify TICK Interrupt
{0}Verify TICK register Overflow
{0}Verify TICK Interrupt
              {1}* Stick & Stick-Compare Reg
              {1}Walk 1/0 STICK Compare register
{0}* Stick & Stick-Compare Reg
              {1}Verify STICK register is counting
{0}Walk 1/0 STICK Compare register
              {1}Verify STICK register Overflow
{0}Verify STICK register is counting
              {1}Verify STICK Interrupt
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(3 of 15)*

```
{0}Verify STICK register Overflow
{0}Verify STICK Interrupt
                {1}* Measure CPU Clock
{0}* Measure CPU Clock
{0}AFT pin is high
{0}Setup Memory Controller
{0}* IMMU Registers
                {1}* IMMU Registers
{0}Testing I-TSB
                {1}Testing I-TSB
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Test walking 0 through the register
                {1}Test walking 0 through the register
{0}Testing I-TLB Tag Access
                {1}Testing I-TLB Tag Access
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Test walking 0 through the register
                {1}Test walking 0 through the register
{0}* DMMU Registers
                {1}* DMMU Registers
{0}Testing Primary Context
                {1}Testing Primary Context
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Testing Secondary Context
                {1}Testing Secondary Context
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Testing D-TSB
                {1}Testing D-TSB
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Testing D-TLB Tag Access
                {1}Testing D-TLB Tag Access
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Testing Virtual Watchpoint
                {1}Testing Virtual Watchpoint
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Testing Physical Watchpoint
                {1}Testing Physical Watchpoint
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(4 of 15)*

```
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}* 4M DTLB RAM
                {1}* 4M DTLB RAM
{0}Test address up
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
{0}Test address line transitions
                {1}Test address line transitions
{0}* 8K DTLB RAM
                {1}* 8K DTLB RAM
{0}Test address up
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
{0}Test address line transitions
                {1}Test address line transitions
{0}* 4M DTLB TAG
{0}Test address up
{0}Test address down
                {1}* 4M DTLB TAG
{0}Test cell disturbance
                {1}Test address up
{0}Test data reliability
                {1}Test address down
{0}Test address line transitions
                {1}Test cell disturbance
{0}* 8K DTLB TAG
                {1}Test data reliability
{0}Test address up
                {1}Test address line transitions
                {1}* 8K DTLB TAG
                {1}Test address up
{0}Test address down
                {1}Test address down
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(5 of 15)*

```
{0}Test address line transitions
                {1}Test address line transitions
{0}* 4M ITLB RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
                {1}* 4M ITLB RAM
{0}Test data reliability
                {1}Test address up
                {1}Test address down
{0}Test address line transitions
                {1}Test cell disturbance
{0}* 8K ITLB RAM
                {1}Test data reliability
{0}Test address up
                {1}Test address line transitions
{0}Test address down
                {1}* 8K ITLB RAM
                {1}Test address up
{0}Test cell disturbance
                {1}Test address down
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
{0}Test address line transitions
{0}* 4M ITLB TAG
                {1}Test address line transitions
{0}Test address up
{0}Test address down
                {1}* 4M ITLB TAG
{0}Test cell disturbance
                {1}Test address up
{0}Test data reliability
                {1}Test address down
                {1}Test cell disturbance
{0}Test address line transitions
                {1}Test data reliability
{0}* 8K ITLB TAG
{0}Test address up
                {1}Test address line transitions
{0}Test address down
                {1}* 8K ITLB TAG
                {1}Test address up
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(6 of 15)*

```
{0}Test address line transitions
                {1}Test address down
{0}* IMMU Init
                {1}Test address line transitions
{0}* DMMU Init
                {1}* IMMU Init
{0}Mapping done. MMU enabled
                {1}* DMMU Init
{0}* Memory address selection Initial area
                {1}Mapping done. MMU enabled
                {1}* Memory address selection Initial area
{0}* Memory marching Initial area
                {1}* Memory marching Initial area
{0}* E-Cache Global Vars Init
{0}* E-Cache Quick Verification
                {1}* E-Cache Global Vars Init
                {1}* E-Cache Quick Verification
{0}* Ecache TAGS
{0}Test address up
                {1}* Ecache TAGS
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
{0}Test address line transitions
                {1}Test address line transitions
{0}* Ecache Address Line
                {1}* Ecache Address Line
{0}* Partial Ecache Init
                {1}* Partial Ecache Init
{0}* BBC E-Star Registers
{0}* I-Cache RAM
                {1}* I-Cache RAM
{0}Test address up
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(7 of 15)*

```
{0}Test address line transitions
                {1}Test address line transitions
{0}* I-Cache TAGS
{0}Testing I-Cache Tag
{0}Test address up
                {1}* I-Cache TAGS
                {1}Testing I-Cache Tag
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
{0}Test address line transitions
                {1}Test address line transitions
{0}Testing I-Cache Micro Tag
{0}Test address up
                {1}Testing I-Cache Micro Tag
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
{0}Test address line transitions
                {1}Test address line transitions
{0}* I-Cache Snoop Tags
{0}Test address up
                {1}* I-Cache Snoop Tags
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
{0}Test address line transitions
                {1}Test address line transitions
{0}* I-Cache Init
                {1}* I-Cache Init
{0}* D-Cache RAM
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(8 of 15)*

```
{0}Test address up
                {1}* D-Cache RAM
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
{0}Test address line transitions
                {1}Test address line transitions
{0}* D-Cache TAGS
{0}Test address up
                {1}* D-Cache TAGS
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
{0}Test address line transitions
                {1}Test address line transitions
{0}* D-Cache MicroTags
{0}Test address up
                {1}* D-Cache MicroTags
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
{0}Test address line transitions
                {1}Test address line transitions
{0}* D-Cache SnoopTags
{0}Test address up
                {1}* D-Cache SnoopTags
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(9 of 15)*

```
{0}Test address line transitions
                {1}Test address line transitions
{0}* D-Cache Init
                {1}* D-Cache Init
{0}* W-Cache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
                {1}* W-Cache RAM
                {1}Test address up
                {1}Test address down
                {1}Test cell disturbance
                {1}Test data reliability
{0}Test address line transitions
{0}* W-Cache TAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* W-Cache SnoopTAGS
{0}Test address up
                {1}Test address line transitions
{0}Test address down
{0}Test cell disturbance
                {1}* W-Cache TAGS
{0}Test data reliability
                {1}Test address up
                {1}Test address down
{0}Test address line transitions
                {1}Test cell disturbance
{0}* W-Cache Init
                {1}Test data reliability
{0}* P-Cache RAM
{0}Test address up
                {1}Test address line transitions
{0}Test address down
                {1}* W-Cache SnoopTAGS
                {1}Test address up
{0}Test cell disturbance
                {1}Test address down
                {1}Test cell disturbance
{0}Test data reliability
                {1}Test data reliability
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(10 of 15)*

```
                {1}Test address line transitions
                {1}* W-Cache Init
                {1}* P-Cache RAM
                {1}Test address up
                {1}Test address down
                {1}Test cell disturbance
{0}Test address line transitions
                {1}Test data reliability
{0}* P-Cache TAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* P-Cache SnoopTags
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
                {1}Test address line transitions
{0}Test address line transitions
                {1}* P-Cache TAGS
{0}* P-Cache Status Data
                {1}Test address up
{0}Test address up
                {1}Test address down
{0}Test address down
                {1}Test cell disturbance
{0}Test cell disturbance
                {1}Test data reliability
{0}Test data reliability
                {1}Test address line transitions
{0}Test address line transitions
                {1}* P-Cache SnoopTags
{0}* P-Cache Init
                {1}Test address up
{0}* FPU Registers
                {1}Test address down
{0}Test walking 1/0 FPU registers
                {1}Test cell disturbance
                {1}Test data reliability
                {1}Test address line transitions
                {1}* P-Cache Status Data
                {1}Test address up
                {1}Test address down
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(11 of 15)*

```
{1}Test cell disturbance
               {1}Test data reliability
               {1}Test address line transitions
               {1}* P-Cache Init
               {1}* FPU Registers
               {1}Test walking 1/0 FPU registers
{0}Test register addressing
{0}* FSR
{0}Test walking 1 FSR register
{0}* Ecache RAM
{0}Test address up
               {1}Test register addressing
               {1}* FSR
               {1}Test walking 1 FSR register
               {1}* Ecache RAM
               {1}Test address up
{0}Test address down
               {1}Test address down
{0}Test cell disturbance
               {1}Test cell disturbance
{0}Test data reliability
               {1}Test data reliability
{0}Test address line transitions
               {1}Test address line transitions
{0}* Ecache Init
               {1}* Ecache Init
{0}* Correctable Ecache ECC Test
               {1}* Correctable Ecache ECC Test
{0}* Uncorrectable Ecache ECC Test
               {1}* Uncorrectable Ecache ECC Test
{0}* Correctable SW Ecache ECC Test
               {1}* Correctable SW Ecache ECC Test
{0}* Uncorrectable SW Ecache ECC Test
               {1}* Uncorrectable SW Ecache ECC Test
{0}* Correctable System ECC Test
               {1}* Correctable System ECC Test
{0}* Uncorrectable System ECC Test
               {1}* Uncorrectable System ECC Test
{0}* Memory address selection All Banks
               {1}* Memory address selection All Banks
{0}* Memory marching All Banks
               {1}* Memory marching All Banks
{0}* Safari registers
{0}Safari ID reg fc000000.0011a953
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(12 of 15)*

```
{0}* Map PCI A space
                {1}* Map PCI B space
{0}* Schizo reg test
                {1}* Schizo reg test
{0}PBM A registers
                {1}PBM B registers
{0}Iommu A registers
                {1}Iommu B registers
{0}Streaming Cache A registers
                {1}Streaming Cache B registers
{0}Mondo Interrupt A registers
                {1}Mondo Interrupt B registers
{0}* Schizo pci A id test
{0}PCI A Vendor ID 108e
                {1}* Schizo pci B id test
{0}PCI A Device ID 8001
                {1}PCI B Vendor ID 108e
{0}* Schizo mem test
                {1}PCI B Device ID 8001
{0}memtst ram data port A
                {1}* Schizo mem test
                {1}memtst ram data port B
{0}memtst cam data port A
                {1}memtst cam data port B
{0}memtst ram addr port A
{0}memtst cam addr port A
                {1}memtst ram addr port B
{0}memtst pnta     port A
                {1}memtst cam addr port B
                {1}memtst pnta     port B
{0}memtst lnta     port A
                {1}memtst lnta     port B
{0}memtst rnta     port A
                {1}memtst rnta     port B
{0}memtst enta     port A
{0}memtst ln addr  port A
                {1}memtst enta     port B
{0}memtst pg addr  port A
                {1}memtst ln addr  port B
{0}memtst sbuf addr port A
                {1}memtst pg addr  port B
                {1}memtst sbuf addr port B
{0}* Schizo merg test
{0}merg_wr 8 byte port A
{0}merg_wr 4 byte port A
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(13 of 15)*

```
{0}merg_wr 2 byte port A
               {1}* Schizo merg test
{0}merg_wr 1 byte port A
               {1}merg_wr 8 byte port B
{0}merg_blkwr block  port A
               {1}merg_wr 4 byte port B
               {1}merg_wr 2 byte port B
               {1}merg_wr 1 byte port B
               {1}merg_blkwr block  port B
{0}* Map PCI B space for RIO
{0}* RIO Config
{0}* RIO EBus access
               {1}* Icache Functional
               {1}Verify cacheline fill on read miss
               {1}* Dcache Functional
               {1}Verify no allocate on write miss
               {1}Verify fetch from memory on read miss
               {1}Verify write-through on write hit
               {1}Verify write-through/fetch on read miss
               {1}Verify set-associativity
               {1}* Wcache Functional
               {1}Verify cacheline fill on write miss
               {1}Verify buffering
               {1}Verify coalescing
               {1}* Pcache Functional
               {1}* FPU Functional
               {1}Test single and double-precision addition
               {1}Test single and double-precision subtraction
               {1}Test single and double-precision multiplication
               {1}Test single and double-precision division
               {1}Test single and double-precision sqrt
               {1}Test single and double-precision abs
               {1}Test single and double-precision conversion
               {1}* FPU Move To Registers
               {1}Moving SP fp value through all fp registers
               {1}Moving DP fp value through all fp registers
               {1}* FPU Branch
               {1}Testing Branching on fcc0
               {1}Verify branching
               {1}Verify no branching
               {1}Testing Branching on fcc1
               {1}Verify branching
               {1}Verify no branching
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(14 of 15)*

```
{1}Testing Branching on fcc2
                {1}Verify branching
                {1}Verify no branching
                {1}Testing Branching on fcc3
                {1}Verify branching
                {1}Verify no branching
                {1}* Ecache Functional
                {1}Verify cacheline fill on read miss
                {1}Verify write allocate on write miss
                {1}Verify cacheline update on write hit
                {1}Verify write back
{0}* Icache Functional
{0}Verify cacheline fill on read miss
{0}* Dcache Functional
{0}Verify no allocate on write miss
{0}Verify fetch from memory on read miss
{0}Verify write-through on write hit
{0}Verify write-through/fetch on read miss
{0}Verify set-associativity
{0}* Wcache Functional
{0}Verify cacheline fill on write miss
{0}Verify buffering
{0}Verify coalescing
{0}* Pcache Functional
{0}* FPU Functional
{0}Test single and double-precision addition
{0}Test single and double-precision subtraction
{0}Test single and double-precision multiplication
{0}Test single and double-precision division
{0}Test single and double-precision sqrt
{0}Test single and double-precision abs
{0}Test single and double-precision conversion
{0}* FPU Move To Registers
{0}Moving SP fp value through all fp registers
{0}Moving DP fp value through all fp registers
{0}* FPU Branch
{0}Testing Branching on fcc0
{0}Verify branching
{0}Verify no branching
{0}Testing Branching on fcc1
{0}Verify branching
{0}Verify no branching
{0}Testing brancing on fcc2
{0}Verify branching
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` (2-Way CPU) *(15 of 15)*

```
{0}Verify no branching
{0}Testing Branching on fcc3
{0}Verify branching
{0}Verify no branching
{0}* Ecache Functional
{0}Verify cacheline fill on read miss
{0}Verify write allocate on write miss
{0}Verify cacheline update on write hit
{0}Verify write back
{0}* Xcall Test
{0}Sending Cross Calls to CPU AID 1
              {1}POST_END
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `max` (single CPU) *(1 of 9)*

```
@(#)  4.0 Version 28 created 2000/06/27 18:05
Clearing TLBs Done
Power-On Reset
Executing Power On SelfTest
{0}
{0}@(#)POST, v4.1.1 06/30/2000 02:15 PM
{0}* Test CPU present
{0}     Device Present register (BBC) showed that
{0}     CPU1 not present or dead
{0}Soft POR to the whole system
{0}* Configure I2C controller 0
{0}* Configure I2C controller 1
{0}* I2C Controller Loopback Test
{0}* Read JTag IDs of all ASICs
{0}     BBC     JTag ID: 1483203b
{0}     SCSI    JTag ID: 15060045
{0}     I chip  JTag ID: d1e203b
{0}     RIO     JTag ID: 3e5d03b
{0}     Schizo  JTag ID: 1024c06d
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}* Probing Seeprom on DIMMs and CPU modules
{0}WARNING: DIMM 0 missing
{0}WARNING: DIMM 2 missing
{0}WARNING: DIMM 4 missing
{0}WARNING: DIMM 6 missing
{0}CPU0 Sensor package temperature 31 oC
{0}WARNING: Temperature sensor on UPA0 missing
{0}WARNING: Temperature sensor on UPA1 missing
{0}Smart card reader present
{0}* Read parameters from seeproms
{0}             Size/bank(MB)           Number of banks
{0}DIMM 0:      0                               0
{0}DIMM 1:      64                              2
{0}DIMM 2:      0                               0
{0}DIMM 3:      64                              2
{0}DIMM 4:      0                               0
{0}DIMM 5:      64                              2
{0}DIMM 6:      0                               0
{0}DIMM 7:      64                              2
{0}Bank 0 not present, size = 00000000.00000000
{0}Bank 1 is  present, size = 00000000.10000000
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `max` (single CPU) *(2 of 9)*

```
{0}Bank 2 not present, size = 00000000.00000000
{0}Bank 3 not present, size = 00000000.10000000
{0}* Setup CPUs and system frequency
{0}CPU 0 ratio: 4
{0}CPU 1 ratio: 0
{0}System frequency: 150 MHz
{0}* Load PLL and reset
{0}
{0}PLL reset
{0}* Configure I2C controller 0
{0}* Configure I2C controller 1
{0}* SoftInt & Interrupt
{0}Test walking 1 through softint register
{0}Test walking 0 through softint register
{0}Verify interrupt occurs for each level
{0}Verify interrupt occurs at the right PIL
{0}* Tick & Tick-Compare Reg
{0}Walk 1/0 TICK Compare register
{0}Verify TICK register is counting
{0}Verify TICK register Overflow
{0}Verify TICK Interrupt
{0}* Stick & Stick-Compare Reg
{0}Walk 1/0 STICK Compare register
{0}Verify STICK register is counting
{0}Verify STICK register Overflow
{0}Verify STICK Interrupt
{0}* Measure CPU Clock
{0}AFT pin is high
{0}Setup Memory Controller
{0}* IMMU Registers
{0}Testing I-TSB
{0}Test walking 1 through the register
{0}Test walking 0 through the register
{0}Testing I-TLB Tag Access
{0}Test walking 1 through the register
{0}Test walking 0 through the register
{0}* DMMU Registers
{0}Testing Primary Context
{0}Test walking 1 through the register
{0}Testing Secondary Context
{0}Test walking 1 through the register
{0}Testing D-TSB
{0}Test walking 1 through the register
{0}Testing D-TLB Tag Access
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `max` (single CPU) *(3 of 9)*

```
{0}Test walking 1 through the register
{0}Testing Virtual Watchpoint
{0}Test walking 1 through the register
{0}Testing Physical Watchpoint
{0}Test walking 1 through the register
{0}* 4M DTLB RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* 8K DTLB RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* 4M DTLB TAG
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* 8K DTLB TAG
{0}Test address up
{0}Test address down
{0}Test address line transitions
{0}* 4M ITLB RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* 8K ITLB RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* 4M ITLB TAG
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* 8K ITLB TAG
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `max` (single CPU) *(4 of 9)*

```
{0}Test address up
{0}Test address down
{0}Test address line transitions
{0}* IMMU Init
{0}* DMMU Init
{0}Mapping done. MMU enabled
{0}* Memory address selection Initial area
{0}* Memory marching Initial area
{0}* E-Cache Global Vars Init
{0}* E-Cache Quick Verification
{0}* Ecache TAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* Ecache Address Line
{0}* Partial Ecache Init
{0}* BBC E-Star Registers
{0}* I-Cache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* I-Cache TAGS
{0}Testing I-Cache Tag
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}Testing I-Cache Micro Tag
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* I-Cache Snoop Tags
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* I-Cache Init
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `max` (single CPU) *(5 of 9)*

```
{0}* D-Cache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* D-Cache TAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* D-Cache MicroTags
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* D-Cache SnoopTags
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* D-Cache Init
{0}* W-Cache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* W-Cache TAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* W-Cache SnoopTAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* W-Cache Init
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `max` (single CPU) *(6 of 9)*

```
{0}* P-Cache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* P-Cache TAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* P-Cache SnoopTags
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* P-Cache Status Data
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* P-Cache Init
{0}* FPU Registers
{0}Test walking 1/0 FPU registers
{0}Test register addressing
{0}* FSR
{0}Test walking 1 FSR register
{0}* Ecache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Test data reliability
{0}Test address line transitions
{0}* Ecache Init
{0}* Correctable Ecache ECC Test
{0}* Uncorrectable Ecache ECC Test
{0}* Correctable SW Ecache ECC Test
{0}* Uncorrectable SW Ecache ECC Test
{0}* Correctable System ECC Test
{0}* Uncorrectable System ECC Test
{0}* Memory address selection All Banks
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `max` (single CPU) *(7 of 9)*

```
{0}* Memory marching All Banks
{0}* Safari registers
{0}Safari ID reg fc000000.0011a953
{0}* Map PCI A space
{0}* Schizo reg test
{0}PBM A registers
{0}Iommu A registers
{0}Streaming Cache A registers
{0}Mondo Interrupt A registers
{0}* Schizo pci A id test
{0}PCI A Vendor ID 108e
{0}PCI A Device ID 8001
{0}* Schizo mem test
{0}memtst ram data port A
{0}memtst cam data port A
{0}memtst ram addr port A
{0}memtst cam addr port A
{0}memtst pnta     port A
{0}memtst lnta     port A
{0}memtst rnta     port A
{0}memtst enta     port A
{0}memtst ln addr  port A
{0}memtst pg addr  port A
{0}memtst sbuf addr port A
{0}* Schizo merg test
{0}merg_wr 8 byte port A
{0}merg_wr 4 byte port A
{0}merg_wr 2 byte port A
{0}merg_wr 1 byte port A
{0}merg_blkwr block  port A
{0}* Map PCI B space
{0}* Schizo reg test
{0}PBM B registers
{0}Iommu B registers
{0}Streaming Cache B registers
{0}Mondo Interrupt B registers
{0}* Schizo pci B id test
{0}PCI B Vendor ID 108e
{0}PCI B Device ID 8001
{0}* Schizo mem test
{0}memtst ram data port B
{0}memtst cam data port B
{0}memtst ram addr port B
{0}memtst cam addr port B
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `max` (single CPU) *(8 of 9)*

```
{0}memtst pnta     port B
{0}memtst lnta     port B
{0}memtst rnta     port B
{0}memtst enta     port B
{0}memtst ln addr  port B
{0}memtst pg addr  port B
{0}memtst sbuf addr port B
{0}* Schizo merg test
{0}merg_wr 8 byte port B
{0}merg_wr 4 byte port B
{0}merg_wr 2 byte port B
{0}merg_wr 1 byte port B
{0}merg_blkwr block  port B
{0}* Map PCI B space for RIO
{0}* RIO Config
{0}* RIO EBus access
{0}* Icache Functional
{0}Verify cacheline fill on read miss
{0}* Dcache Functional
{0}Verify no allocate on write miss
{0}Verify fetch from memory on read miss
{0}Verify write-through on write hit
{0}Verify write-through/fetch on read miss
{0}Verify set-associativity
{0}* Wcache Functional
{0}Verify cacheline fill on write miss
{0}Verify buffering
{0}Verify coalescing
{0}* Pcache Functional
{0}* FPU Functional
{0}Test single and double-precision addition
{0}Test single and double-precision subtraction
{0}Test single and double-precision multiplication
{0}Test single and double-precision division
{0}Test single and double-precision sqrt
{0}Test single and double-precision abs
{0}Test single and double-precision conversion
{0}* FPU Move To Registers
{0}Moving SP fp value through all fp registers
{0}Moving DP fp value through all fp registers
{0}* FPU Branch
{0}Testing Branching on fcc0
{0}Verify branching
{0}Verify no branching
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `max` (single CPU) *(9 of 9)*

```
{0}Testing Branching on fcc1
{0}Verify branching
{0}Verify no branching
{0}Testing Branching on fcc2
{0}Verify branching
{0}Verify no branching
{0}Testing Branching on fcc3
{0}Verify branching
{0}Verify no branching
{0}* Ecache Functional
{0}Verify cacheline fill on read miss
{0}Verify write allocate on write miss
{0}Verify cacheline update on write hit
{0}Verify write back
{0}POST_END
```

3.4.2 `diag-level` Variable Set to `min`

When the `diag-level` variable is set to `min`, POST enables an abbreviated set of diagnostic-level tests. See TABLE 3-1 on page 3-5 for approximate completion times. The following code example identifies serial port A POST output with the `diag-level` NVRAM variable set to `min` for 2-way, and single CPU configurations.

- `diag-level` Variable Set to `min` (2-Way CPU) CODE EXAMPLE 3-3 on page 3-32
- `diag-level` Variable Set to `min` (single CPU) CODE EXAMPLE 3-4 on page 3-45

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(1 of 12)*

```
@(#)  4.0 Version 28 created 2000/06/27 18:05
Clearing TLBs Done
Power-On Reset
Executing Power On SelfTest
{0}@(#)POST, v4.1.1 06/30/2000 02:15 PM
               {1}
{0}* Test CPU present
               {1}@(#)POST, v4.1.1 06/30/2000 02:15 PM
               {1}* Test CPU present
{0}Soft POR to the whole system
               {1}Soft POR to the whole system
{0}* Configure I2C controller 0
{0}* Configure I2C controller 1
{0}* I2C Controller Loopback Test
{0}* Read JTag IDs of all ASICs
{0}     BBC     JTag ID: 1483203b
{0}     SCSI    JTag ID: 15060045
{0}     I chip  JTag ID: d1e203b
{0}     RIO     JTag ID: 3e5d03b
{0}     Schizo  JTag ID: 1024c06d
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}* Probing Seeprom on DIMMs and CPU modules
{0}WARNING: DIMM 0 missing
{0}WARNING: DIMM 2 missing
{0}WARNING: DIMM 4 missing
{0}WARNING: DIMM 6 missing
{0}CPU0 Sensor package temperature 32 oC
{0}CPU1 Sensor package temperature 24 oC
{0}WARNING: Temperature sensor on UPA0 missing
{0}WARNING: Temperature sensor on UPA1 missing
{0}Smart card reader present
{0}* Read parameters from seeproms
{0}             Size/bank(MB)           Number of banks
{0}DIMM 0:      0                               0
{0}DIMM 1:      64                              2
{0}DIMM 2:      0                               0
{0}DIMM 3:      64                              2
{0}DIMM 4:      0                               0
{0}DIMM 5:      64                              2
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(2 of 12)*

```
{0}DIMM 6:      0                                   0
{0}DIMM 7:      64                                  2
{0}Bank 0 not present, size = 00000000.00000000
{0}Bank 1 is  present, size = 00000000.10000000
{0}Bank 2 not present, size = 00000000.00000000
{0}Bank 3 not present, size = 00000000.10000000
{0}* Setup CPUs and system frequency
{0}CPU 0 ratio: 5
{0}CPU 1 ratio: 4
{0}System frequency: 150 MHz
{0}* Load PLL and reset
               {1}
{0}
{0}PLL reset
               {1}PLL reset
{0}* Configure I2C controller 0
               {1}* SoftInt & Interrupt
{0}* Configure I2C controller 1
               {1}Test walking 1 through softint register
{0}* SoftInt & Interrupt
               {1}Test walking 0 through softint register
{0}Test walking 1 through softint register
               {1}Verify interrupt occurs for each level
{0}Test walking 0 through softint register
               {1}Verify interrupt occurs at the right PIL
{0}Verify interrupt occurs for each level
               {1}* Tick & Tick-Compare Reg
{0}Verify interrupt occurs at the right PIL
               {1}Walk 1/0 TICK Compare register
{0}* Tick & Tick-Compare Reg
               {1}Verify TICK register is counting
{0}Walk 1/0 TICK Compare register
               {1}Verify TICK register Overflow
{0}Verify TICK register is counting
               {1}Verify TICK Interrupt
{0}Verify TICK register Overflow
{0}Verify TICK Interrupt
               {1}* Stick & Stick-Compare Reg
               {1}Walk 1/0 STICK Compare register
{0}* Stick & Stick-Compare Reg
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(3 of 12)*

```
{0}Walk 1/0 STICK Compare register
                {1}Verify STICK register Overflow
{0}Verify STICK register is counting
                {1}Verify STICK Interrupt
{0}Verify STICK register Overflow
{0}Verify STICK Interrupt
                {1}* Measure CPU Clock
{0}* Measure CPU Clock
{0}AFT pin is high
{0}Setup Memory Controller
{0}* IMMU Registers
                {1}* IMMU Registers
{0}Testing I-TSB
                {1}Testing I-TSB
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Test walking 0 through the register
                {1}Test walking 0 through the register
{0}Testing I-TLB Tag Access
                {1}Testing I-TLB Tag Access
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Test walking 0 through the register
                {1}Test walking 0 through the register
{0}* DMMU Registers
                {1}* DMMU Registers
{0}Testing Primary Context
                {1}Testing Primary Context
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Testing Secondary Context
                {1}Testing Secondary Context
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Testing D-TSB
                {1}Testing D-TSB
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Testing D-TLB Tag Access
                {1}Testing D-TLB Tag Access
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Testing Virtual Watchpoint
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(4 of 12)*

```
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}Testing Physical Watchpoint
                {1}Testing Physical Watchpoint
{0}Test walking 1 through the register
                {1}Test walking 1 through the register
{0}* 4M DTLB RAM
                {1}* 4M DTLB RAM
{0}Test address up
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* 8K DTLB RAM
                {1}* 8K DTLB RAM
{0}Test address up
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* 4M DTLB TAG
{0}Test address up
                {1}* 4M DTLB TAG
{0}Test address down
                {1}Test address up
{0}Test cell disturbance
{0}* 8K DTLB TAG
                {1}Test cell disturbance
{0}Test address up
                {1}* 8K DTLB TAG
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test address line transitions
                {1}Test address line transitions
{0}* 4M ITLB RAM
{0}Test address up
{0}Test address down
                {1}* 4M ITLB RAM
{0}Test cell disturbance
{0}* 8K ITLB RAM
                {1}Test address down
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(5 of 12)*

```
{0}Test address up
                {1}Test cell disturbance
{0}Test address down
                {1}* 8K ITLB RAM
                {1}Test address up
{0}Test cell disturbance
                {1}Test address down
                {1}Test cell disturbance
{0}* 4M ITLB TAG
{0}Test address up
{0}Test address down
{0}Test cell disturbance
                {1}* 4M ITLB TAG
{0}* 8K ITLB TAG
                {1}Test address up
{0}Test address up
                {1}Test address down
{0}Test address down
                {1}Test cell disturbance
{0}Test address line transitions
                {1}* 8K ITLB TAG
                {1}Test address up
{0}* IMMU Init
                {1}Test address down
{0}* DMMU Init
                {1}Test address line transitions
{0}Mapping done. MMU enabled
                {1}* IMMU Init
{0}* Memory address selection Initial area
                {1}* DMMU Init
                {1}Mapping done. MMU enabled
                {1}* Memory address selection Initial area
{0}* E-Cache Global Vars Init
{0}* E-Cache Quick Verification
                {1}* E-Cache Global Vars Init
                {1}* E-Cache Quick Verification
{0}* Ecache TAGS
{0}Test address up
                {1}* Ecache TAGS
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbancen
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(6 of 12)*

```
{0}* Ecache Address Line
                {1}* Ecache Address Line
{0}* Partial Ecache Init
                {1}* Partial Ecache Init
{0}* BBC E-Star Registers
{0}* I-Cache RAM
                {1}* I-Cache RAM
{0}Test address up
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* I-Cache TAGS
{0}Testing I-Cache Tag
                {1}* I-Cache TAGS
{0}Test address up
                {1}Testing I-Cache Tag
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}Testing I-Cache Micro Tag
{0}Test address up
                {1}Testing I-Cache Micro Tag
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* I-Cache Snoop Tags
{0}Test address up
                {1}* I-Cache Snoop Tags
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* I-Cache Init
                {1}* I-Cache Init
{0}* D-Cache RAM
{0}Test address up
                {1}* D-Cache RAM
                {1}Test address up
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(7 of 12)*

```
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* D-Cache TAGS
{0}Test address up
                {1}* D-Cache TAGS
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* D-Cache MicroTags
{0}Test address up
                {1}* D-Cache MicroTags
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* D-Cache SnoopTags
{0}Test address up
                {1}* D-Cache SnoopTags
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* D-Cache Init
                {1}* D-Cache Init
{0}* W-Cache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
                {1}* W-Cache RAM
                {1}Test address up
{0}* W-Cache TAGS
{0}Test address up
                {1}Test address down
{0}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* W-Cache SnoopTAGS
{0}Test address up
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(8 of 12)*

```
{0}Test address down
                {1}* W-Cache TAGS
{0}Test cell disturbance
                {1}Test address up
{0}* W-Cache Init
                {1}Test address down
{0}* P-Cache RAM
                {1}Test cell disturbance
{0}Test address up
                {1}* W-Cache SnoopTAGS
                {1}Test address up
{0}Test address down
                {1}Test address down
                {1}Test cell disturbance
{0}Test cell disturbance
                {1}* W-Cache Init
                {1}* P-Cache RAM
                {1}Test address up
{0}* P-Cache TAGS
{0}Test address up
                {1}Test address down
{0}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* P-Cache SnoopTags
{0}Test address up
{0}Test address down
                {1}* P-Cache TAGS
{0}Test cell disturbance
                {1}Test address up
{0}* P-Cache Status Data
                {1}Test address down
{0}Test address up
                {1}Test cell disturbance
{0}Test address down
                {1}* P-Cache SnoopTags
{0}Test cell disturbance
                {1}Test address up
{0}* P-Cache Init
                {1}Test address down
{0}* FPU Registers
                {1}Test cell disturbance
{0}Test walking 1/0 FPU registers
                {1}* P-Cache Status Data
                {1}Test address up
                {1}Test address down
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(9 of 12)*

```
                {1}Test cell disturbance
                {1}* P-Cache Init
                {1}* FPU Registers
                {1}Test walking 1/0 FPU registers
{0}Test register addressing
{0}* FSR
{0}Test walking 1 FSR register
{0}* Ecache RAM
                {1}Test register addressing
{0}Test address up
                {1}* FSR
                {1}Test walking 1 FSR register
                {1}* Ecache RAM
                {1}Test address up
{0}Test address down
                {1}Test address down
{0}Test cell disturbance
                {1}Test cell disturbance
{0}* Ecache Init
                {1}* Ecache Init
{0}* Correctable Ecache ECC Test
                {1}* Correctable Ecache ECC Test
{0}* Uncorrectable Ecache ECC Test
                {1}* Uncorrectable Ecache ECC Test
{0}* Correctable SW Ecache ECC Test
                {1}* Correctable SW Ecache ECC Test
{0}* Uncorrectable SW Ecache ECC Test
                {1}* Uncorrectable SW Ecache ECC Test
{0}* Correctable System ECC Test
                {1}* Correctable System ECC Test
{0}* Uncorrectable System ECC Test
                {1}* Uncorrectable System ECC Test
{0}* Memory address selection All Banks
                {1}* Memory address selection All Banks
{0}* Safari registers
{0}Safari ID reg fc000000.0011a953
{0}* Map PCI A space
                {1}* Map PCI B space
{0}* Schizo reg test
                {1}* Schizo reg test
{0}PBM A registers
                {1}PBM B registers
{0}Iommu A registers
                {1}Iommu B registers
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(10 of 12)*

```
{0}Streaming Cache A registers
                                    {1}Streaming Cache B registers
{0}Mondo Interrupt A registers
               {1}Mondo Interrupt B registers
{0}* Schizo pci A id test
{0}PCI A Vendor ID 108e
               {1}* Schizo pci B id test
{0}PCI A Device ID 8001
               {1}PCI B Vendor ID 108e
{0}* Schizo mem test
               {1}PCI B Device ID 8001
{0}memtst ram data port A
               {1}* Schizo mem test
               {1}memtst ram data port B
{0}memtst cam data port A
               {1}memtst cam data port B
{0}memtst ram addr port A
{0}memtst cam addr port A
               {1}memtst ram addr port B
{0}memtst pnta     port A
               {1}memtst cam addr port B
               {1}memtst pnta     port B
{0}memtst lnta     port A
               {1}memtst lnta     port B
{0}memtst rnta     port A
               {1}memtst rnta     port B
{0}memtst enta     port A
{0}memtst ln addr  port A
               {1}memtst enta     port B
{0}memtst pg addr  port A
               {1}memtst ln addr  port B
{0}memtst sbuf addr port A
               {1}memtst pg addr  port B
               {1}memtst sbuf addr port B
{0}* Schizo merg test
{0}merg_wr 8 byte port A
{0}merg_wr 4 byte port A
               {1}* Schizo merg test
               {1}merg_wr 8 byte port B
               {1}merg_wr 4 byte port B
{0}* Map PCI B space for RIO
{0}* RIO Config
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(11 of 12)*

```
{0}* RIO EBus access
                {1}* Icache Functional
                {1}Verify cacheline fill on read miss
                {1}* Dcache Functional
                {1}Verify no allocate on write miss
                {1}Verify fetch from memory on read miss
                {1}Verify write-through on write hit
                {1}Verify write-through/fetch on read miss
                {1}Verify set-associativity
                {1}* Wcache Functional
                {1}Verify cacheline fill on write miss
                {1}Verify buffering
                {1}Verify coalescing
                {1}* Pcache Functional
                {1}* FPU Functional
                {1}Test single and double-precision addition
                {1}Test single and double-precision subtraction
                {1}Test single and double-precision multiplication
                {1}Test single and double-precision division
                {1}Test single and double-precision sqrt
                {1}Test single and double-precision abs
                {1}Test single and double-precision conversion
                {1}* FPU Move To Registers
                {1}Moving SP fp value through all fp registers
                {1}Moving DP fp value through all fp registers
                {1}* FPU Branch
                {1}Testing Branching on fcc0
                {1}Verify branching
                {1}Verify no branching
                {1}Testing Branching on fcc1
                {1}Verify branching
                {1}Verify no branching
                {1}Testing Branching on fcc2
                {1}Verify branching
                {1}Verify no branching
                {1}Testing Branching on fcc3
                {1}Verify branching
                {1}Verify no branching
                {1}* Ecache Functional
                {1}Verify cacheline fill on read miss
                {1}Verify write allocate on write miss
                {1}Verify cacheline update on write hit
                {1}Verify write back
{0}* Icache Functional
{0}Verify cacheline fill on read miss
{0}* Dcache Functional
```

CODE EXAMPLE 3-3 `diag-level` Variable Set to `min` (2-Way CPU) *(12 of 12)*

```
{0}Verify no allocate on write miss
{0}Verify fetch from memory on read miss
{0}Verify write-through on write hit
{0}Verify write-through/fetch on read miss
{0}Verify set-associativity
{0}* Wcache Functional
{0}Verify cacheline fill on write miss
{0}Verify buffering
{0}Verify coalescing
{0}* Pcache Functional
{0}* FPU Functional
{0}Test single and double-precision addition
{0}Test single and double-precision subtraction
{0}Test single and double-precision multiplication
{0}Test single and double-precision division
{0}Test single and double-precision sqrt
{0}Test single and double-precision abs
{0}Test single and double-precision conversion
{0}* FPU Move To Registers
{0}Moving SP fp value through all fp registers
{0}Moving DP fp value through all fp registers
{0}* FPU Branch
{0}Testing Branching on fcc0
{0}Verify branching
{0}Verify no branching
{0}Testing Branching on fcc1
{0}Verify branching
{0}Verify no branching
{0}Testing Branching on fcc2
{0}Verify branching
{0}Verify no branching
{0}Testing Branching on fcc3
{0}Verify branching
{0}Verify no branching
{0}* Ecache Functional
{0}Verify cacheline fill on read miss
{0}Verify write allocate on write miss
{0}Verify cacheline update on write hit
{0}Verify write back
{0}* Xcall Test
{0}Sending Cross Calls to CPU AID 1
              {1}POST_END
```

Note – The following POST examples are executed with 750-MHz CPUs and 512-MB of memory.

CODE EXAMPLE 3-4 `diag-level` Variable Set to `min` (Single CPU) *(1 of 8)*

```
@(#)  4.0 Version 35 created 2000/01/21 17:29
Clearing TLBs Done
Executing Power On SelfTest
{0}

@(#)  4.0 Version 28 created 2000/06/27 18:05
Clearing TLBs Done
Power-On Reset
Executing Power On SelfTest
{0}
{0}@(#)POST, v4.1.1 06/30/2000 02:15 PM
{0}* Test CPU present
{0}     Device Present register (BBC) showed that
{0}     CPU1 not present or dead
{0}Soft POR to the whole system
{0}* Configure I2C controller 0
{0}* Configure I2C controller 1
{0}* I2C Controller Loopback Test
{0}* Read JTag IDs of all ASICs
{0}     BBC     JTag ID: 1483203b
{0}     SCSI    JTag ID: 15060045
{0}     I chip  JTag ID: d1e203b
{0}     RIO     JTag ID: 3e5d03b
{0}     Schizo  JTag ID: 1024c06d
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}     CPMS    JTag ID: 1142903b
{0}* Probing Seeprom on DIMMs and CPU modules
{0}WARNING: DIMM 0 missing
{0}WARNING: DIMM 2 missing
{0}WARNING: DIMM 4 missing
{0}WARNING: DIMM 6 missing
{0}CPU0 Sensor package temperature 34 oC
{0}WARNING: Temperature sensor on UPA0 missing
{0}WARNING: Temperature sensor on UPA1 missing
{0}Smart card reader present
{0}* Read parameters from seeproms
{0}             Size/bank(MB)           Number of banks
{0}DIMM 0:      0                        0
{0}DIMM 1:      64                       2
{0}DIMM 2:      0                        0
{0}DIMM 3:      64                       2
```

CODE EXAMPLE 3-4 `diag-level` Variable Set to `min` (Single CPU) *(Continued) (2 of 8)*

```
{0}DIMM 4:      0                                   0
{0}DIMM 5:      64                                  2
{0}DIMM 6:      0                                   0
{0}DIMM 7:      64                                  2
{0}Bank 0 not present, size = 00000000.00000000
{0}Bank 1 is  present, size = 00000000.10000000
{0}Bank 2 not present, size = 00000000.00000000
{0}Bank 3 not present, size = 00000000.10000000
{0}* Setup CPUs and system frequency
{0}CPU 0 ratio: 4
{0}CPU 1 ratio: 0
{0}System frequency: 150 MHz
{0}* Load PLL and reset
{0}
{0}PLL reset
{0}* Configure I2C controller 0
{0}* Configure I2C controller 1
{0}* SoftInt & Interrupt
{0}Test walking 1 through softint register
{0}Test walking 0 through softint register
{0}Verify interrupt occurs for each level
{0}Verify interrupt occurs at the right PIL
{0}* Tick & Tick-Compare Reg
{0}Walk 1/0 TICK Compare register
{0}Verify TICK register is counting
{0}Verify TICK register Overflow
{0}Verify TICK Interrupt
{0}* Stick & Stick-Compare Reg
{0}Walk 1/0 STICK Compare register
{0}Verify STICK register is counting
{0}Verify STICK register Overflow
{0}Verify STICK Interrupt
{0}* Measure CPU Clock
{0}AFT pin is high
{0}Setup Memory Controller
{0}* IMMU Registers
{0}Testing I-TSB
{0}Test walking 1 through the register
{0}Test walking 0 through the register
{0}Testing I-TLB Tag Access
{0}Test walking 1 through the register
{0}Test walking 0 through the register
{0}* DMMU Registers
{0}Testing Primary Context
{0}Test walking 1 through the register
{0}Testing Secondary Context
```

CODE EXAMPLE 3-4 `diag-level` Variable Set to `min` (Single CPU) *(Continued) (3 of 8)*

```
{0}Test walking 1 through the register
{0}Testing D-TSB
{0}Test walking 1 through the register
{0}Testing D-TLB Tag Access
{0}Test walking 1 through the register
{0}Testing Virtual Watchpoint
{0}Test walking 1 through the register
{0}Testing Physical Watchpoint
{0}Test walking 1 through the register
{0}* 4M DTLB RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* 8K DTLB RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* 4M DTLB TAG
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* 8K DTLB TAG
{0}Test address up
{0}Test address down
{0}Test address line transitions
{0}* 4M ITLB RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* 8K ITLB RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* 4M ITLB TAG
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* 8K ITLB TAG
{0}Test address up
{0}Test address down
{0}Test address line transitions
{0}* IMMU Init
{0}* DMMU Init
{0}Mapping done. MMU enabled
{0}* Memory address selection Initial area
{0}* E-Cache Global Vars Init
```

CODE EXAMPLE 3-4 `diag-level` Variable Set to `min` (Single CPU) *(Continued) (4 of 8)*

```
{0}* E-Cache Quick Verification
{0}* Ecache TAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* Ecache Address Line
{0}* Partial Ecache Init
{0}* BBC E-Star Registers
{0}* I-Cache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* I-Cache TAGS
{0}Testing I-Cache Tag
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}Testing I-Cache Micro Tag
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* I-Cache Snoop Tags
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* I-Cache Init
{0}* D-Cache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* D-Cache TAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* D-Cache MicroTags
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* D-Cache SnoopTags
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* D-Cache Init
{0}* W-Cache RAM
```

CODE EXAMPLE 3-4 `diag-level` Variable Set to `min` (Single CPU) *(Continued) (5 of 8)*

```
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* W-Cache TAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* W-Cache SnoopTAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* W-Cache Init
{0}* P-Cache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* P-Cache TAGS
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* P-Cache SnoopTags
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* P-Cache Status Data
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* P-Cache Init
{0}* FPU Registers
{0}Test walking 1/0 FPU registers
{0}Test register addressing
{0}* FSR
{0}Test walking 1 FSR register
{0}* Ecache RAM
{0}Test address up
{0}Test address down
{0}Test cell disturbance
{0}* Ecache Init
{0}* Correctable Ecache ECC Test
{0}* Uncorrectable Ecache ECC Test
{0}* Correctable SW Ecache ECC Test
{0}* Uncorrectable SW Ecache ECC Test
{0}* Correctable System ECC Test
```

CODE EXAMPLE 3-4 `diag-level` Variable Set to `min` (Single CPU) *(Continued) (6 of 8)*

```
{0}* Uncorrectable System ECC Test
{0}* Memory address selection All Banks
{0}* Safari registers
{0}Safari ID reg fc000000.0011a953
{0}* Map PCI A space
{0}* Schizo reg test
{0}PBM A registers
{0}Iommu A registers
{0}Streaming Cache A registers
{0}Mondo Interrupt A registers
{0}* Schizo pci A id test
{0}PCI A Vendor ID 108e
{0}PCI A Device ID 8001
{0}* Schizo mem test
{0}memtst ram data port A
{0}memtst cam data port A
{0}memtst ram addr port A
{0}memtst cam addr port A
{0}memtst pnta     port A
{0}memtst lnta     port A
{0}memtst rnta     port A
{0}memtst enta     port A
{0}memtst ln addr  port A
{0}memtst pg addr  port A
{0}memtst sbuf addr port A
{0}* Schizo merg test
{0}merg_wr 8 byte port A
{0}merg_wr 4 byte port A
{0}* Map PCI B space
{0}* Schizo reg test
{0}PBM B registers
{0}Iommu B registers
{0}Streaming Cache B registers
{0}Mondo Interrupt B registers
{0}* Schizo pci B id test
{0}PCI B Vendor ID 108e
{0}PCI B Device ID 8001
{0}* Schizo mem test
{0}memtst ram data port B
{0}memtst cam data port B
{0}memtst ram addr port B
{0}memtst cam addr port B
{0}memtst pnta     port B
{0}memtst lnta     port B
```

CODE EXAMPLE 3-4 `diag-level` Variable Set to `min` (Single CPU) *(Continued) (7 of 8)*

```
{0}memtst rnta     port B
{0}memtst enta     port B
{0}memtst ln addr  port B
{0}memtst pg addr  port B
{0}memtst sbuf addr port B
{0}* Schizo merg test
{0}merg_wr 8 byte port B
{0}merg_wr 4 byte port B
{0}* Map PCI B space for RIO
{0}* RIO Config
{0}* RIO EBus access
{0}* Icache Functional
{0}Verify cacheline fill on read miss
{0}* Dcache Functional
{0}Verify no allocate on write miss
{0}Verify fetch from memory on read miss
{0}Verify write-through on write hit
{0}Verify write-through/fetch on read miss
{0}Verify set-associativity
{0}* Wcache Functional
{0}Verify cacheline fill on write miss
{0}Verify buffering
{0}Verify coalescing
{0}* Pcache Functional
{0}* FPU Functional
{0}Test single and double-precision addition
{0}Test single and double-precision subtraction
{0}Test single and double-precision multiplication
{0}Test single and double-precision division
{0}Test single and double-precision sqrt
{0}Test single and double-precision abs
{0}Test single and double-precision conversion
{0}* FPU Move To Registers
{0}Moving SP fp value through all fp registers
{0}Moving DP fp value through all fp registers
{0}* FPU Branch
{0}Testing Branching on fcc0
{0}Verify branching
{0}Verify no branching
{0}Testing Branching on fcc1
{0}Verify branching
{0}Verify no branching
{0}Testing Branching on fcc2
{0}Verify branching
```

CODE EXAMPLE 3-4 `diag-level` Variable Set to `min` (Single CPU) *(Continued) (8 of 8)*

```
{0}Verify no branching
{0}Testing Branching on fcc3
{0}Verify branching
{0}Verify no branching
{0}* Ecache Functional
{0}Verify cacheline fill on read miss
{0}Verify write allocate on write miss
{0}Verify cacheline update on write hit
{0}Verify write back
{0}POST_END
```

3.4.3 POST Progress and Error Reporting

In most cases, POST also attempts to send a failure message to the POST monitoring system. The following code example identifies the typical appearance of a failure message.

Note – The system does not automatically boot if a POST error occurs; it halts at the `ok` prompt to alert the user to a failure.

CODE EXAMPLE 3-5 POST Error Message

```
{0}ERROR: TEST = * Memory marching Initial area TESTID = 68
{0}H/W under test = MAIN MEMORY
{0}     Fault address 00000000.00000090
{0}     Fault status 00000002.0000004f
{0}     (CE) Correctable system data ECC error
{0}     CPU data bit 6
{0}     Memory data bit 146
{0}     DIMM connector J0406
{0}     Connector pin 124
{0}     CPMS Slice 1
```

CHAPTER 4

Troubleshooting Procedures

This chapter describes how to troubleshoot possible hardware problems and suggests corrective actions.

This chapter contains the following topics:

4.1 Power-On Failure

This section provides examples of power-on failure symptoms and suggested actions.

Symptom

The system does not power up when you press the Power switch.

Action

Ensure that the AC power cord is properly connected to the system and to the wall receptacle. Verify that the wall receptacle is supplying AC power to the system.

Ensure that the cover is securely fastened to the chassis. If the cover is not installed, the power interlock will prevent power on of the system.

Press the Power switch. If the system does not power on, the CPU module(s) may not be properly seated. Inspect the CPU module(s) for proper seating, and press the Power switch again.

If the wall receptacle AC power has been verified and the CPU module(s) is properly seated, but the system does not power on, the system power supply may be defective. See Section 4.5 “Power Supply Troubleshooting” on page 4-5.

4.2 System LEDs

The power-indicator LED (FIGURE 1-2 on page 1-4) has three states that indicate the power status of the system (TABLE 4-1).

TABLE 4-1 Power-Indicator LED States

LED Activity	Meaning
LED off	System power is off or system is booting.
LED blinking	All internal subsystems are in lowest possible power consumption mode for this system*. *Some hardware components and software drivers do not support this system’s lowest possible power consumption mode. When this occurs, the power indicator LED will not blink.
LED on	Full power is on in one or more internal subsystems. and system self test has completed successfully.

The logo LED light indicates only that power is supplied to the system.

4.3 Video Output Failure

This section provides video output failure symptom and suggested action.

Symptom

No video at the system monitor.

Action

Ensure that the power cord is connected to the monitor and to the wall receptacle.

Verify that the wall receptacle is supplying AC power to the monitor.

Check the video cable connection between the monitor and the system graphics card output port at the rear of the system.

Check that each CPU module is properly seated. If the AC connection to the monitor is correct, the video cable is correctly connected, and each CPU module is properly seated, the system monitor or the system graphics card may be defective. Replace the monitor or the graphics card.

4.4 Hard Drive or DVD-ROM Drive Failure

This section provides hard drive and DVD-ROM drive failure symptoms and suggested actions.

Symptom

A hard drive read, write, or parity error is reported by the operating system or by customer application.

A DVD-ROM drive read error or parity error is reported by the operating system or by customer application.

Action

Replace the drive indicated by the failure message. The operating system identifies the internal drives, as listed in the following table.

TABLE 4-2 Internal Drives Identification

Operating System Address	Drive Physical Location and Target
`c1t1d0s#`	Lower hard drive, LiD / HA 1
`c1t2d0s#`	Upper hard drive, LiD / HA 2
`c0t6d0s#`	DVD-ROM drive, target 6 (optional)
`c0t5d0s#`	Tape drive, target 5 (optional)

Note – The # symbol in the operating system address examples is a numeral between 0 and 7 that describes the slice or partition on the drive.

Symptom

The DVD-ROM drive fails to respond to commands.

Action

Test the drive response to the `probe-scsi` command as follows.

Note – To bypass POST, type **`setenv diag-switch? false`** at the `ok` prompt.

At the system ok prompt type:

```
ok reset-all
ok probe-scsi-all
```

If the DVD-ROM drive responds correctly to `probe-scsi all`, the message identified in CODE EXAMPLE 4-5 on page 4-9 is displayed; the system SCSI controller has successfully probed the device. This is an indication that the motherboard is operating correctly. If the drive does not respond to the SCSI controller probe, replace the unresponsive drive.

4.5 Power Supply Troubleshooting

Caution – This procedure must be performed by a qualified, Sun Blade 1000 service-trained, maintenance provider. Persons who remove any of the outer panels to access this equipment must observe all safety precautions and comply with skill level requirements, certification, and all applicable local and national laws.

Caution – During the power supply voltage measurement checks, an operational load must be on the power supply. Ensure that the power supply cables remain connected to the motherboard.

The section describes how to use a DVM to test the power supply under operational load. See the figures and tables in this section to identify the J3601 and J3603 power connectors.

1. **Power off the system and remove the access panel.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Defeat the interlock.**

   The interlock switch can be defeated by mechanically closing the switch while the access cover is removed from the system.

Caution – Hazardous voltage are present. To reduce the risk of electrical shock and danger to personal health, follow the instructions.

3. **Power on the system.**

4. **Using a DVM, check the power supply output voltages.**

   See Section B.1 “Power Connectors” on page B-2 and for power supply connector descriptions.

Note – All power supply connectors being tested must remain connected to the motherboard.

   a. **With the negative probe of the DVM placed on a connector ground (Gnd) pin, position the positive probe on each power pin.**

   b. **Verify voltage and signal availability as listed in the voltage-pin tables.**

5. **If any power pin signal is not present with the power supply active and properly connected to the motherboard, replace the power supply.**

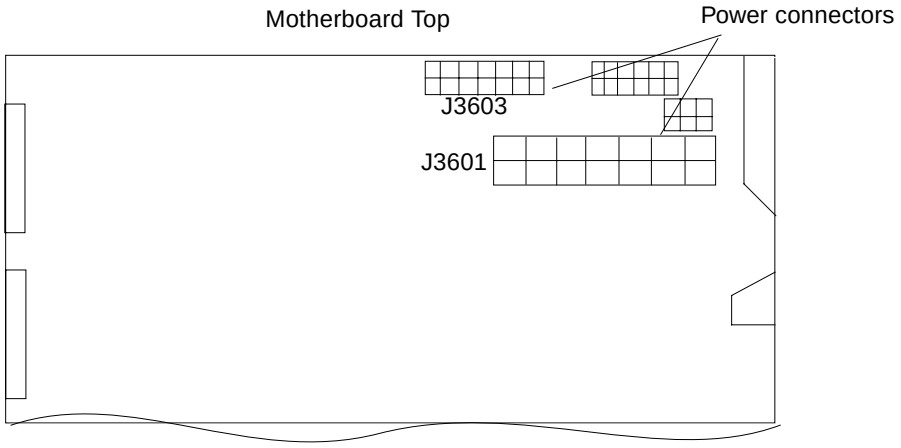

FIGURE 4-1 Power Supply Connector Jack Location

4.6 DIMM Failure

The operating system, diagnostic program, or POST may not always display a DIMM location (U number) as part of a memory error message. In this situation the only available information is a physical memory address and failing byte (or bit).

4.7 OpenBoot PROM On-Board Diagnostics

The following sections describe the OpenBoot PROM on-board diagnostics. To execute the OpenBoot PROM on-board diagnostics, the system must be at the `ok` prompt.

4.7.1 Watch-Clock Diagnostic

The watch-clock diagnostic displays the result as a seconds counter. During normal operation, the seconds counter repeatedly increments from 0 to 59. Initialize the watch-clock diagnostic by typing the `watch-clock` command at the `ok` prompt.

The following code example identifies the watch-clock diagnostic output message.

CODE EXAMPLE 4-1 Watch-Clock Diagnostic Output Message

```
{0} ok watch-clock
Watching the ‘seconds’ register of the real time clock chip.
It should be ‘ticking’ once a second.
Type any key to stop.
4
```

4.7.2 Watch-Net and Watch-Net-All Diagnostics

The watch-net and watch-net-all diagnostics monitor Ethernet packets on the Ethernet interfaces connected to the system. Good packets received by the system are indicated by a period (.). Errors such as the framing error and the cyclic redundancy check (CRC) error are indicated with an X and an associated error description. Initialize the watch-net diagnostic is by typing the `watch-net` command at the `ok` prompt and initialize the watch-net-all diagnostic by typing the `watch-net-all` command at the `ok` prompt.

The following code examples identify the watch-net and the watch-net-all output messages.

CODE EXAMPLE 4-2 Watch-Net Diagnostic Output Message

```
{0} ok watch-net
Internal loopback test -- succeeded.
Link is -- up
Looking for Ethernet Packets.
‘.’ is a Good Packet. ‘X’ is a Bad Packet.
Type any key to stop.............................
```

CODE EXAMPLE 4-3 Watch-Net-All Diagnostic Output Message

```
{0} ok watch-net-all
/pci@8,700000/network@5,1
Internal loopback test -- succeeded.
Link is -- up
Looking for Ethernet Packets.
‘.’ is a Good Packet. ‘X’ is a Bad Packet.
Type any key to stop.
```

4.7.3 Probe-SCSI and Probe-SCSI-All Diagnostics

The probe-SCSI diagnostic transmits an inquiry command to internal and external FC-AL and SCSI devices connected to the system on-board SCSI or FC-AL interface. If the SCSI device is connected and active, the target address, unit number, device type, and manufacturer name are displayed.

The probe-SCSI-all diagnostic transmits an inquiry command to all devices connected to the system. The first identifier listed in the display is the SCSI host adapter address in the system device tree followed by the SCSI device identification data.

Initialize the probe-SCSI diagnostic by typing the `probe-scsi` command at the `ok` prompt and initialize the probe-SCSI-all diagnostic by typing the `probe-scsi-all` command at the `ok` prompt.

The following code examples identify the probe-SCSI and the probe-SCSI-all diagnostic output messages.

CODE EXAMPLE 4-4 Probe-SCSI Diagnostic Output Message

```
ok probe-scsi
LiD HA --- Port WWN ---      ---- Disk description ----
1   1  210000203700ca78  SEAGATE ST39103FCSUN9.0G01479916021084
3   3  210000203708ad4d  SEAGATE ST39102FCSUN9.0G09299906F45038
ok
```

CODE EXAMPLE 4-5 Probe-SCSI-All Output Message

```
ok probe-scsi-all
/pci@8,600000/scsi@4
LiD HA  --- Port WWN ---      ---- Disk description ----
3   3  210000203708ad4d  SEAGATE ST39102FCSUN9.0G09299906F45038
1   1  210000203700ca78  SEAGATE ST39103FCSUN9.0G01479916021084
/pci@8,700000/scsi@6,1
Target 0
 Unit 0   Disk     SEAGATE ST39173W SUN9.0G2815
/pci@8,700000/scsi@6

Target 6
 Unit 0  Removable Read Only device   TOSHIBA DVD-ROM SD-M12011B08

ok
```

4.7.4 Test *alias name, device path, -all* Diagnostic

The test diagnostic, combined with a device alias or device path, enables a device self-test program. If a device has no self-test program, the message `No selftest method for device name` is displayed. To enable the self-test program for a device, type the `test` command, followed by the device alias or device path name.

The following code example identifies the test output message. TABLE 4-3 lists `test` *alias name* selections, their descriptions, and their required preparation.

Note – The diskette drive is selected as the test *alias name* example.

CODE EXAMPLE 4-6 Test Output Message

```
ok test floppy
Testing floppy
```

TABLE 4-3 Selected OpenBoot PROM On-Board Diagnostic Tests

Type of Test	Description	Preparation
`test screen`	Tests system video graphics hardware and monitor.	`diag-switch?` NVRAM parameter must be true for the test to execute.
`test floppy`	Tests diskette drive response to commands.	A formatted diskette must be inserted into the diskette drive.
`test net`	Performs internal / external loopback test of the system auto-selected Ethernet interface.	An Ethernet cable must be attached to the system and to an Ethernet tap or hub. If the Ethernet cable is not correctly attached the external loopback test will fail.
`test-all`	Sequentially tests system-configured devices containing selftest.	Tests are sequentially executed in device-tree order (viewed with the `show-devs` command).

4.7.5 Graphics Card

The graphics card contains a built-in diagnostic test that is enabled through the OpenBoot PROM. The graphics card built-in diagnostic test verifies basic graphics functionality without booting the operating system software.

To execute the built-in diagnostic test, the system must be at the `ok` prompt.

To initilize the graphics card diagnostic

1. **At the** ok **prompt, type**:

```
ok setenv diag-switch? true
diag-switch? = true
```

2. **At the** ok **prompt, type**:

```
ok test screen
ok test screen
Testing screen
Starting IFB Selftest
 (This will take an estimated
 2-4 minutes for the full test)
Direct access frame buffer test:
    address test ovl0 pass
    address test ovl1 pass
    pattern test ovl0 00 ff a5 5a pass
    pattern test ovl1 00 ff a5 5a pass
  passed
Frame buffer color test:
    The frame buffer will be painted with:
       red in the top third
       green in the middle third
       blue in the bottom third.
Direct Burst memory test:
    address test db mem pass
    pattern test db mem 00 ff a5 5a pass
ok
```

3. **When the graphics card on-board diagnostics are completed type**:

```
ok setenv diag-switch? false
diag-switch? = false
```

4.8 OpenBoot Diagnostics

The OpenBoot diagnostics is a menu-driven set of diagnostics that reside in flash PROM on the motherboard. OpenBootDiag can isolate errors in the following system components:

- Motherboard

- Diskette drive
- DVD-ROM drive
- Hard drive
- Any option card that contains an onboard self-test

OpenBootDiag performs root-cause failure analysis on the referenced devices by testing internal registers, confirming subsystem integrity, and verifying device functionality.

On the motherboard, OpenBootDiag tests not only the motherboard but also its interfaces:

- PCI
- SCSI
- Ethernet
- Serial
- Parallel

4.8.1 Starting the OpenBootDiag Menu

This section contains the following OpenBootDiag diagnostic information:

Note – Set the `diag-level` variable to `min` prior to performing these tests. This may be done at the `ok prompt` or within the `obdiag` menu.

Perform the following steps to start OpenBootDiag:

1. **At the** ok **prompt, type:**

```
ok setenv mfg-mode on
mfg-mode = on
```

2. **Then type:**

```
ok setenv diag-switch? true
diag-switch? = true
```

3. **Then type:**

```
ok setenv auto-boot? false
auto-boot? = false
```

4. **Then type:**

```
ok reset-all
```

5. **Verify that the platform resets (see the following code example).**

CODE EXAMPLE 4-7 Reset All

```
ok reset-all
Resetting...
@(#)  4.0 common-23 Version 23 created 2000/04/19 16:09
Clearing TLBs Done
Reset: 0000.0000.0000.0010 SPOR
Loading Configuration
Membase: 0000.0000.0000.0000
MemSize: 0000.0000.2000.0000
Init CPU arrays Done
Init E$ tags Done
Setup TLB Done
MMUs ON
Block Scrubbing Done
Copy Done
PC = 0000.07ff.f000.2f84
```

CODE EXAMPLE 4-7 Reset All

```
PC = 0000.0000.0000.2ff8


Decompressing Done
Size = 0000.0000.0006.da00
ttya initialized
Start Reason: Soft Reset
System Reset: (SPOR)
Probing gptwo at 0,0 SUNW,UltraSPARC-III (400 MHz @ 4:1, 4 MB)
memory controller

Probing gptwo at 1,0 Nothing there
Probing gptwo at 8,0 pci pci upa ppm
Loading Support Packages: kbd-translator
Loading onboard drivers: ebus flashprom bbc ppm i2c dimm dimm dimm
dimm
  nvram idprom i2c cpu sensor fan-control card-reader motherboard
beep
   audio rtc gpio pmc floppy parallel serial
Memory Configuration:
Segment @ Base:        0  Size:   512 MB ( 2-Way)
Can't read mem-layout table from sys SEEPROM.  Using default!

WARNING: HOSTID data should be moved to socketed SEEPROM!
HW support required for hostid reprogramming!

Probing /upa@8,480000 Device 0,0 Nothing there
Probing /upa@8,480000 Device 1,0 Nothing there
Probing /pci@8,600000 Device 4  scsi disk
Probing /pci@8,600000 Device 1  Nothing there
Probing /pci@8,700000 Device 5  network firewire usb
Probing /pci@8,700000 Device 6  scsi disk tape scsi disk tape
Probing /pci@8,700000 Device 1  Nothing there
Probing /pci@8,700000 Device 2  Nothing there
Probing /pci@8,700000 Device 3  Nothing there
Probing /pci@8,700000 Device 4  Nothing there

(UltraSPARC-III), No Keyboard
OpenBoot 4.0 common-23, 512 MB memory installed, Serial #8839885.
Ethernet address 8:0:20:86:e2:cd, Host ID: 8086e2cd.
```

6. **At the** `ok` **prompt, type** `obdiag`**. Verify that the OBDiag menu is displayed (**CODE EXAMPLE 4-8**).**

CODE EXAMPLE 4-8 OBDiag Menu

```
                              o b d i a g

1 SUNW,glc@4          2 audio@1,200000          3 bbc@1,0
4 ebus@5              5 firewire@5,2            6 flashprom@0,0
7 floppy@1,3023f0     8 gpio@1,300600           9 i2c@1,2e
10 i2c@1,30           11 network@5,1            12
                                                parallel@1,300278
13 pmc@1,300700       14 rtc@1,300070           15 scsi@6
16 scsi@6,1           17 serial@1,400000        18 usb@5,3

|Commands:test test-all except help what printenvs setenv versions
exit|
```

The following menu is displayed when the `help` command is executed.

Command	Description
`exit`	Exits obdiag tool
`help`	Prints this help information
`setenv`	Sets diagnostic configuration variable to new value
`printenvs`	Prints values for diagnostic configuration variables
`versions`	Prints self tests, library and obdiag tool versions
`test-all`	Tests all devices displayed in the menu
`test 1,2,5`	Tests devices 1, 2 and 5
`except 2,5`	Tests all devices except devices 2 and 5
`what 1,2,5`	Prints some selected properties for devices 1, 2, and 5

4.8.2 QLC Diagnostic Output Message

The following code example shows the QLC test output.

CODE EXAMPLE 4-9 QLC Diagnostic Output Message

CODE EXAMPLE 4-10 QLC Diagnostic Output Message

```
obdiag> test 01
Hit the spacebar to interrupt testing
Testing /pci@8,600000/SUNW,qlc@4.............passed
Hit any key to return to main menu
```

4.8.3 Audio Output Message

The following code example shows the Audio output message.

CODE EXAMPLE 4-11 Audio Diagnostic Output Message

```
obdiag> test 02
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/audio@1,200000.........passed
Hit any key to return to the main menu
```

4.8.4 bbc@1,0 Output Message

The following code example shows the bbc@1,0 output message.

CODE EXAMPLE 4-12 bbc@1,0 Diagnostic Output Message

```
obdiag> test 03
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/bbc@1,0
............................... passed

Hit any key to return to the main menu
```

4.8.5 ebus@5 Output Message

The following code example shows the ebus output message.

CODE EXAMPLE 4-13 ebus@5 Diagnostic Output Message

```
obdiag> test 04
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5
..................................... passed

Hit any key to return to the main menu
```

4.8.6 firewire@5,2 Output Message

The following code example shows the firewire output message.

CODE EXAMPLE 4-14 Firewire Output Message

```
obdiag> test 05
Hit the spacebar to interrupt testing
Testing /pci@8,700000/firewire@5,2
.................................. passed

Hit any key to return to the main menu
```

4.8.7 flashprom@0,0 Output Message

The following code example shows the flashprom output message.

CODE EXAMPLE 4-15 Flashprom@0,0 Output Message

```
obdiag> test 06
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/flashprom@0,0
.............................. passed

Hit any key to return to the main menu
```

4.8.8 Floppy Output Message

The floppy diagnostic verifies the diskette drive controller initialization. It also validates the status of a selected disk drive and reads the diskette drive header.

The following code example shows the floppy output message.

CODE EXAMPLE 4-16 Floppy Diagnostic Output Message

```
obdiag> test 07
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/floppy@1,3023f0
.......................... passed

Hit any key to return to the main menu
```

4.8.9 gpio@1,300600 Output Message

The following code example shows the gpio output message.

CODE EXAMPLE 4-17 gpio Output Message

```
obdiag> test 08
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/gpio@1,300600
.......................... passed

Hit any key to return to the main menu
```

4.8.10 i2c@1,2e Output Message

The following code example shows the i2c1,2e output message.

CODE EXAMPLE 4-18 I2c@1,2e Diagnostic Output Message with Tip Line Installed

```
obdiag> test 09
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/i2c@1,2e
.............................. passed

Hit any key to return to the main menu
```

4.8.11 i2c@1,30 Output Message

The following code example shows the i2c1,30 output message.

CODE EXAMPLE 4-19 I2c@1,30 Diagnostic Output Message

```
obdiag> test 10
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/i2c@1,30
.............................. passed

Hit any key to return to the main menu
```

4.8.12 network@5,1 Output Message

The following code example shows the network@5,1 output message.

CODE EXAMPLE 4-20 Network@5.1 Diagnostic Output Message

```
obdiag> test 11
Hit the spacebar to interrupt testing
Testing /pci@8,700000/network@5,1
................................... passed

Hit any key to return to the main menu
```

4.8.13 Parallel Port Output Message

The following code example shows the parallel port output message.

CODE EXAMPLE 4-21 Parallel Port Diagnostic Output Message

```
obdiag> test 12
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/parallel@1,300278
..................... passed

Hit any key to return to the main menu
```

4.8.14 pmc@1,300700 Output Message

The following code example shows the pmc@1,300700 output message.

CODE EXAMPLE 4-22 pmc@1,300700 Output Message

```
obdiag> test 13
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/pmc@1,300700
........................... passed

Hit any key to return to the main menu
```

4.8.15 rtc@1,300070 Output Message

The following code example shows the rtc@1,300070 output message..

CODE EXAMPLE 4-23 rtc@1,300070 Diagnostic Output Message

```
obdiag> test 14
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/rtc@1,300070
.............................. passed

Hit any key to return to the main menu
```

4.8.16 scsi@6 Output Message

The following code example shows the scsi@6 output message

CODE EXAMPLE 4-24 scsi@6 Diagnostic Output Message

CODE EXAMPLE 4-25

```
obdiag> test 15
Hit the spacebar to interrupt testing
Testing /pci@8,700000/scsi@6
.........................................passed
```

4.8.17 scsi@6,1 Output Message

The following code example shows the scsi@6,1 output message.

CODE EXAMPLE 4-26 scsi@6 Diagnostic Output Message

```
obdiag> test 16
Hit the spacebar to interrupt testing
Testing /pci@8,700000/scsi@6,1
..................................... passed

Hit any key to return to the main menu
```

4.8.18 Serial Output Message

The following code example shows the serial output message.

CODE EXAMPLE 4-27 Serial Diagnostic Output Message

```
obdiag> test 17
Hit the spacebar to interrupt testing
Testing /pci@8,700000/ebus@5/serial@1,400000
....................... passed

Hit any key to return to the main menu
```

4.8.19 USB Output Message

The following code example shows the USB output message.

CODE EXAMPLE 4-28 Serial Diagnostic Output Message

```
obdiag> test 18
```

CODE EXAMPLE 4-28 Serial Diagnostic Output Message

```
Hit the spacebar to interrupt testing
Testing /pci@8,700000/usb@5,3
..................................... passed

Hit any key to return to the main menu
```

4.8.20 Test-All Output Message

The test-all diagnostic runs all tests in sequence.

Note – You may exclude certain tests using the except command.

The following code example shows the test-all output message.

CODE EXAMPLE 4-29 Test-all Diagnostic Output Message

```
obdiag> test-all
Hit the spacebar to interrupt testing
Testing /pci@8,600000/SUNW,qlc@4.....................passed
Testing /pci@8,700000/ebus@5/audio@1,200000 ....... ....passed
Testing /pci@8,700000/ebus@5/bbc@1,0 ................. passed
Testing /pci@8,700000/ebus@5 ......................... passed
Testing /pci@8,700000/firewire@5,2 ................... passed
Testing /pci@8,700000/ebus@5/flashprom@0,0 ............ passed
Testing /pci@8,700000/ebus@5/floppy@1,3023f0... ....... passed
Testing /pci@8,700000/ebus@5/gpio@1,300600 ............ passed
Testing /pci@8,700000/ebus@5/i2c@1,2e ................. passed
Testing /pci@8,700000/ebus@5/i2c@1,30 ................. passed
Testing /pci@8,700000/network@5,1 ..................... passed
Testing /pci@8,700000/ebus@5/parallel@1,300278 ........ passed
Testing /pci@8,700000/ebus@5/pmc@1,300700 .............passed
Testing /pci@8,700000/ebus@5/rtc@1,300070 .............passed
Testing /pci@8,700000/scsi@6 ......................... passed
Testing /pci@8,700000/scsi@6,1 ....................... passed
Testing /pci@8,700000/ebus@5/serial@1,400000 ..........passed
Testing /pci@8,700000/usb@5,3 .........................passed
Hit any key to return to the main menu
```

CHAPTER 5

Preparing for Component Removal and Replacement

This chapter describes how to prepare for removal and replacement of internal system components.

Note – It is very important that you review the safety requirements, safety symbols, and safety precautions in this chapter before you begin to remove or replace system components.

This chapter contains the following topics:

5.1 Safety Requirements

For your protection, observe the following safety precautions when setting up the equipment:

- Follow all cautions, warnings, and instructions marked on the equipment.
- Ensure that the voltages and frequency rating of the power receptacle match the electrical rating label on the equipment.
- Never push objects of any kind through openings in the equipment. They may touch dangerous voltage points or may short components, resulting in fire or electric shock.
- Refer the servicing of equipment to qualified personnel.

5.2 Safety Symbols

Note the following symbols and their meanings:

Caution – To avoid personal injury and equipment damage, follow the instructions.

Caution – Hazardous voltages are present. To reduce the risk of electric shock and personal injury, follow the instructions.

Caution – Avoid contact. Surfaces are hot and may cause personal injury if touched.

5.3 Safety Precautions

Follow all safety precautions.

5.3.1 Modification to Equipment

Caution – Do not make mechanical or electrical modifications to the equipment. Sun Microsystems is not responsible for regulatory compliance of a modified Sun product.

5.3.2 Placement of a Sun Product

Caution – To ensure reliable operation of the Sun product and to protect it from overheating, ensure that equipment openings are not blocked or covered. Never place a Sun product near a radiator or hot air register.

5.3.3 Power Cord Connection

Caution – Not all power cords have the same current ratings. Household extension cords do not have overload protection. Do not use household extension cords with a Sun product.

Caution – The power switch on this product functions as a standby-type device only. The power cord serves as the primary disconnect device for the system. Be sure to connect the power cord into a grounded electrical receptacle that is near the system and is readily accessible. Do not connect the power cord when the power supply has been removed from the system chassis.

5.3.4 Electrostatic Discharge

Caution – The boards and hard drives contain electronic components that are extremely sensitive to static electricity. Ordinary amounts of static electricity from clothing or the work environment can destroy components. Do not touch the components themselves or any metal parts. Wear an antistatic wrist strap when handling the drive assemblies, boards, or cards.

Caution – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system components, attach an ESD strap to your wrist and then to a metal area on the chassis. Then disconnect the power cord from the system and the wall receptacle. Following this caution equalizes all electrical potentials with the system.

5.3.5 Lithium Battery

Caution – This system contains a replaceable lithium battery, part number 150-2850. Lithium batteries may explode if mishandled. Do not dispose of a battery in fire. Do not disassemble a battery or attempt to recharge it.

5.4 Tools Required

The following tools are required for servicing the Sun Blade 1000 system.

- No. 2 Phillips screwdriver (magnetized tip suggested)
- Needle-nose pliers
- Grounding wrist strap
- CPU module torque-indicator tool, located in the hard drive bracket
- Digital voltage meter (DVM)
- Antistatic mat
- 5/16-inch nut driver

Place ESD-sensitive components such as the motherboard, circuit cards, hard drives, and SEEPROM, on an antistatic mat. The following items can be used as an antistatic mat:

- Bag used to wrap a Sun replacement part
- Shipping container used to package a Sun replacement part
- Inner side (metal part) of the system cover
- Sun ESD mat, part number 250-1088 (available through your Sun sales representative)
- Disposable ESD mat (shipped with replacement parts or optional system features)

5.5 Power Off the System

Caution – Prior to turning off the system power, save, back up, and close any open files. Notify affected users that you are powering off your system.

1. **To power off the system:**

   a. **If the Solaris OS *is* running in a windowing environment:**

      i. **Press and release the front panel Power switch (**FIGURE 5-1**) to automatically shut down all programs, the operating system, and to power off the system.**

      ii. **From the menu displayed on the system monitor, select “Shutdown”.**

   b. **If the Solaris OS *is not* running in a windowing environment:**

      i. **Press the front panel Power switch (**FIGURE 5-1**) to power off the system.**

      This action allows automatic shutdown of all programs, the operating system and to power off the system.

c. If the system is at the “ok”prompt (OpenBoot interface) press and hold the front panel Power swtich for four seconds (see FIGURE 5-1**) to power off the system.**

This action forces an immediate power off of the system.

Caution – Pressing the Power switch does not remove all power from the system; a trickle current remains in the power supply. To remove all power from the system, disconnect the power cord.

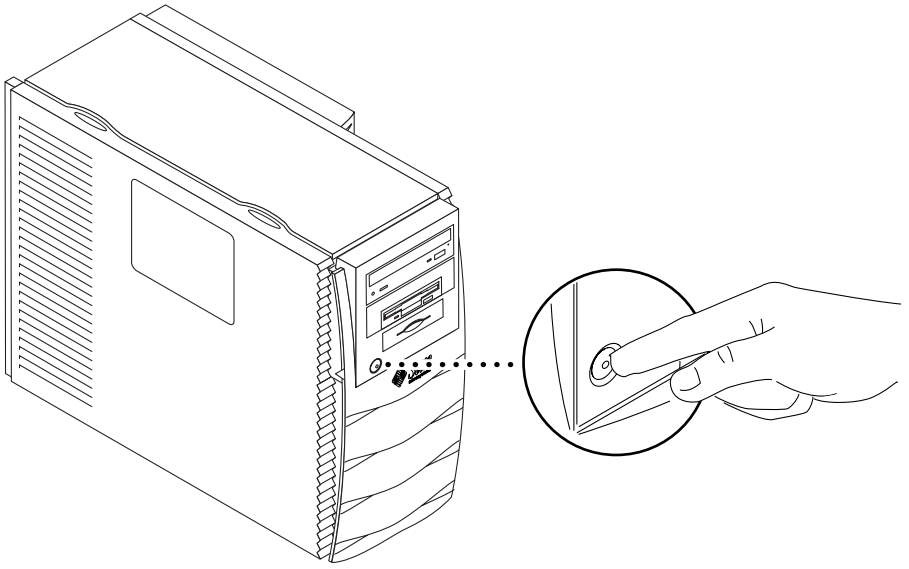

FIGURE 5-1 System Power Switch

2. Verify the following:

a. That the backlit Sun logo on the front panel is off.

b. That the system fans are not spinning.

Caution – Disconnect the power cord prior to servicing system components.

3. Turn off the power to the monitor and other external peripherals.

4. Disconnect cables to any peripheral equipment.

5. Remove the lock block, if one is installed (FIGURE 5-2**).**

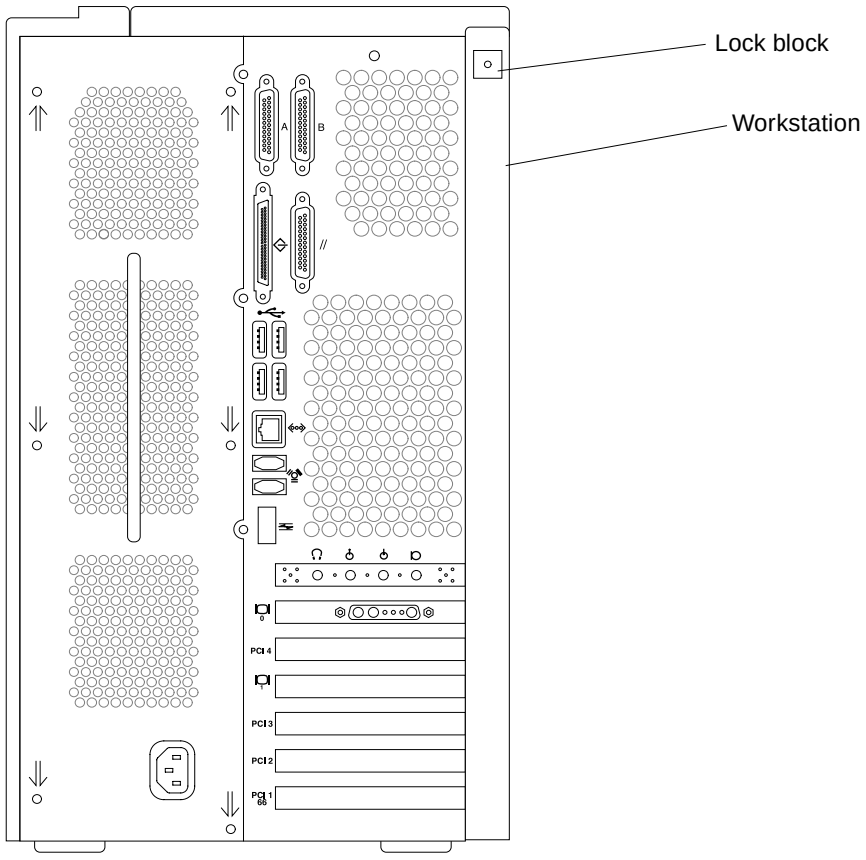

FIGURE 5-2 Lock Block Location

5.6 Removing the Access Panel

To remove the access panel (FIGURE 5-3):

Note – Removing the access panel activates the system power interlock circuit. If the power cord is connected, this safety mechanism prevents all DC voltages (except 5 VDC standby power) from reaching any internal components when the access panel is removed.

---

1. **Disconnect the system power cord.**
2. **Press down on the two depressions at the top of the access panel. Tilt the top of the access panel about an inch away from the chassis.**
3. **Lift the access panel up and off.**

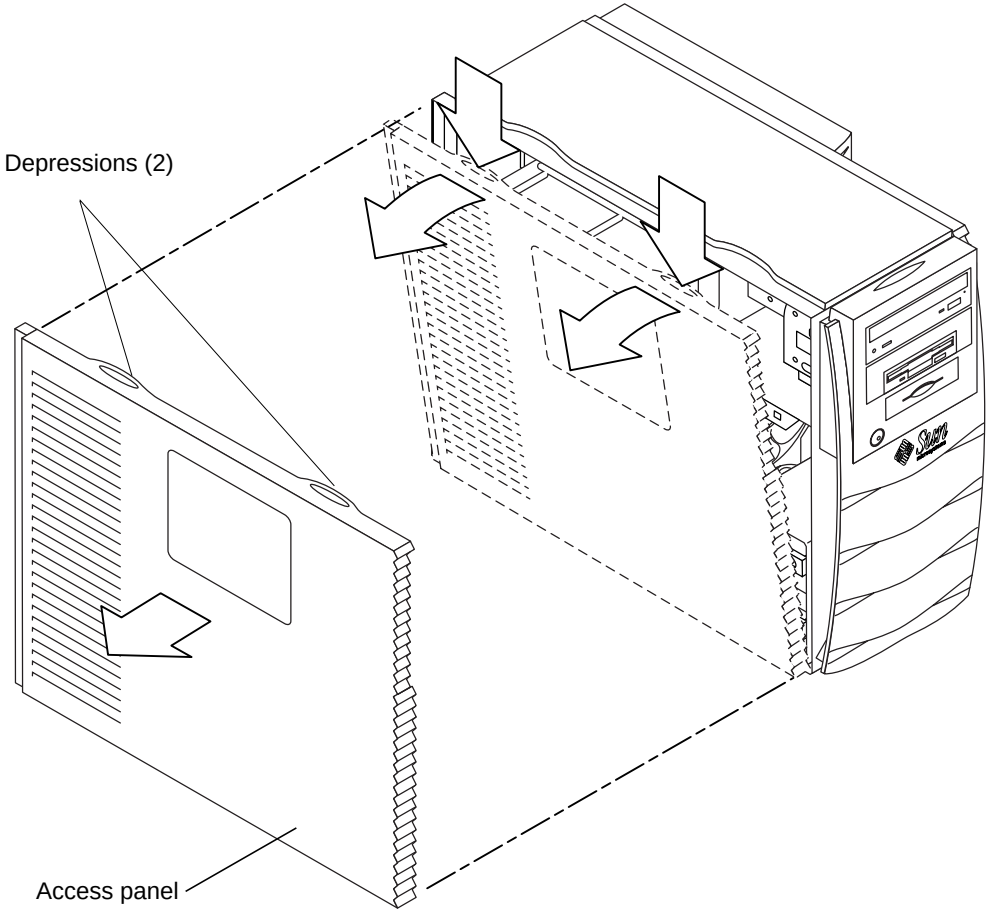

FIGURE 5-3 Removing the Access Panel

5.7 Attaching the Antistatic Wrist Strap

Caution – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system components, attach an ESD strap to your wrist and then to a metal area on the chassis. Then disconnect the power cord from the system and the wall receptacle. Following this caution equalizes all electrical potentials with the system.

1. **Unwrap the first two folds of the antistatic wrist strap and wrap the adhesive side firmly against your wrist.**
2. **Peel the liner from the copper foil at the opposite end of the antistatic wrist strap.**
3. **Attach the copper end of the antistatic wrist strap to the chassis (**FIGURE 5-4**).**
4. **Disconnect the power cord.**

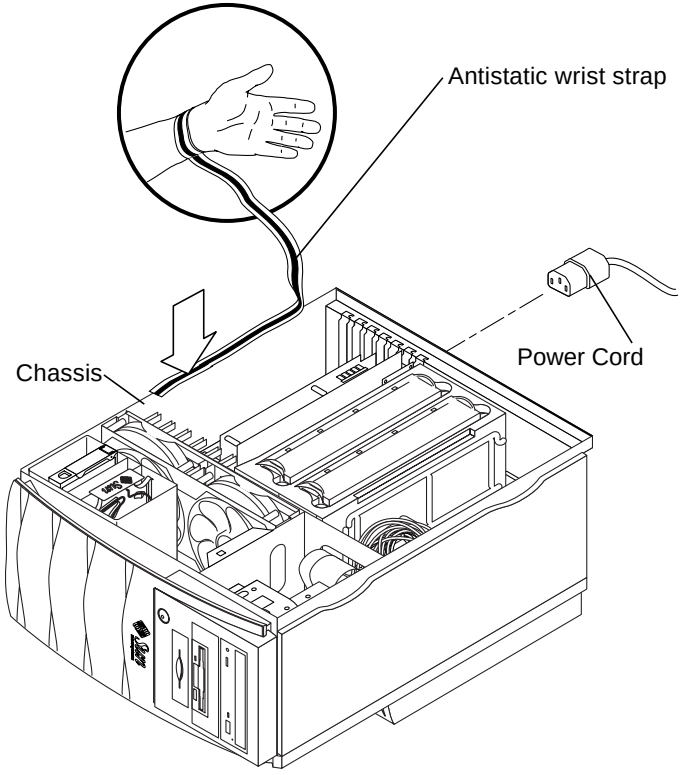

FIGURE 5-4 Attaching the Antistatic Wrist Strap to the Chassis

CHAPTER 6

Removing and Replacing Major Subassemblies

This chapter describes how to remove and replace the following major subassemblies:

6.1 Power Supply Assembly

Perform the following procedures to remove and replace the power supply assembly. If necessary, view the ShowMe How video clip located on the Sun Blade 1000 Hardware Documentation CD-ROM.

6.1.1 Removing the Power Supply Assembly

1. **Power off the system and remove the access panel.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Squeeze the connectors to disengage them from the motherboard. Now, disconnect the two power supply assembly connectors, J3601 and J3603, from the motherboard (**FIGURE 6-2**).**

3. **Loosen the reusable cable tie in the upper-right corner of the chassis cutout that secures the two power supply cables. (**FIGURE 6-1**)**

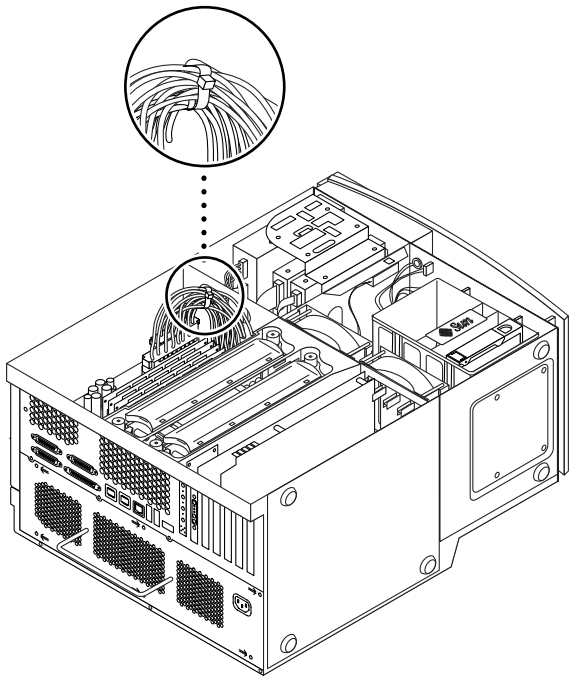

FIGURE 6-1 Power Supply Cable Tie

4. **Using a No. 2 Phillips screwdriver, remove the six screws securing the power supply assembly to the chassis back panel (**FIGURE 6-3**).**

5. **Remove the power supply from the chassis by pulling on the power supply assembly handle.**

   Push the power supply cable connectors through the chassis cutout while slowly pulling the power supply out.

Note – Support the power supply assembly with one hand as you remove it from the chassis.

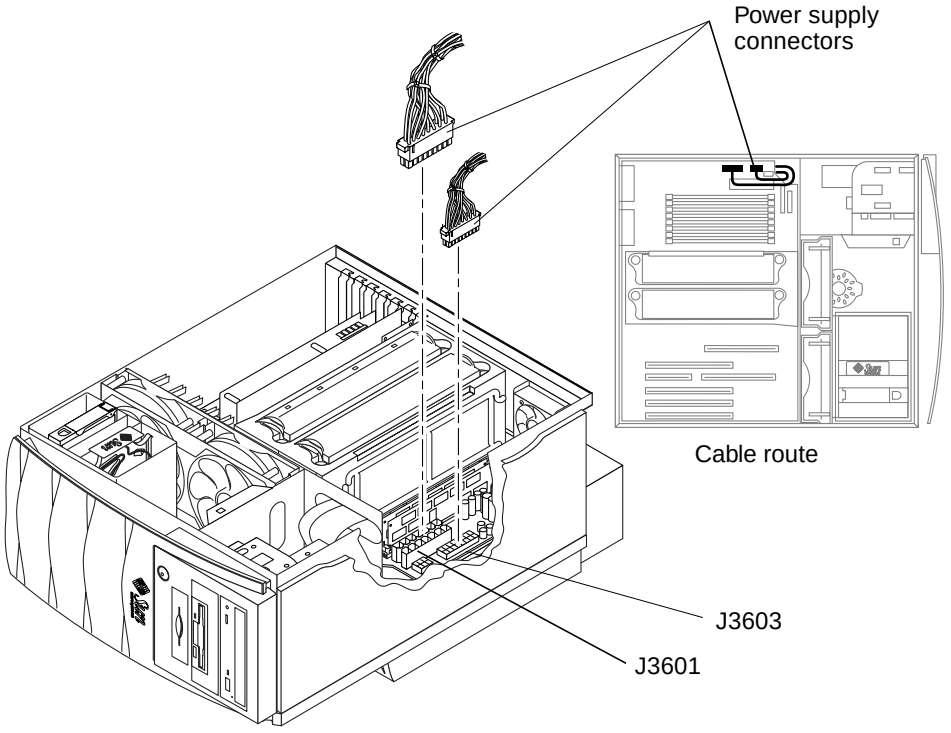

FIGURE 6-2 Removing and Replacing the Power Supply Assembly

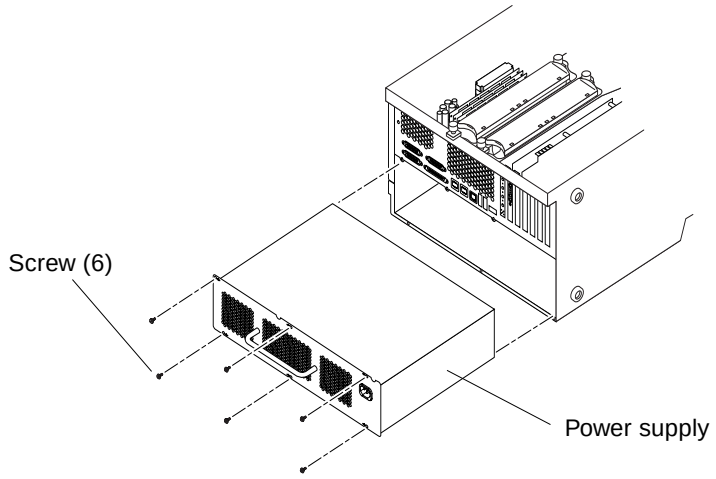

FIGURE 6-3 Removing and Replacing the connectors for the Power Supply Assembly

6.1.2 Replacing the Power Supply Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Tuck the power supply cables into the plastic retainer bracket (**FIGURE 6-4**).**

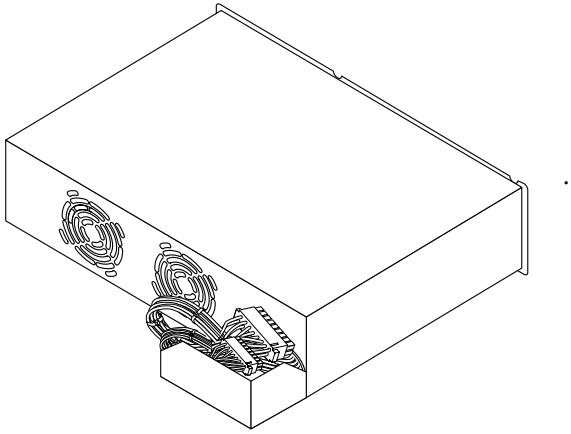

FIGURE 6-4 Dressing the Power Supply Cables

2. **Place the power supply into the chassis.**
3. **Tip up the front of the power supply as you slide it in the chassis, so that the front edge of the power supply engages the chassis tab under the motherboard.**
4. **Pull the power supply cables through the cutout at the upper-right corner of the motherboard.**
5. **Connect the power supply assembly connectors to the motherboard connectors J3601 and J3603 (**FIGURE 6-2**).**
6. **Attach the reusable cable tie around the power supply cables (**FIGURE 6-1**).**
7. **Using a No. 2 Phillips screwdriver, replace the six screws securing the power supply assembly to the chassis back panel (**FIGURE 6-3**).**
8. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

6.2 Power Switch Assembly

Use the following procedures to remove and replace the power switch assembly.

6.2.1 Removing the Power Switch Assembly

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Remove the peripheral bezel assembly by pressing on top of the bezel and tilting it out from the system chassis**.
3. **Using a 5/16-inch nutdriver, remove the nut securing the power switch assembly to the chassis (**FIGURE 6-5**).**
4. **Remove the combined cable assembly connectors from the power switch assembly terminators.**
5. **Remove the power switch assembly.**

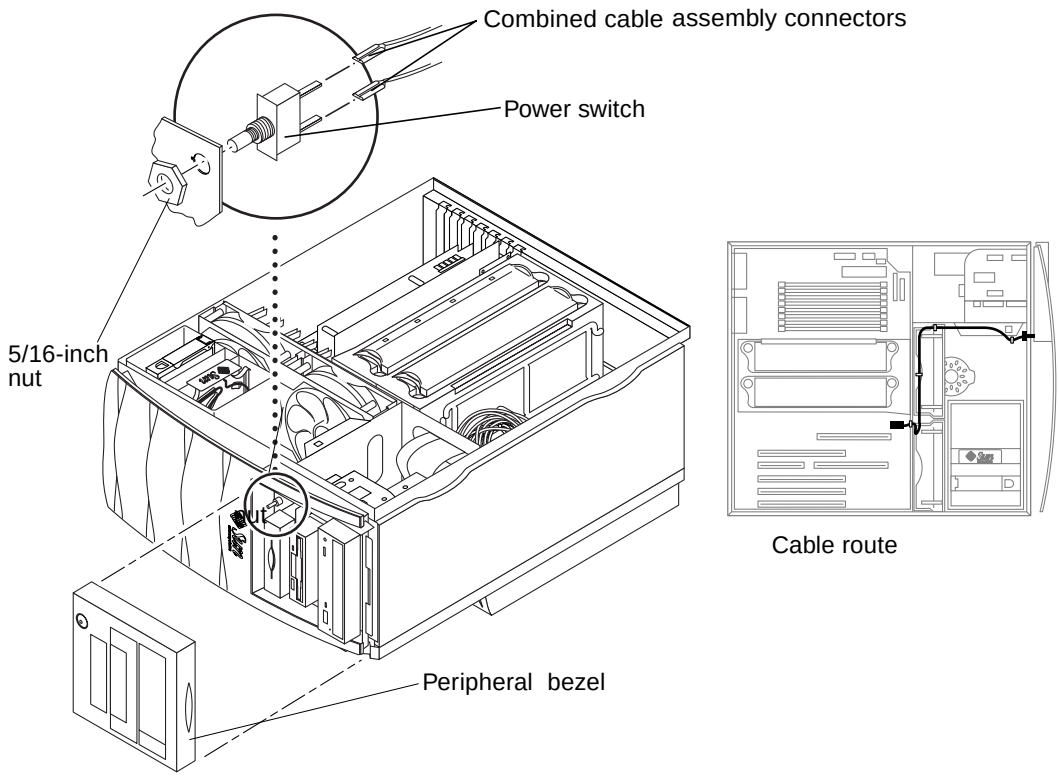

FIGURE 6-5 Removing and Replacing the Power Switch Assembly

6.2.2 Replacing the Power Switch Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position the power switch assembly in the chassis cutout (**FIGURE 6-5**).**
2. **Connect the combined cable assembly connectors to the power switch assembly terminators.**
3. **Using a 5/16-inch nutdriver, replace the nut securing the power switch assembly to the chassis.**

4. **Replace the peripheral bezel assembly.**

5. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

6.3 Cable Assemblies

Use the following procedures to remove and replace these assemblies:

- Peripheral power cable assembly
- SCSI cable assembly
- Diskette drive cable assembly
- Smart card reader cable assembly
- Combined cable assembly
- Logo LED cable assembly

Note – Unconnected portions of the peripheral power cable assembly should remain clipped inside the chassis.

6.3.1 Removing the Peripheral Power Cable Assembly

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

---

2. **Remove the fan assembly and fan bracket.**

   See Section 6.5.1 “Removing a Fan Assembly” on page 6-22 and Section 6.6.1 “Removing the Fan Bracket” on page 6-24.

3. **Partially remove the peripheral assembly to gain access to the peripheral connectors.**

   See Section 7.2 “Peripheral Assembly Drive” on page 7-3.

4. **Disconnect the peripheral power cable assembly as follows (**FIGURE 6-6**):**

a. Disconnect the peripheral power cable assembly connector from the motherboard connector J3608.

b. Disconnect the peripheral power cable assembly connectors from the tape drive, DVD-ROM drive, diskette drive and the FC-AL backplane assembly.

5. Lift the peripheral power cable assembly up and out of the chassis.

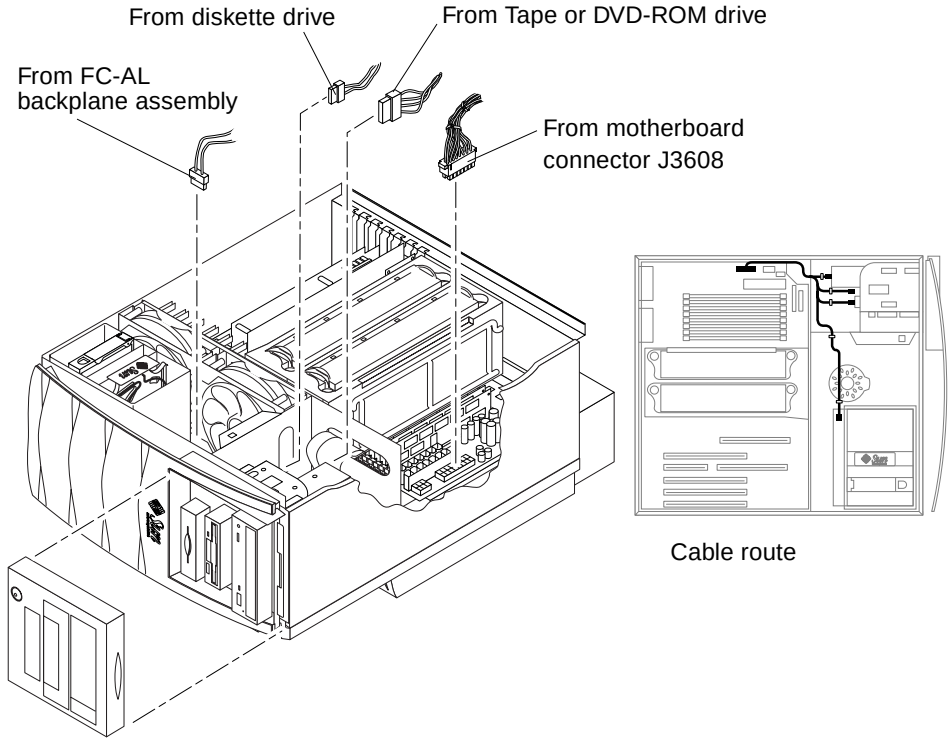

FIGURE 6-6 Removing and Replacing the Peripheral Power Cable Assembly

6.3.2 Replacing the Peripheral Power Cable Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. Position the peripheral cable assembly in the chassis (FIGURE 6-6**).**

2. Connect the peripheral power cable assembly as follows (FIGURE 6-6**):**

a. Connect the peripheral power cable assembly connectors to the tape drive or DVD-ROM drive, diskette drive and the FC-AL backplane assembly.

b. Connect the peripheral power cable assembly connector to the motherboard connector J3608.

3. Replace the fan assembly and fan bracket.

See Section 6.5.2 “Replacing a Fan Assembly” on page 6-23 and Section 6.6.2 “Replacing the Fan Bracket” on page 6-25.

4. Reinstall the partially removed peripheral assembly removed earlier.t

5. Detach the antistatic wrist strap, replace the access panel, and power on the system.

See Chapter 9 “Finishing Replacement Procedures.”

6.3.3 Removing the SCSI Cable Assembly

1. Power off the system, remove the access panel, and attach the antistatic wrist strap.

See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Disconnect the SCSI cable assembly as follows (FIGURE 6-7**):**

a. Disconnect the SCSI cable assembly from the from the Tape or DVD-ROM drive.

b. Pass the SCSI cable assembly through the chassis cutout.

Lift the SCSI cable assembly out of the sheet metal cable guides.

c. Disconnect the SCSI cable assembly from the motherboard connector J5002.

d. Remove the SCSI cable assembly from the chassis.

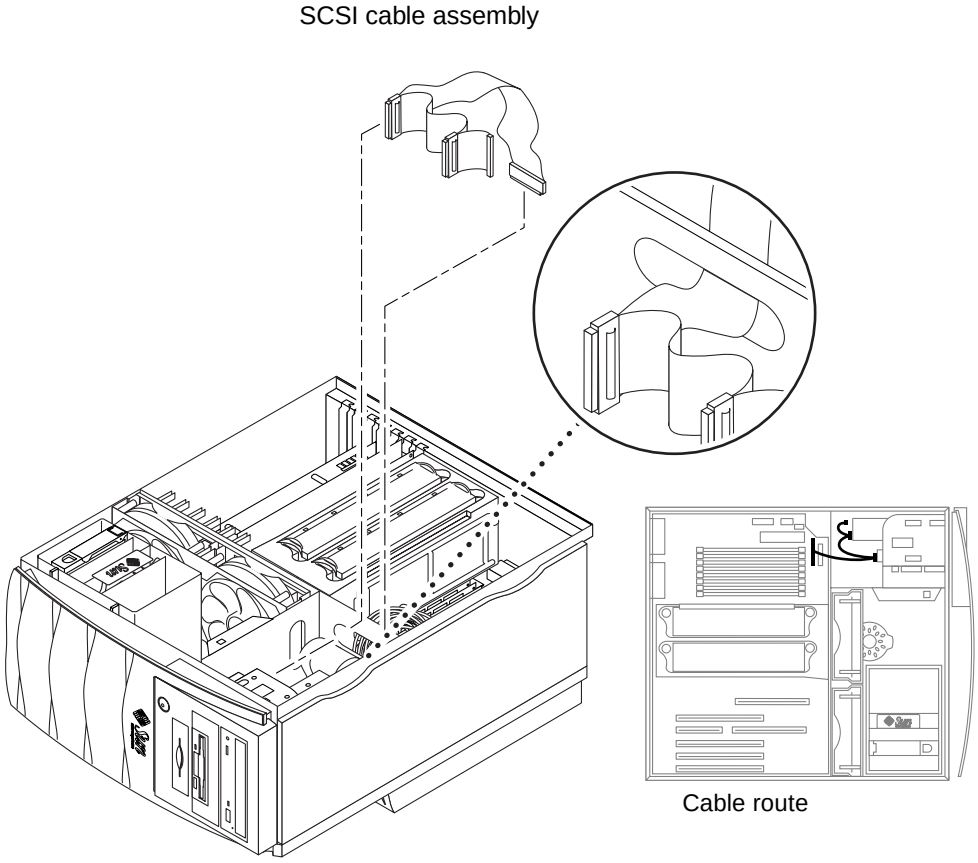

FIGURE 6-7 Removing and Replacing the SCSI Cable Assembly

6.3.4 Replacing the SCSI Cable Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Connect the SCSI cable assembly as follows (**FIGURE 6-7**):**

   a. **Pass the SCSI cable assembly through the chassis cutout.**

      Route the SCSI cable assembly through the sheet metal cable guides.

   b. **Connect the SCSI cable assembly to connector J5002 on the motherboard.**

c. **Connect the SCSI cable assembly connector to the Tape or DVD-ROM drive.**

2. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

6.3.5 Removing the Diskette Drive Cable Assembly

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Disconnect the SCSI cable assembly at the motherboard connector J5002.**
3. **Disconnect the diskette drive cable assembly as follows (**FIGURE 6-8**):**
   a. **Disconnect the diskette drive cable assembly from the motherboard diskette drive connector J1801.**
   b. **Disconnect the diskette drive cable assembly from the rear of the diskette drive.**
4. **Feed the SCSI and diskette drive cables through the chassis cutout.**
5. **Remove the diskette drive cable assembly.**

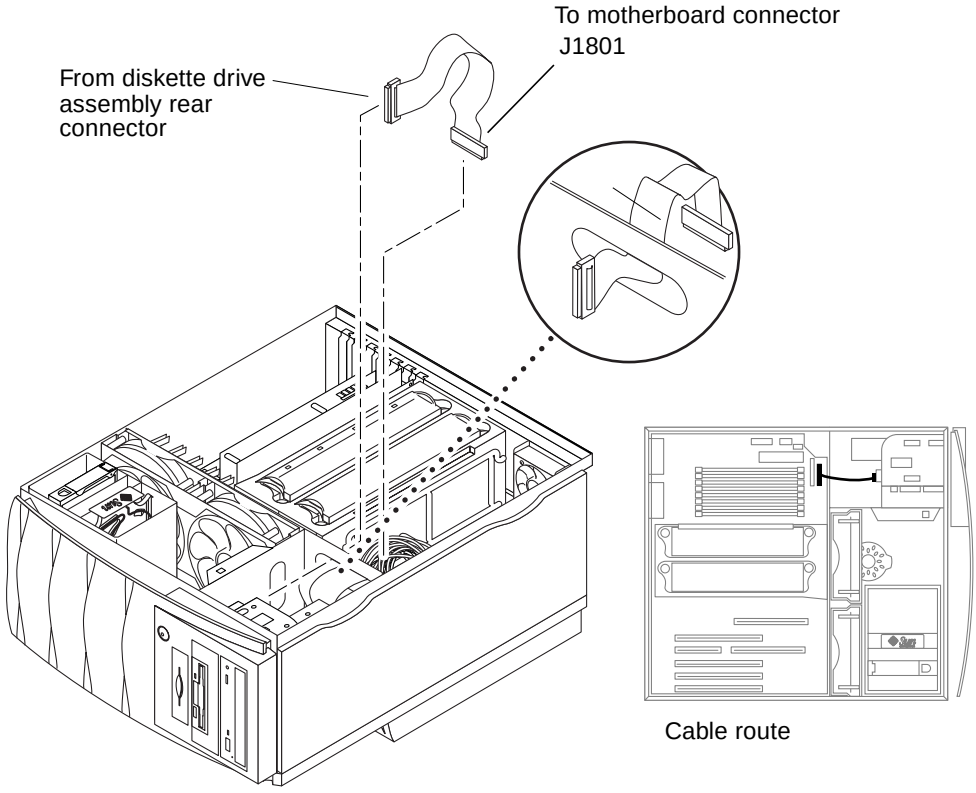

FIGURE 6-8 Removing and Replacing the Diskette Drive Cable Assembly

6.3.6 Replacing the Diskette Drive Cable Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position the diskette drive cable assembly in the chassis (**FIGURE 6-8**).**
2. **Connect the diskette drive cable assembly as follows (**FIGURE 6-8**):**
   a. **Connect the diskette drive cable assembly to the motherboard diskette drive connector J1801.**
   b. **Feed the diskette drive cable through the chassis cutout.**

c. Feed the SCSI cable through the chassis cutout.

d. Connect the diskette drive cable assembly to the rear of the diskette drive.

e. Connect the SCSI cable to J5002.

3. Detach the antistatic wrist strap, replace the access panel, and power on the system.

See Chapter 9 “Finishing Replacement Procedures.”

6.3.7 Removing the Smart Card Reader Cable Assembly

1. Power off the system, remove the access panel, and attach the antistatic wrist strap.

See Chapter 5 “Preparing for Component Removal and Replacement.”

2. Disconnect the smart card reader cable assembly from the smart card reader (FIGURE 6-9**).**

3. Disconnect the smart card reader cable assembly from the motherboard connector J3904.

4. Remove the smart card reader cable assembly from the system.

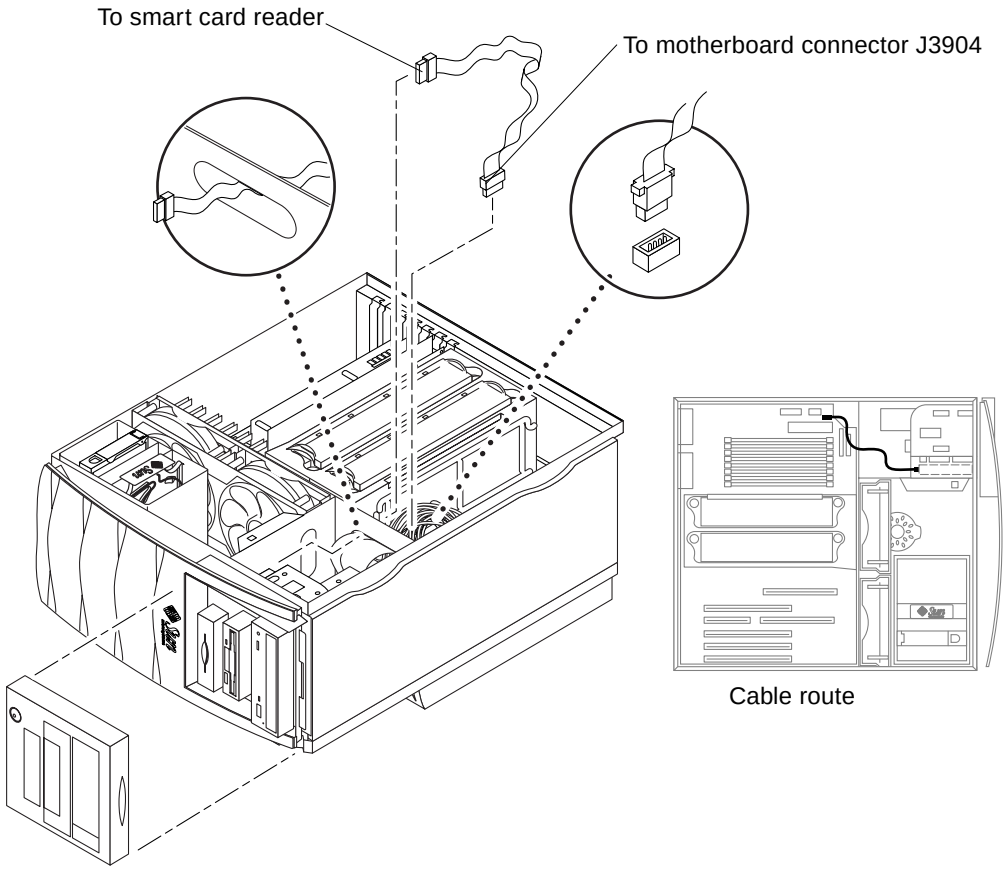

FIGURE 6-9 Removing and Replacing the Smart Card Reader Cable Assembly

6.3.8 Replacing the Smart Card Reader Cable Assembly

1. **Position the smart card reader cable assembly in the chassis (**FIGURE 6-9**).**
2. **Connect the smart card reader cable assembly to the smart card reader.**
3. **Connect the smart card reader cable assembly to the motherboard connector J3904.**
4. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

6.3.9 Removing the Combined Cable Assembly

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Remove any PCI cards necessary to gain access to the combined cable assembly.**

   See Section 8.2.1 “Removing a PCI Card” on page 8-5.

3. **Remove the CPU shroud cover.**

4. **Remove the fan bracket.**

   See Section 6.6.1 “Removing the Fan Bracket” on page 6-24.

5. **Disconnect the combined cable assembly as follows (**FIGURE 6-10**):**

   a. **Remove the combined cable assembly connectors from the interlock switch terminators.**

   b. **Remove the combined cable assembly connectors from the power switch terminators.**

   c. **Remove the combined cable assembly connectors from the speaker assembly terminators.**

   d. **Remove the combined cable assembly connector from J3602 on the motherboard.**

6. **Remove the LED from the chassis and lift the combined cable assembly up and out from chassis.**

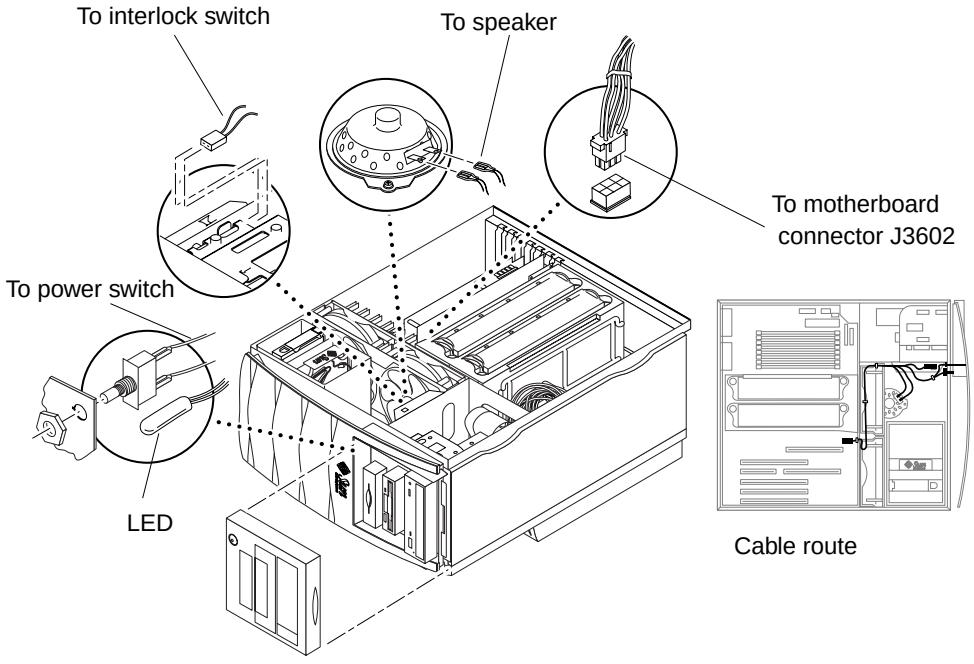

FIGURE 6-10 Removing and Replacing the Combined Cable Assembly

6.3.10 Replacing the Combined Cable Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position the combined cable assembly in the chassis (**FIGURE 6-10**).**
2. **Connect the combined cable assembly as follows:**
   a. **Attach the combined cable assembly connectors to the interlock switch terminators.**
   b. **Attach the combined cable assembly connectors to the power switch terminators.**
   c. **Replace the LED in the front panel LED holder.**

d. Replace the combined cable assembly connectors to the speaker assembly terminators.

e. Connect the combined cable assembly connector to motherboard connector J3602.

3. Replace the fan bracket.

See Section 6.6.2 “Replacing the Fan Bracket” on page 6-25.

4. Replace the CPU shroud cover.

See Section 8.8.2 “Replacing the CPU Shroud Assembly” on page 8-29.

5. Detach the antistatic wrist strap, replace the access panel, and power on the system.

See Chapter 9 “Finishing Replacement Procedures.”

6.3.11 Removing the Logo LED Cable Assembly

1. Power off the system, remove the access panel, and attach the antistatic wrist strap.

See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the CPU shroud cover.

See Section 8.8.1 “Removing the CPU Shroud Assembly” on page 8-28.

3. Remove the fan bracket.

See Section 6.6.1 “Removing the Fan Bracket” on page 6-24.

4. Disconnect the logo LED cable assembly as follows (FIGURE 6-11**):**

a. Remove the logo LEDs from the front panel.

b. Remove the logo LED cable assembly connector from J3605 on the motherboard.

5. Remove the logo LED cable assembly from the chassis.

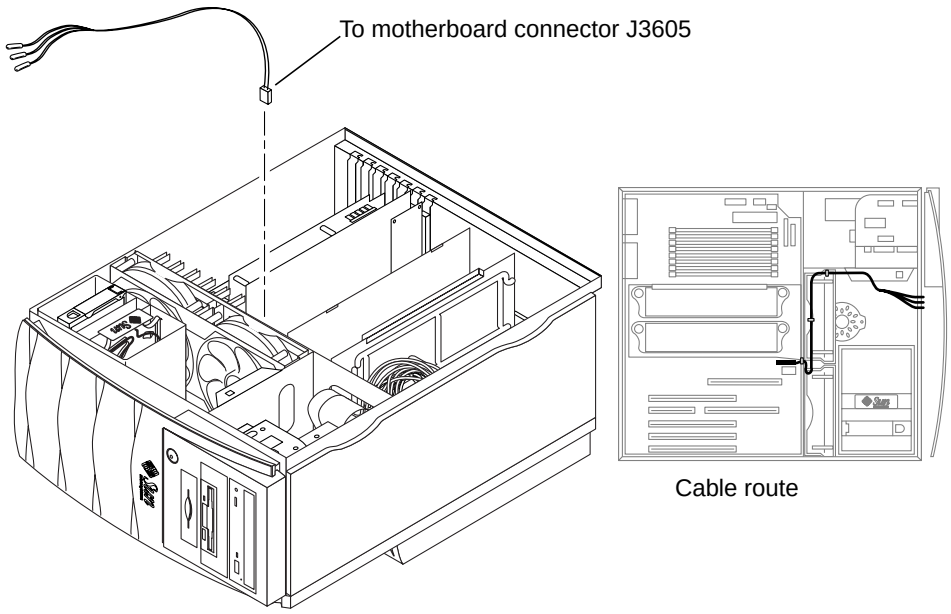

FIGURE 6-11 Removing and Replacing the Logo LED Cable Assembly

6.3.12 Replacing the Logo LED Cable Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position the logo LED cable assembly in the chassis (**FIGURE 6-11**).**
2. **Connect the logo LED cable assembly as follows:**
   a. **Replace the LEDs in the front panel LED holders.**
   b. **Connect the logo LED cable assembly connector to motherboard connector J3605.**
3. **Replace the fan bracket.**

   See Section 6.6.2 “Replacing the Fan Bracket” on page 6-25.
4. **Replace the CPU shroud cover.**

   See Section 8.8.2 “Replacing the CPU Shroud Assembly” on page 8-29.

5. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

6.4 Interlock Switch Assembly

Use the following procedures to remove and replace the interlock switch assembly.

6.4.1 Removing the Interlock Switch Assembly

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Press the detent tabs at either side of the interlock switch assembly while pulling the switch from the chassis switch housing (**FIGURE 6-12**).**
3. **Continue to press the detent tabs and pull the interlock switch assembly until the interlock switch assembly is free from the housing.**
4. **Remove the combined cable assembly connectors from the interlock switch terminators.**
5. **Remove the interlock switch assembly.**

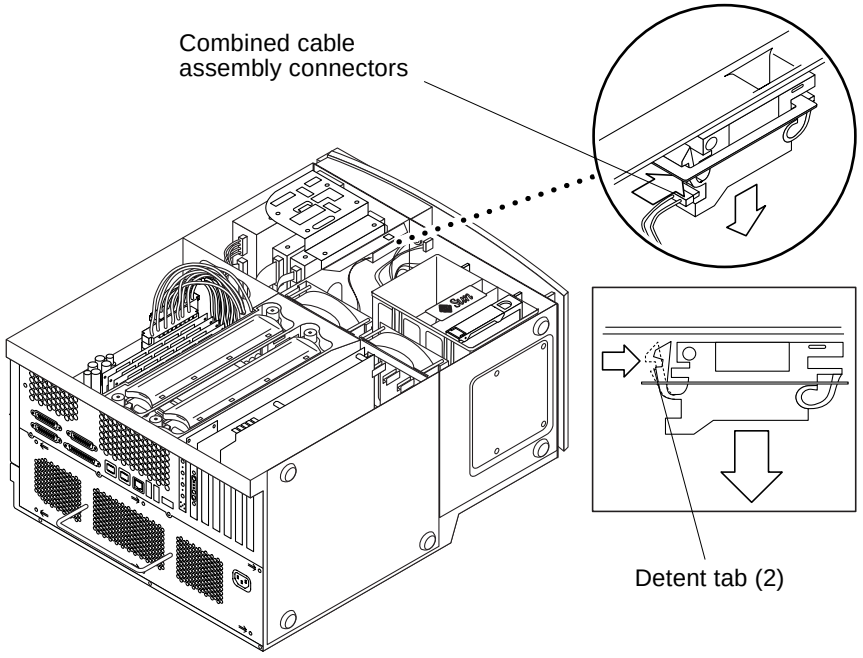

FIGURE 6-12 Removing and Replacing the Interlock Switch Assembly

6.4.2 Replacing the Interlock Switch Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Connect the combined cable assembly connectors to the interlock switch terminators (**FIGURE 6-12**).**
2. **Press the detent tabs at either side of the interlock switch assembly while positioning the switch into the chassis.**
3. **Continue to press the detent tabs and pull the interlock switch assembly until the switch is properly seated.**

4. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

6.5 System Fan Assemblies

Use the following procedures to remove and replace the upper or lower system fan assemblies.

6.5.1 Removing a Fan Assembly

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Disconnect the fan assembly power connectors from the motherboard connector J3302 for the lower fan assembly or J3303 for the upper fan assembly (**FIGURE 6-13**).**

Note – Use a small screwdriver to release the connector tabs.

3. **Release the three fan bracket tabs in the chassis.**

   See FIGURE 6-13.

4. **Lift the fan bracket and fans from the chassis.**

5. **Remove the fan assembly from the bracket.**

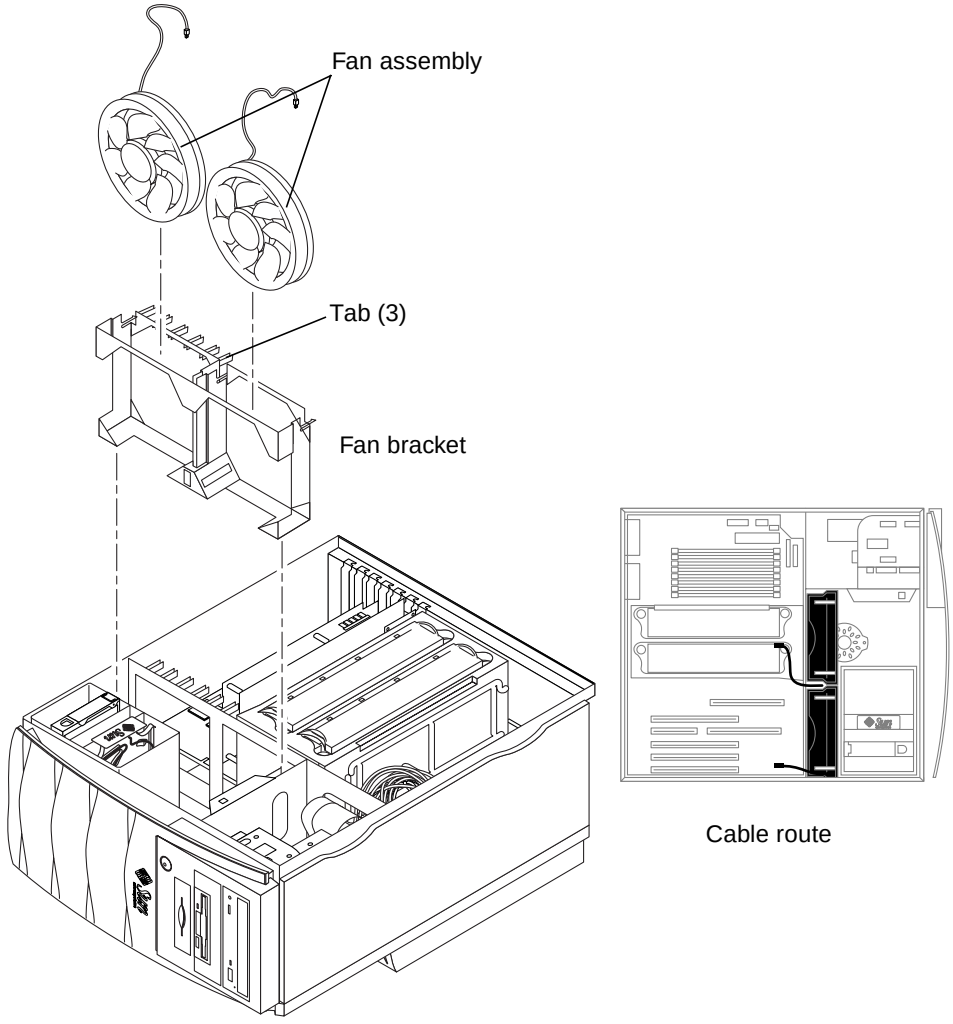

FIGURE 6-13 Removing and Replacing a Fan Assembly

6.5.2 Replacing a Fan Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Press the fan assembly into the fan bracket (**FIGURE 6-13**).**
2. **Feed the fan cable through the sheet metal cutout in the chassis.**
3. **Position the fan bracket into the chassis by aligning the four lower tabs and three upper side tabs.**
4. **Gently push the fan bracket down and towards the chassis frame until the fan bracket side tabs latch.**
5. **Connect the fan assembly power connectors to the motherboard connector J3302 for the lower fan assembly or J3303 for the upper fan assembly.**
6. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

6.6 Fan Bracket

Use the following procedures to remove and replace the fan bracket.

6.6.1 Removing the Fan Bracket

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Disconnect the fan assemblies from the motherboard (**FIGURE 6-14**).**

   See Section 6.5.1 “Removing a Fan Assembly” on page 6-22.
3. **Release the three fan bracket tabs in the chassis.**

   See FIGURE 6-14.
4. **Lift the fan bracket and fans from the chassis.**
5. **Remove the fan assemblies from the bracket.**

   See Section 6.5.1 “Removing a Fan Assembly” on page 6-22.

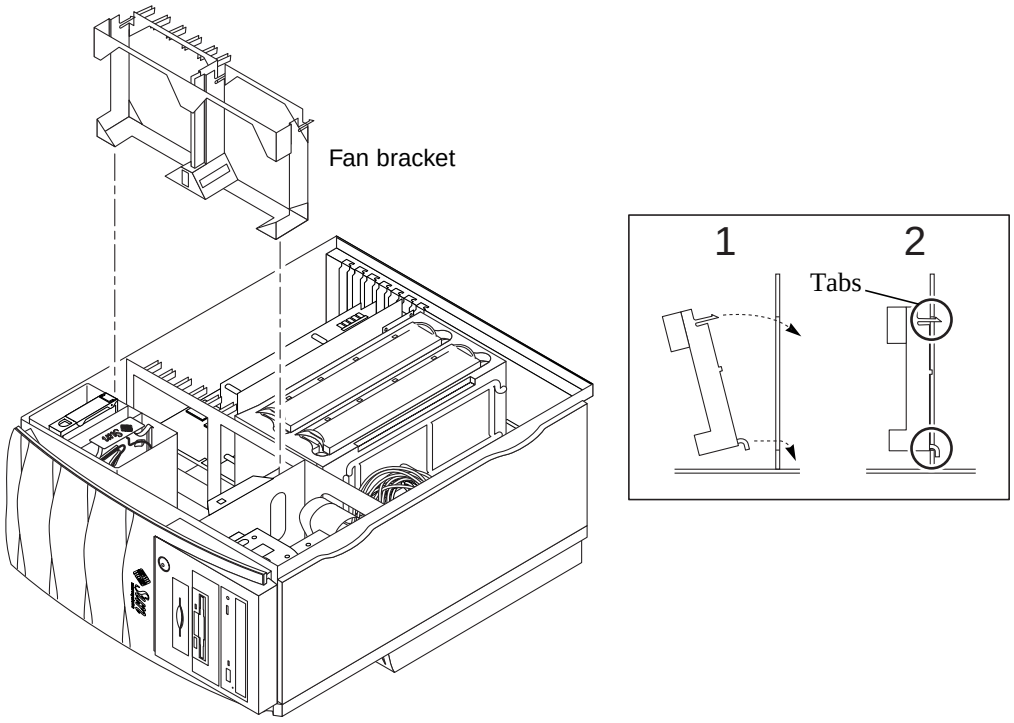

FIGURE 6-14 Removing and Replacing the Fan Bracket

6.6.2 Replacing the Fan Bracket

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Replace the fan assemblies (**FIGURE 6-14**).**

   See Section 6.5.2 “Replacing a Fan Assembly” on page 6-23.

2. **Position the fan bracket and fans into the chassis by aligning the four lower tabs and three upper side tabs.**

3. **Gently push the fan bracket down and toward the chassis frame until the fan bracket side tabs latch.**

4. **Reconnect the fan power connectors.**

   See Section 6.5.2 “Replacing a Fan Assembly” on page 6-23.

5. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

6.7 Speaker Assembly

Use the following procedures to remove and replace the speaker assembly.

6.7.1 Removing the Speaker Assembly

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Using a No. 2 Phillips screwdriver, remove the screw securing the speaker assembly to the chassis (**FIGURE 6-15**).**
3. **Disconnect the combined cable assembly connectors from the speaker assembly terminators.**
4. **Remove the speaker assembly.**

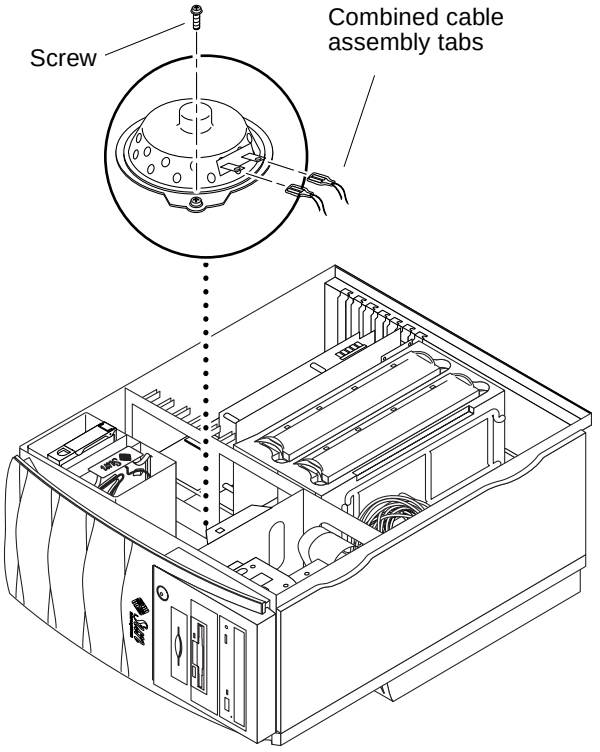

FIGURE 6-15 Removing and Replacing the Speaker Assembly

6.7.2 Replacing the Speaker Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Connect the combined cable assembly connectors to the speaker assembly terminators (**FIGURE 6-15**).**
2. **Place the speaker tab into the chassis slot.**
3. **Using a No. 2 Phillips screwdriver, replace the screw securing the speaker assembly to the chassis.**

4. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

6.8 FC-AL Backplane Assembly

The FC-AL backplane assembly consists of the FC-AL backplane, FC-AL cable assembly, and hard drive bracket. The FC-AL backplane assembly is attached to the chassis. Use the following procedures to remove and replace the FC-AL backplane assembly.

6.8.1 Removing the FC-AL Backplane Assembly

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Remove the fan bracket.**

   See Section 6.6.1 “Removing the Fan Bracket” on page 6-24.

3. **Remove the hard drive(s).**

   See Section 7.1.1 “Removing a Hard Drive” on page 7-2.

4. **Remove the torque tool from the slot in the FC-AL backplane assembly.**

5. **Disconnect the power connector from the FC-AL backplane assembly.**

6. **Disconnect the FC-AL cable assembly from the FC-AL backplane assembly.**

7. **Using a No. 2 Phillips screwdriver, proceed as follows (**FIGURE 6-16**):**

   a. **Loosen the two captive screws (located on the left side of the FC-AL backplane assembly).**

   b. **Remove the two screws from the chassis bottom that secure the FC-AL backplane assembly to the chassis.**

8. **Disconnect the FC-AL backplane assembly from the chassis cutouts and lift it from the chassis.**

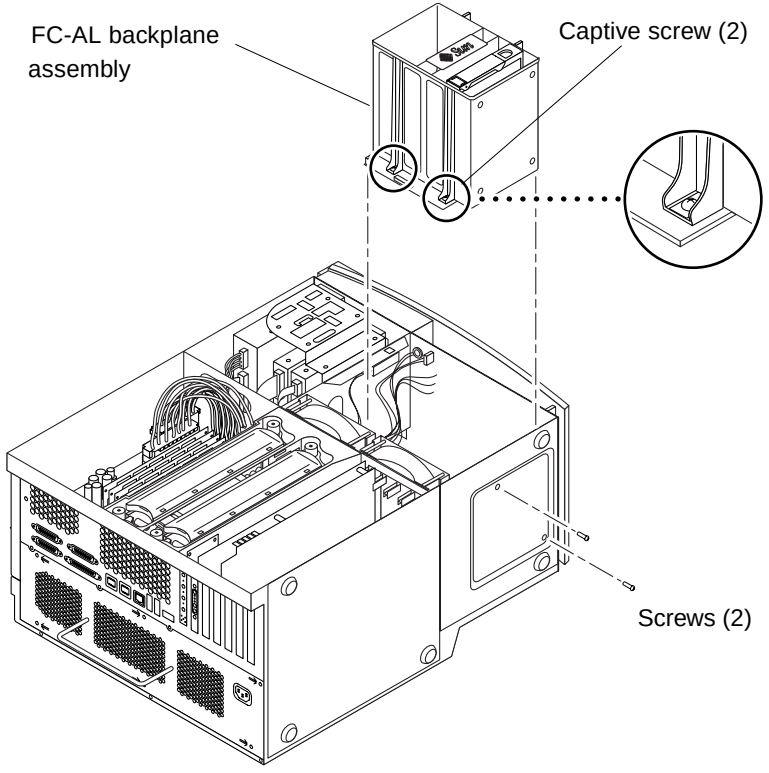

FIGURE 6-16 Removing and Replacing the FC-AL Backplane Assembly

6.8.2 Replacing the FC-AL Backplane Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position the FC-AL backplane assembly in the chassis and connect it to the chassis cutouts (**FIGURE 6-16**).**
2. **Using a No. 2 Phillips screwdriver, proceed as follows:**

a. **Replace the two screws into the chassis bottom that secure the FC-AL backplane assembly to the chassis.**

b. **Tighten the two captive screws (located on the left side of the FC-AL backplane assembly).**

3. **Connect the FC-AL backplane cable assembly to the FC-AL backplane.**
4. **Connect the power connector to the FC-AL backplane assembly.**
5. **Replace the hard drive(s).**

   See Section 7.1.2 “Replacing a Hard Drive” on page 7-3.
6. **Return the torque tool to the slot in the backplane assembly.**
7. **Replace the fan bracket.**

   See Section 6.6.2 “Replacing the Fan Bracket” on page 6-25.
8. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

6.9 Chassis Foot

Use the following procedures to remove and replace a chassis foot.

6.9.1 Removing a Chassis Foot

- **Use a flat-tipped tool to pry the foot from the chassis (**FIGURE 6-17**).**

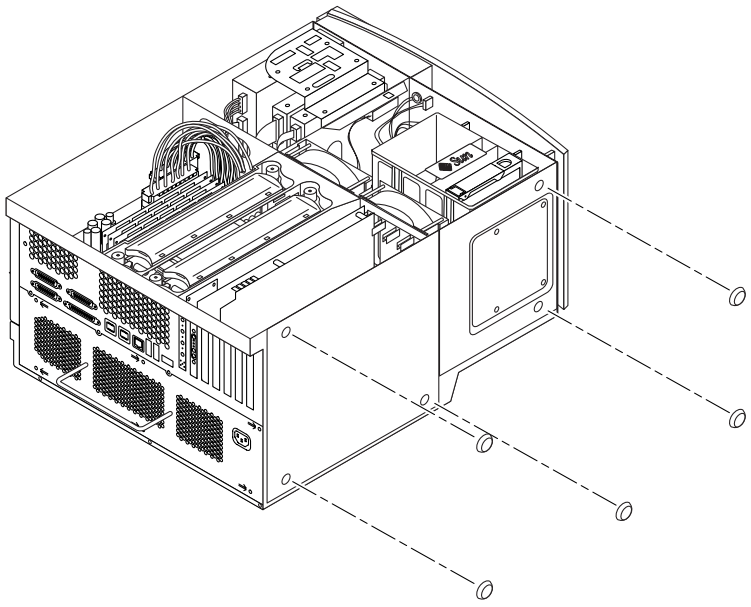

FIGURE 6-17 Removing and Replacing the Chassis Foot

6.9.2 Replacing a Chassis Foot

1. **Using a cloth rag and cleanser, clean the chassis area where the foot is to be mounted (**FIGURE 6-17**).**
2. **Peel the protective cover from the adhesive side of the foot and place the foot on the chassis.**

6.10 Filler Panels

Use the following procedures to remove and replace a filler panel.

6.10.1 Removing a Filler Panel

1. **Identify the filler panel to be removed.**
2. **Remove the peripheral bezel assembly (**FIGURE 6-18**).**
3. **Remove the plastic filler panel from the peripheral bezel assembly.**
4. **Remove the metal filler panel from the peripheral assembly (**FIGURE 6-19**).**

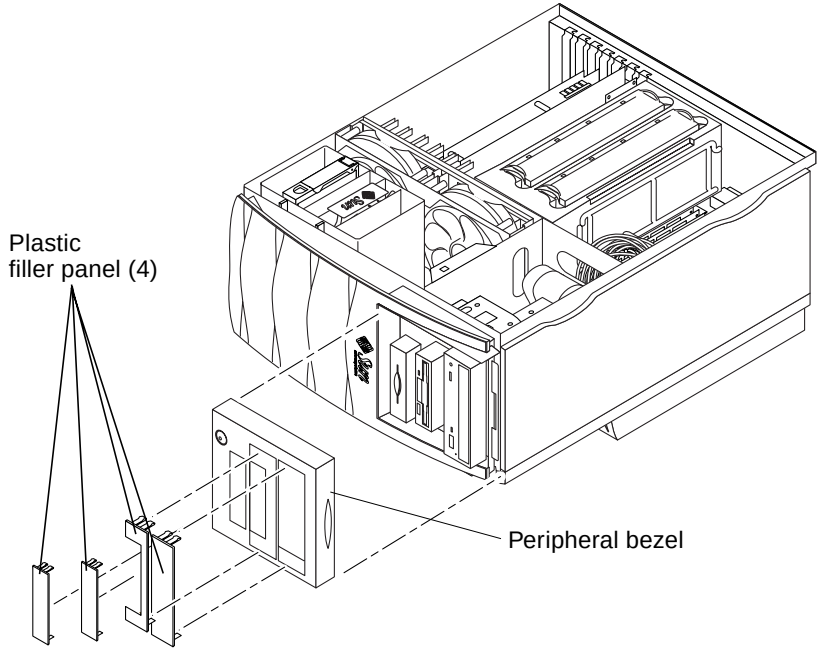

FIGURE 6-18 Removing and Replacing Plastic Filler Panels

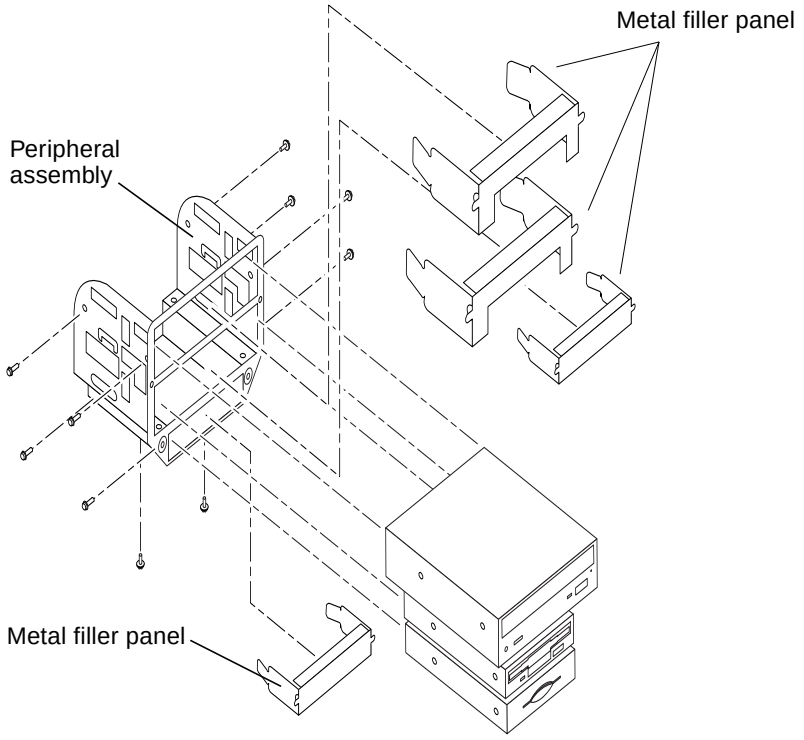

FIGURE 6-19 Removing and Replacing Metal Filler Panels

6.10.2 Replacing a Filler Panel

1. **Position and snap the metal filler panel into the peripheral assembly (**FIGURE 6-19**).**
2. **Position and snap the plastic filler panel into the peripheral bezel assembly (**FIGURE 6-18**).**

CHAPTER 7

Removing and Replacing Storage Devices

This chapter describes how to remove and replace the Sun Blade 1000 storage devices.

The chapter contains the following topics:

7.1 Hard Drive

Perform the following procedures to remove and replace a hard drive. If necessary, view the ShowMe How video clip located on the Sun Blade 1000 Hardware Documentation CD-ROM.

Note – When removing or replacing a hard drive, drive slot 1 is in the bottom position of the hard drive bracket. Drive slot 2 is in the upper position of the hard drive bracket.

Note – If only one hard drive is installed on the system or if you only want to boot from a specific drive, that hard drive must be installed in drive slot 1 in the bottom position of the hard drive bracket.

7.1.1 Removing a Hard Drive

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Release the drive handle by pushing the handle release button toward the front of the chassis housing (**FIGURE 7-1**).**
3. **Pull out on the drive handle to disconnect the hard drive from the FC-AL backplane assembly connector.**
4. **Remove the hard drive from the hard drive bracket.**
5. **Place the hard drive on an antistatic mat.**

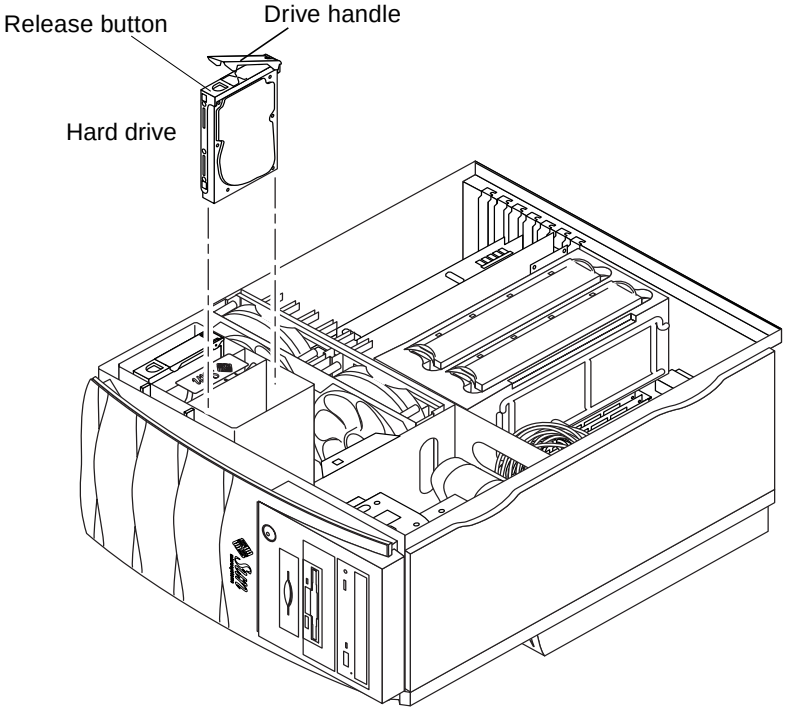

FIGURE 7-1 Removing and Replacing a Hard Drive

7.1.2 Replacing a Hard Drive

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Holding the drive handle, insert the hard drive into the hard drive bracket along the vertical plastic guides until the hard drive handle starts to close (**FIGURE 7-1**).**
2. **Close the hard drive handle to lock the hard drive into the hard drive bracket.**
3. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

7.2 Peripheral Assembly Drive

To remove and replace a peripheral assembly drive, it is necessary to remove the peripheral assembly. If necessary, view the ShowMe How video clip located on the Sun Blade 1000 CD-ROM.

Note – The peripheral assembly drive can include a DVD-ROM drive, a 4-mm tape drive, or other offered optional drive components.

Note – If no drives are installed in the peripheral assembly, only the SCSI cable should be routed into the upper drive bay. Attach the SCSI cable through the clip affixed on the rear wall of the peripheral assembly.

7.2.1 Removing the Peripheral Assembly

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Remove the peripheral bezel assembly by pressing down on the top of the bezel and pulling it straight out from the chassis (**FIGURE 7-2**).**
3. **Using a No. 2 Phillips screwdriver, remove the four screws securing the peripheral assembly to the chassis.**
4. **Partially remove the peripheral assembly from the chassis.**
5. **Disconnect the power and interface cables from all drives installed in the peripheral assembly.**
6. **Remove the peripheral assembly from the chassis.**
7. **Place the peripheral assembly on an antistatic mat.**

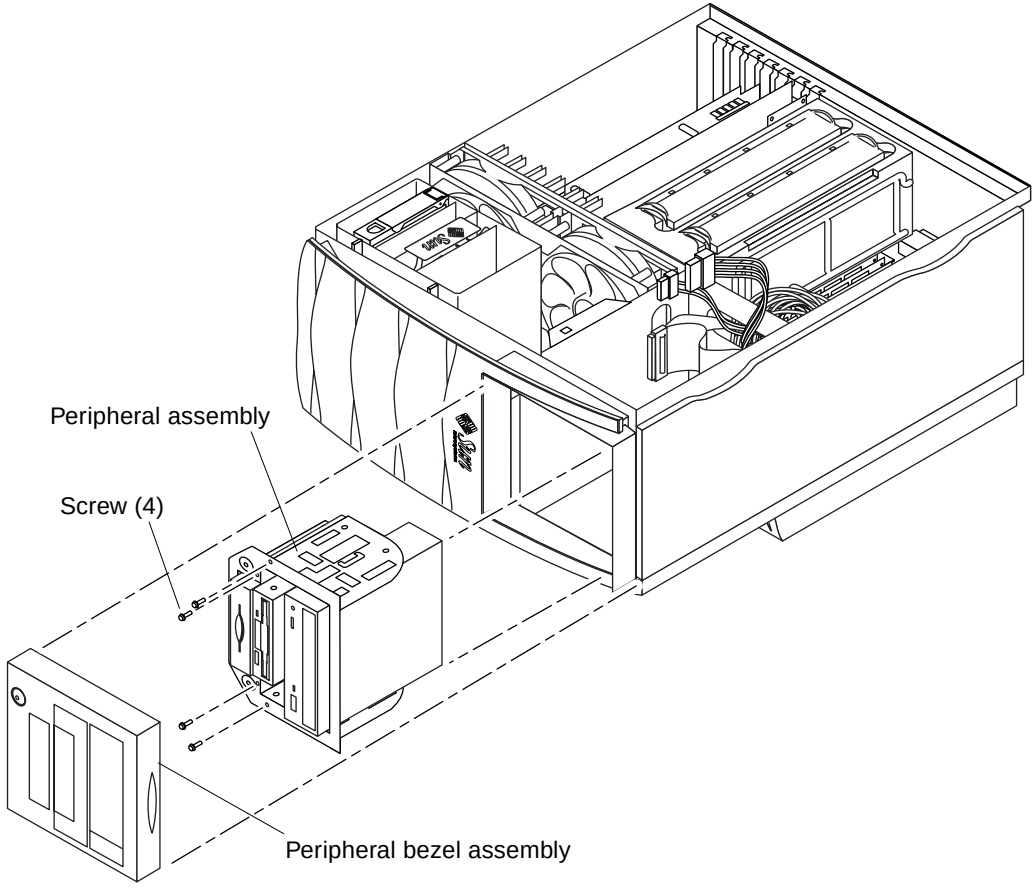

FIGURE 7-2 Removing and Replacing the Peripheral Assembly

7.2.2 Removing the DVD-ROM Drive, or Any Optional Tape Drive Component

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position the peripheral assembly on a flat surface so that the DVD-ROM drive, or tape drive is flat (**FIGURE 7-3**).**

2. **Using a No. 2 Phillips screwdriver, remove the four screws securing the DVD-ROM drive, or tape drive to the peripheral assembly.**

Note – The four screws that secure a drive to the peripheral drive assembly are specifically sized screws. Do not intermingle them with other screws.

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3. **Remove the DVD-ROM drive, or tape drive and place it on an antistatic mat.**

4. **Install the filler panel if necessary.**

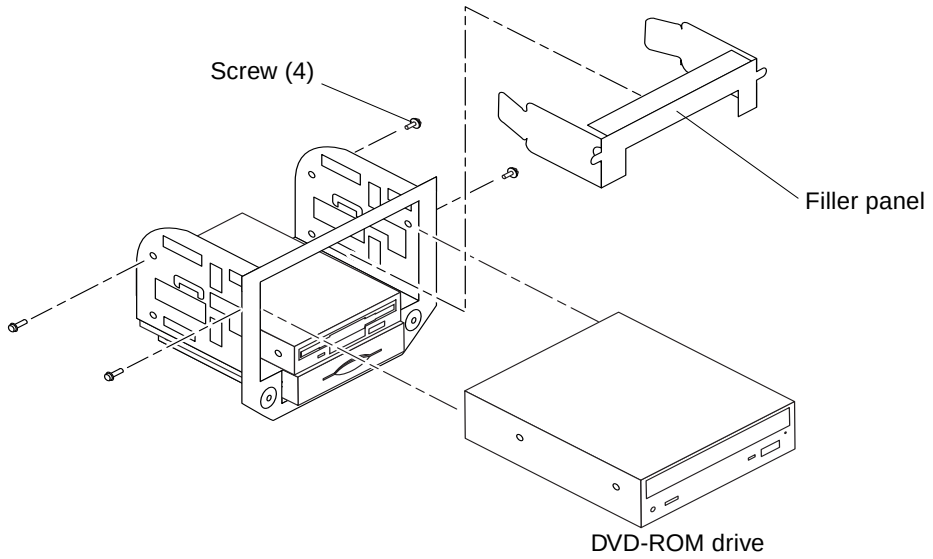

FIGURE 7-3 Removing and Replacing the DVD-ROM Drive

7.2.3 Replacing the DVD-ROM Drive, or Any Optional Tape Drive Component

Note – If you are installing a DVD-ROM drive or any optional tape drive component (instead of replacing it), ensure that the peripheral power cable and all data cables are properly routed through the clips adjacent to the peripheral assembly. Route the SCSI cable through the clip affixed on the rear wall of the peripheral assembly.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Remove the filler panel if necessary (**FIGURE 7-3 **on page 7-6).**
2. **Position the DVD-ROM drive or tape drive into the peripheral assembly.**
3. **Using a No. 2 Phillips screwdriver, replace the four screws securing the DVD-ROM drive or tape drive to the peripheral assembly.**
4. **Replace the peripheral assembly.**

   See Section 7.2.8 “Replacing the Peripheral Assembly” on page 7-11.

7.2.4 Removing the Smart Card Reader (future support)

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Note – Though SmartCard readers are physically configured in Sun Blade workstations at product introduction, the driver support necessary to make the readers functional is not available in this Solaris software release. The reader driver support will be made available in a future Solaris software release.

1. **Position the peripheral assembly on a flat surface so that the smart card reader is flat (**FIGURE 7-4**).**
2. **Using a No. 2 Phillips screwdriver, remove the four screws securing the smart card reader to the peripheral assembly.**

3. **Remove the smart card reader and place it on an antistatic mat.**

Note – The four screws that secure a drive to the peripheral drive assembly are specifically sized screws. Do not intermingle them with other screws.

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4. **Install the filler panel, if necessary.**

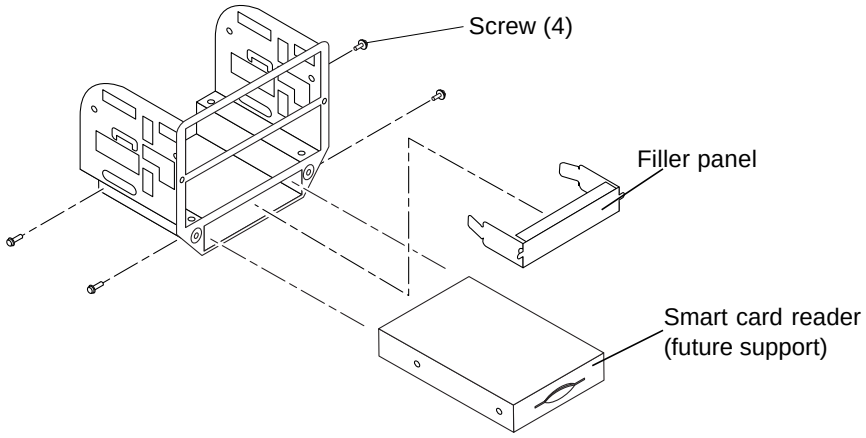

FIGURE 7-4 Removing and Replacing the Smart card reader (future support)

7.2.5 Replacing the Smart Card Reader (future support)

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Note – Though SmartCard readers are physically configured in Sun Blade workstations at product introduction, the driver support necessary to make the readers functional is not available in this Solaris software release. The reader driver support will be made available in a future Solaris software release.

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1. **Remove the filler panel if necessary (**FIGURE 7-3 **on page 7-6).**
2. **Replace the diskette drive if it has been removed.**

   See Section 7.2.7 “Replacing the Diskette Drive” on page 7-10.

3. **Position the smart card reader into the peripheral assembly.**
4. **Using a No. 2 Phillips screwdriver, replace the four screws securing the smart card reader to the peripheral assembly.**
5. **Replace the peripheral assembly.**

See Section 7.2.8 “Replacing the Peripheral Assembly” on page 7-11.

7.2.6 Removing the Diskette Drive

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position the peripheral assembly on a flat surface so that the diskette drive is flat (**FIGURE 7-5**).**
2. **Remove the smart card reader.**

See Section 7.2.4 “Removing the Smart Card Reader (future support)” on page 7-7.

3. **Using a No. 2 Phillips screwdriver, remove the four screws securing the diskette drive to the peripheral assembly.**

Note – The four screws that secure a drive to the peripheral drive assembly are specifically sized screws. Do not intermingle them with other screws.

4. **Remove the diskette drive and place it on an antistatic mat.**
5. **Install the filler panel if necessary.**

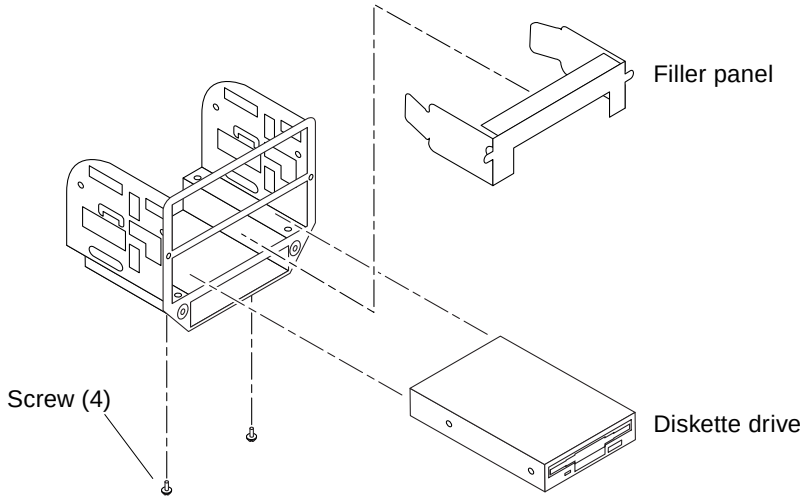

FIGURE 7-5 Removing and Replacing the Diskette Drive

7.2.7 Replacing the Diskette Drive

Note – If you are installing a diskette drive (instead of replacing it), ensure that the peripheral power cable and all data cables are properly routed through the clips adjacent to the drive bay.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

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1. **Remove the filler panel if necessary (**FIGURE 7-3 **on page 7-6).**
2. **Remove the smart card reader if it has been installed.**

   See Section 7.2.4 “Removing the Smart Card Reader (future support)” on page 7-7.
3. **Position the diskette drive in the peripheral assembly.**
4. **Using a No. 2 Phillips screwdriver, replace the four screws securing the diskette drive to the peripheral assembly.**
5. **Replace the smart card reader.**

   See Section 7.2.5 “Replacing the Smart Card Reader (future support)” on page 7-8.

6. **Replace the peripheral assembly.**

   See Section 7.2.8 “Replacing the Peripheral Assembly”.

7.2.8 Replacing the Peripheral Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position the peripheral assembly in the chassis (**FIGURE 7-2 **on page 7-5).**

   Note – Ensure that the peripheral assembly is correctly seated in the rails of the chassis.

2. **Connect the rear cable connectors to the drives as required.**
3. **Using a No. 2 Phillips screwdriver, tighten the four screws securing the peripheral assembly to the chassis.**
4. **Replace the peripheral bezel assembly.**
5. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

CHAPTER 8

Removing and Replacing the Motherboard and Associated Components

This chapter describes how to remove and replace the system motherboard and associated components.

This chapter covers the following topics:

8.1 CPU Module

The Sun Blade 1000 system contains one or two CPU modules. An unused CPU slot will be filled with a CPU shroud filler panel. Perform the following procedures to remove and replace a CPU module. If necessary, view the ShowMe How video clip located on the Sun Blade 1000 Hardware Documentation CD-ROM.

8.1.1 Removing a CPU Module

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Lay the system on its side.**
3. Squeeze the two tabs on the CPU shroud cover and lift the cover up to **remove (**FIGURE 8-7**).**
4. **Use the torque tool to loosen the captive screws.**
5. **Lift the CPU module out of the CPU shroud.**
6. **Place the CPU module on an antistatic mat with the heat sink on the top, facing up.**

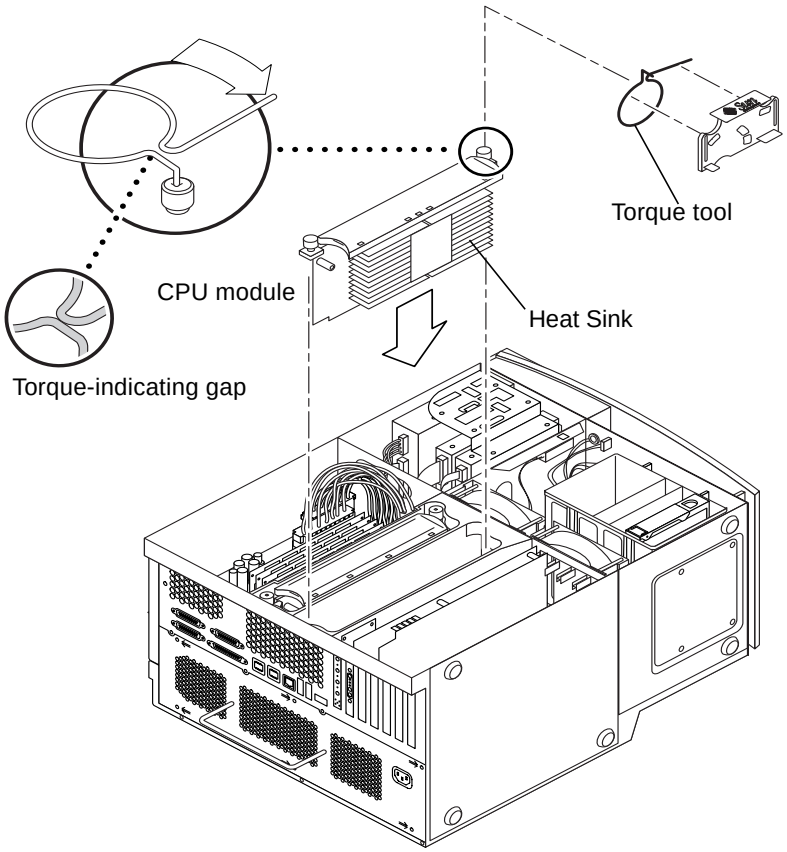


FIGURE 8-1 Removing and Replacing a CPU Module

8.1.2 Replacing a CPU Module

Note – The system can use either one or two CPU modules. If one module is used it should be placed in the slot closest to the top of the system.

Caution – To ensure proper system cooling, any unused CPU slot must contain a CPU shroud filler panel in place of a CPU module.

Caution – When you unpack a new CPU module from its packing carton, it is important that you observe the following handling precautions to avoid damaging the module. 1.) When you lift the module from the packing carton in its antistatic bag, use both hands to support the module along its short sides. 2.) After you remove the module from its antistatic bag, handle it only by its captive screws. Do not touch the connectors on the bottom edge of the module, which can be easily bent or damaged by improper handling. 3.) Do not remove the plastic cover from the connectors until you are ready to install the module. 4.) Do not grip the module by the heat sinks, which can shift if handled improperly. 5.) Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Lower the CPU module into the CPU shroud until the module's captive screws are aligned with the screw holes in the CPU shroud (**FIGURE 8-1**).**

2. **Tighten the captive screws.**

   Use the torque indicator tool to tighten the screws to the correct torque. As seen in FIGURE 8-1, the correct torque setting is indicated when the gap in the torque indicator tool is closed.

Caution – Do not use a torque indicator tool from another Sun product. The tool is designed for this system specifically.

Note – If you are using an adjustable torque tool, tighten the CPU module captive screws to 5 inch-pounds.

Caution – Under torquing the CPU module captive screws may cause a loss of continuity and failure of the system to boot. Over torquing the CPU module captive screws will cause severe damage and system failure.

3. **Reinstall the shroud cover.**

4. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 "Finishing Replacement Procedures."

5. **Verify proper operation.**

   See Section 3.4 "Maximum and Minimum Levels of POST" on page 3-5.

8.2 PCI Card

Perform the following procedures to remove and replace a PCI card. If necessary, view the ShowMe How video clip located on the Sun Blade 1000 Hardware Documentation CD-ROM.

8.2.1 Removing a PCI Card

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

2. **Lay the system on its side.**

3. **Disconnect any external cables from the PCI card that you plan to remove.**

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Note – To remove extra-long PCI cards, detach the fan bracket tabs and pull the bracket back out of the way.

4. **Using a No. 2 Phillips screwdriver, remove the screw securing the PCI card bracket tab to the system chassis (**FIGURE 8-2**).**

Caution – Avoid damaging the connector by not applying force to one end or one side of the board.

5. **Pull the upper two corners of the card straight up from the connector.**

6. **Remove the PCI card.**

7. **Place the PCI card on an antistatic mat.**

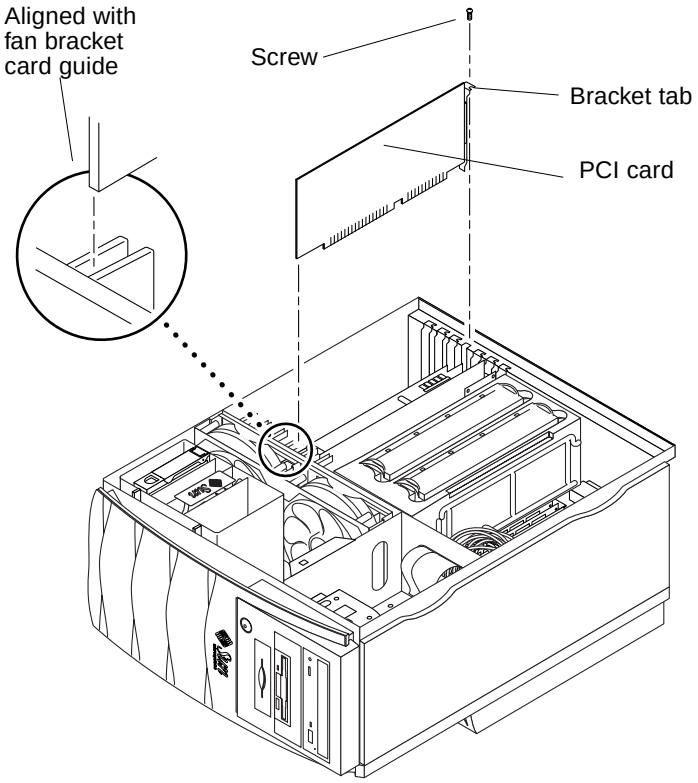


FIGURE 8-2 Removing and Replacing a PCI Card

8.2.2 Replacing a PCI Card

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Note – Read the PCI card product guide for information about jumper or switch settings, connector requirements, and required tools.

Note – To insert extra-long PCI cards, detach the fan bracket tabs and pull the bracket back out of the way.

1. **Position the PCI card in the chassis (**FIGURE 8-2**).**
2. **Guide the card bracket tab into the chassis back-panel opening. Guide the opposite end of the card into the fan bracket card guide so that the card is aligned evenly with the motherboard connector.**
3. **At the two upper corners of the PCI card, push the PCI card straight down into the connector until the PCI card is fully seated.**
4. **Using a No. 2 Phillips screwdriver, replace the screw securing the PCI card bracket tab to the system chassis.**

   Note – If you have removed the fan bracket for extra long PCI cards, replace it by latching it into the slots in the chassis.

5. **If necessary, reattach the fan bracket removed earlier.**
6. **Connect any cables to the PCI boards.**
7. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”
8. **Verify proper operation.**

   See Section 3.4 “Maximum and Minimum Levels of POST” on page 3-5.

8.3 Graphics Card

Perform the following procedure to remove and replace a graphics card. If necessar, view the ShowMe How video clip located on the Sun Blade 1000 Hardware Documentation CD-ROM.

Note – The Expert 3D graphics card can not be used in a 66 MHz PCI slot.

8.3.1 Removing the Graphics Card

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

2. **Lay the system on its side.**

3. **Disconnect the video cable from the graphics card video connector.**

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

4. **Using a No. 2 Phillips screwdriver, remove the screw securing the graphics card bracket tab to the system chassis (**FIGURE 8-3**).**

Caution – Avoid applying force to one end or one side of the board, or connector damage may occur.

5. **At the two upper corners of the graphics card, pull the card straight up from the connector.**

6. **Remove the graphics card.**

7. **Place the graphics card on an antistatic mat.**

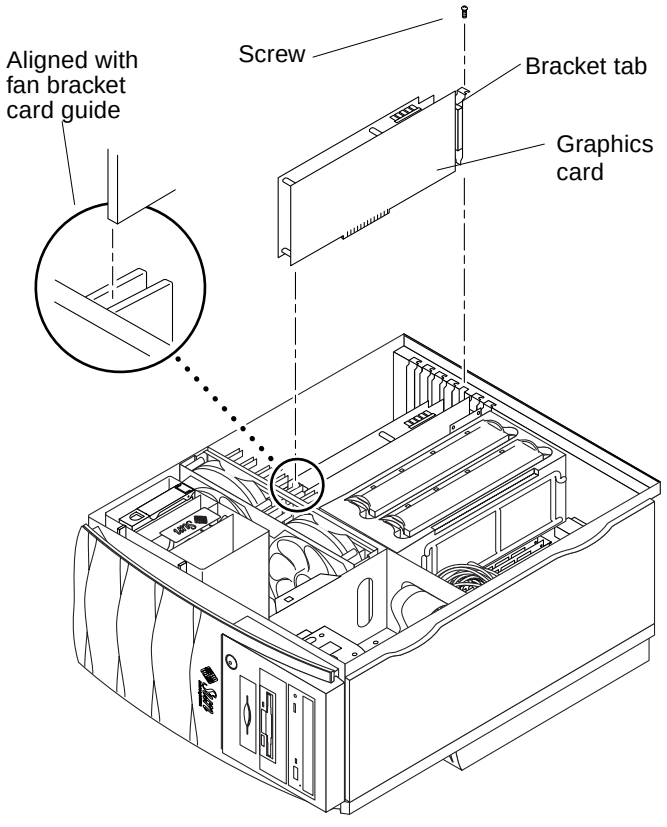


FIGURE 8-3 Removing and Replacing a Graphics Card

8.3.2 Replacing the Graphics Card

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position the graphics card in the chassis (**FIGURE 8-3**).**
2. **Guide the card bracket tab into the chassis back-panel slot opening. Guide the opposite end of the card into the fan bracket card guide so that the card is aligned evenly with the motherboard connector.**

Caution – Avoid applying excessive force to one end or one side of the card, or connector damage may occur.

3. **At the two upper corners of the card, push the card straight down into the connector until the card is fully seated.**

Note – The graphics card connector is a double-row connector that requires two levels of insertion. When installing the graphics card, ensure that the card is fully seated into the connector.

4. **Using a No. 2 Phillips screwdriver, replace the screw securing the bracket tab to the system chassis.**
5. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”
6. **Connect the video cable to the graphics card video connector.**

8.4 Audio Module Assembly

Perform the following procedures to remove and replace the audio module assembly. If necessary, view the ShowMe How video clip located on the Sun Blade 1000 CD-ROM.

8.4.1 Removing the Audio Module Assembly

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

2. **Lay the system on its side.**

3. **Disconnect any external audio cables from the audio module assembly.**

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

4. **Using a No. 2 Phillips screwdriver, remove the screw securing the audio module assembly bracket tab to the system chassis (**FIGURE 8-4**).**

Caution – Avoid damaging the connector by not applying force to one end or one side of the module.

5. **At the two upper corners of the audio module assembly, pull the module straight up from the connector.**

6. **Remove the audio module assembly.**

7. **Place the audio module assembly on an antistatic mat.**

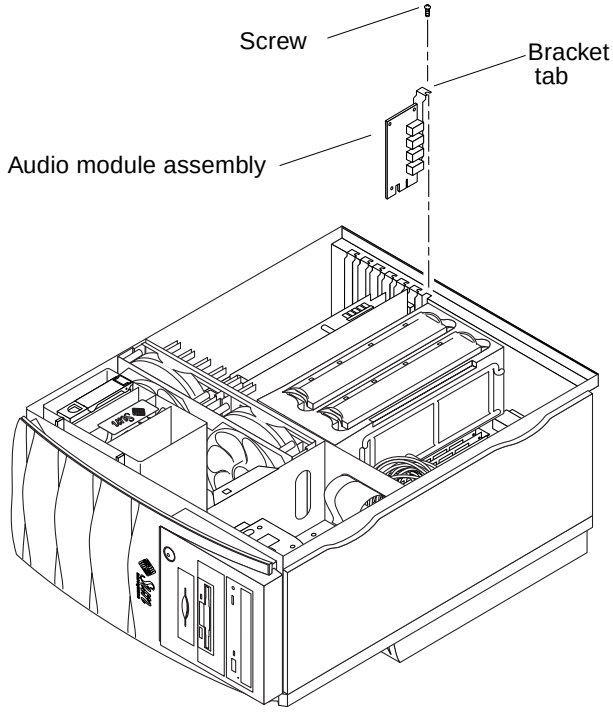


FIGURE 8-4 Removing and Replacing the Audio Module Assembly

8.4.2 Replacing the Audio Module Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position the audio module assembly into the chassis (**FIGURE 8-4**).**
2. **Lower the audio module assembly connector so that it touches its associated connector on the motherboard.**
3. **Align the audio module assembly bracket tab with the chassis back panel slot opening.**
4. **At the two upper corners of the module, push the module straight down into the connector until the module is fully seated.**

5. **Using a No. 2 Phillips screwdriver, replace the screw securing the audio module assembly to the system chassis.**
6. **Connect any external audio cables to the audio card.**
7. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

8.5 DIMM

Perform the following procedures to remove and replace a DIMM. If necessary, view the ShowMe How video clip located on the Sun Blade 1000 Hardware Documentation CD-ROM.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

Caution – When you remove and replace a single DIMM, an identical replacement is required. The replacement DIMM must be inserted into the same socket as the removed DIMM.

Caution – Each DIMM bank must contain at least four DIMMs of equal density (for example, four 128-Mbyte DIMMs) to function properly. Do not mix DIMM densities within any bank.

Caution – Handle DIMMs only by the edges. Do not touch the DIMM components or metal parts. Always wear a grounding strap when handling a DIMM.

8.5.1 Removing a DIMM

1. **Power off the system, remove the access panel and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Lay the system on its side.**
3. **Locate the DIMM(s) to be removed.**
4. **Press down the ejection lever at each end of the DIMM connector (**FIGURE 8-5**).**
5. **Lift the DIMM straight out of the connector and set it aside on the antistatic mat.**

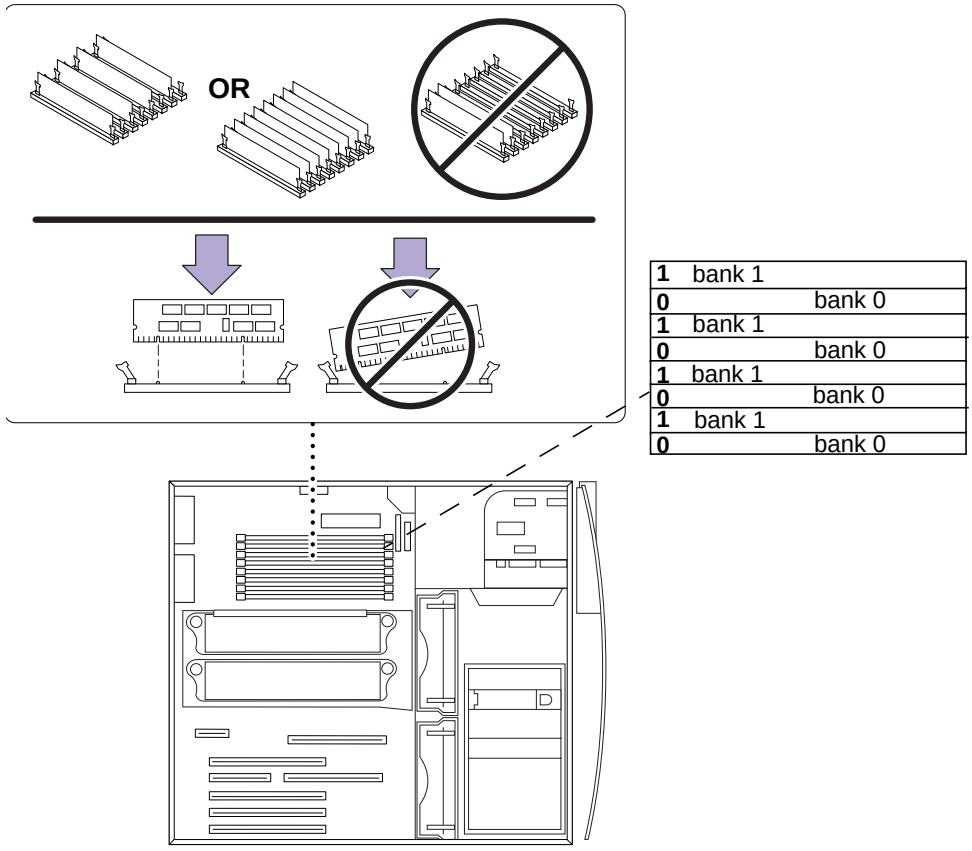


FIGURE 8-5 Removing and Replacing a DIMM

8.5.2 Replacing a DIMM

Caution – Do not remove any DIMM from the antistatic container until you are ready to install it on the motherboard. Handle DIMMs only by their edges. Do not touch DIMM components or metal parts.

Note – For optimum memory performance, consider interleaving issues when installing DIMMs.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface. Handle DIMMs only by the edges.

1. **Before installing a DIMM, review the following:**
   - DIMMs are arranged in two banks, 0 and 1. Each bank has four connectors labeled “0” or “1”.
   - The system must have four or eight DIMMs installed to operate.
   - Each DIMM bank must contain four DIMMs of equal size to function properly. For example four 128-Mbyte DIMMs in bank 0, four 256-Mbyte DIMMs in bank 1.
   - The default location for DIMMs installed at the factory is the four connectors labeled “0” (FIGURE 8-5).
2. **Remove the DIMM from the antistatic container.**
3. **Install the DIMM as follows (**FIGURE 8-5**):**
   a. **Align the notches on the DIMM with the memory connector.**
   b. **Using your thumbs, press the DIMM straight down into the connector until the ejection levers click, locking the DIMM in the connector.**

Note – The DIMM is seated when you hear a clicking sound and the DIMM ejection levers are in the vertical position.

4. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”
5. **Verify proper operation.**

   See Section 3.4 “Maximum and Minimum Levels of POST” on page 3-5.

8.6 Replaceable Battery

The system contains a replaceable lithium battery, part number 150-2850. Lithium batteries may explode if mishandled. Do not dispose of the battery in fire. Do not disassemble it or attempt to recharge it.

8.6.1 Removing the Battery

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Lay the system on its side.**
3. **Locate the battery on the motherboard.**

   See FIGURE C-14 on page C-36
4. **Remove the CPU shroud cover.**

   See Section 8.8.1 “Removing the CPU Shroud Assembly” on page 8-24.
5. **Remove the graphics card.**

   See Section 8.3.1 “Removing the Graphics Card” on page 8-9.
6. **Carefully lift the battery retaining clip with a small screwdriver.**
7. **Carefully slide the battery out of its socket and remove it from the system.**

8.6.2 Replacing the Battery

Note – Install the new battery with the plus (+) side up.

1. **Hold the battery retaining clip up and slide the battery into its socket.**

2. **Install the graphics card.**

   See Section 8.3.2 “Replacing the Graphics Card” on page 8-10.

3. **Install the CPU shroud cover.**

   See Section 8.8.2 “Replacing the CPU Shroud Assembly” on page 8-25.

4. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

5. **Reset the time of day and date.**

8.7 Motherboard

Perform the following procedures to remove and replace the motherboard. If necessary, view the ShowMe How video clip located on the Sun Blade 1000 Hardware Documentation CD-ROM.

Caution – Use an antistatic mat when working with the motherboard. An antistatic mat contains the cushioning needed to protect the underside components, to prevent motherboard flexing, and to provide antistatic protection.

Note – If you are replacing the motherboard, remove the audio module, graphics card(s), CPU module(s), and PCI card(s) prior to removing the motherboard. Note the chassis connector location for each graphics card and PCI card prior to removal.

Note – The system ID SEEPROM contains the system host identification (ID) and Ethernet address. If the same ID and Ethernet address are to be used on the replacement motherboard, remove the system ID SEEPROM from the motherboard and install the removed system ID SEEPROM on the replacement motherboard after motherboard installation. See Section FIGURE C-14 “System Motherboard Block Diagram” on page C-36.

8.7.1 Removing the Motherboard

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

2. **Lay the system on its side (**FIGURE 8-6**).**

3. **Remove the following**:

   a. **CPU module(s)**

      See Section 8.1.1 “Removing a CPU Module” on page 8-2.

   b. **PCI card(s)**

      See Section 8.2.1 “Removing a PCI Card” on page 8-5.

   c. **Graphics card(s)**

      See Section 8.3.1 “Removing the Graphics Card” on page 8-9.

   d. **Audio module**

      See Section 8.4.1 “Removing the Audio Module Assembly” on page 8-12.

4. **Disconnect the power supply cables from motherboard connectors J3601 and J3603.**

5. **Disconnect the following cables from the motherboard**:

   - Power supply cables to each fan
   - Combined cable assembly
   - Internal SCSI cable assemblies
   - Peripheral power cable assembly
   - FC-AL backplane cable assembly
   - Diskette drive cable assembly
   - Smart card reader cable assembly
   - Logo LED cable assembly

6. **Using a No. 2 Phillips screwdriver, remove the three screws securing the motherboard to the chassis back panel (**FIGURE 8-6**).**

Caution – Handle the motherboard by the CPU shroud or edges only.

7. **Separate the CPU shroud assembly by pressing the tabs together and withdrawing the CPU shroud cover from the chassis.**

8. **Using the attached part of the CPU shroud, push the motherboard carefully toward the front of the unit until it is disengaged from the chassis.**

9. **Lift the motherboard from the chassis and place it on an antistatic mat.**
10. **Remove the attached part of the CPU shroud.**

    See Section 8.8.1 “Removing the CPU Shroud Assembly” on page 8-24.
11. **Remove the DIMMs.**

    See Section 8.5.1 “Removing a DIMM” on page 8-14.
12. **Remove the system ID SEEPROM.**

    See FIGURE C-15 on page C-41.

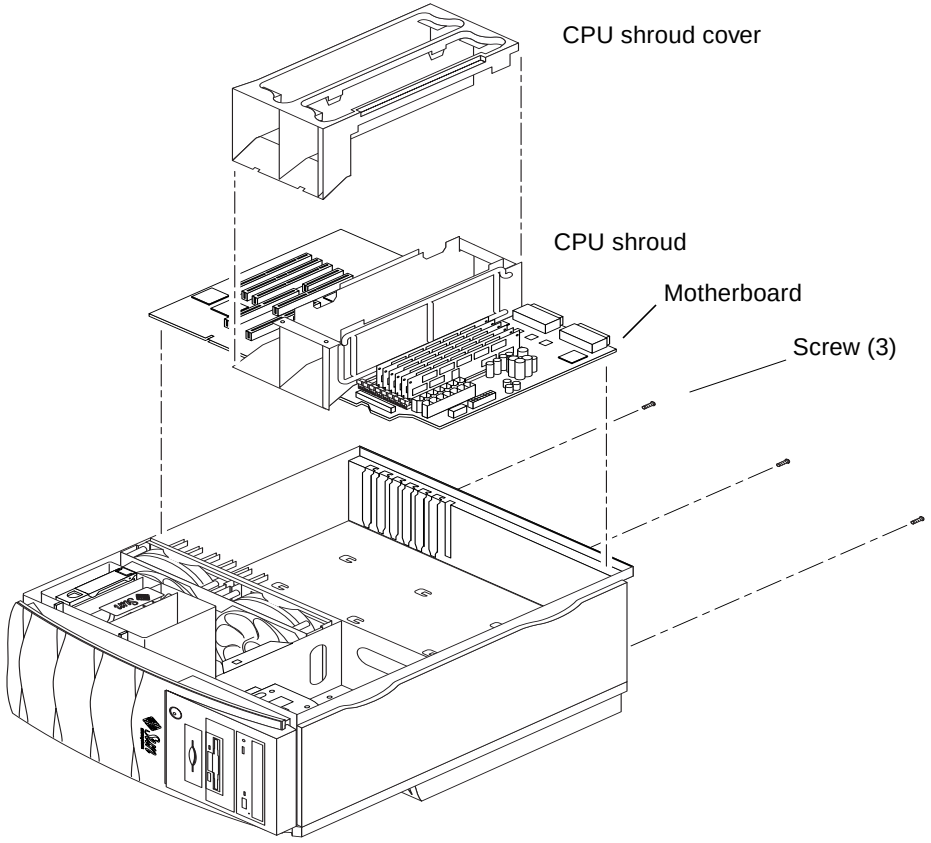


FIGURE 8-6 Removing and Replacing the Motherboard

8.7.2 Replacing the Motherboard

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Place the motherboard on an antistatic mat.**

Caution – Handle the motherboard by the shroud or edges only.

2. **Replace the system ID SEEPROM.**

   See FIGURE C-15 on page C-41.

3. **Install a new battery.**

   See Section 8.6.2 “Replacing the Battery” on page 8-17.

4. **Replace the DIMMs.**

   See Section 8.5.2 “Replacing a DIMM” on page 8-16.

5. **Replace the CPU shroud cover.**

   See Section 8.8.2 “Replacing the CPU Shroud Assembly” on page 8-25.

6. **Using needle-nosed pliers, remove the CPU connector covers.**

7. **Position the motherboard in the chassis (**FIGURE 8-6**).**

8. **Align the motherboard frame with the chassis tabs and carefully slide the motherboard toward the chassis back panel until the motherboard frame is engaged with the chassis tabs.**

9. **Using a No. 2 Phillips screwdriver, replace the three screws that secure the motherboard to the chassis back panel (**FIGURE 8-6**).**

Caution – Handle the motherboard by the CPU shroud or edges only.

10. **Connect the following cables to the motherboard:**

    - Power supply cables to each fan
    - Combined cable assembly
    - Internal SCSI cable assemblies
    - Peripheral power cable assembly
    - FC-AL backplane cable assembly
    - Diskette drive cable assembly
    - Smart card reader cable assembly

- Logo LED cable assembly

11. Connect the power supply cables to motherboard connectors J3601 and J3603.

12. Replace the following:

a. Audio card

See Section 8.4.2 “Replacing the Audio Module Assembly” on page 8-13.

b. Graphics card(s)

See Section 8.3.2 “Replacing the Graphics Card” on page 8-10.

c. PCI card(s)

See Section 8.2.2 “Replacing a PCI Card” on page 8-7.

d. CPU shroud assembly

See Section 8.8.2 “Replacing the CPU Shroud Assembly” on page 8-25.

e. CPU module(s)

See Section 8.1.2 “Replacing a CPU Module” on page 8-3.

13. Detach the antistatic wrist strap, replace the access panel, and power on the system.

See Chapter 9 “Finishing Replacement Procedures.”

14. Select RS-232 or RS-423 mode at serial ports A and B.

Note – The default setting at serial ports A and B is the RS-423 mode. To change the serial port mode proceed as follows.

---

a. At the `ok` prompt, type:

```
ok setenv ttya-mode 9600,8,n,1,-,rs232
   setenv ttyb-mode 9600,8,n,1,-,rs232
```

b. Type `reset-all` to implement the new mode.

Note – Setting only one of the `ttya` or `ttyb` rs232/rs423 mode variables causes both ports to be set to that mode.

---

15. Reset the *#power-cycles* NVRAM variable to zero as follows:

a. Press the keyboard Stop and A keys after the system banner appears on the monitor.

b. At the ok **prompt, type:**

```
ok setenv #power-cycles 0
```

c. Verify that the *#power-cycles* **NVRAM variable increments each time the system is power cycled.**

Note – The Solaris operating environment Power Management software uses the *#power-cycles* NVRAM variable to control the frequency of automatic system shutdown if automatic shutdown is enabled.

---

16. Verify proper operation.

See Section 3.4 “Maximum and Minimum Levels of POST” on page 3-5.

8.8 CPU Shroud Assembly

Use the following procedures to remove and replace the CPU shroud assembly.

8.8.1 Removing the CPU Shroud Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Power off the system, remove the access panel, and attach the antistatic wrist strap.**

   See Chapter 5 “Preparing for Component Removal and Replacement.”

2. **Lay the system on its side.**

3. **Remove the CPU shroud cover (**FIGURE 8-7**).**

   Squeeze the two tabs on the cover to release it from the CPU shroud assembly.

4. **Remove the CPU module(s)**

   See Section 8.1.1 “Removing a CPU Module” on page 8-2.

5. **Using a No. 2 Phillips screwdriver, loosen the six captive screws securing the CPU shroud assembly to the motherboard.**

6. **Lift the CPU shroud assembly from the motherboard (**FIGURE 8-7**).**

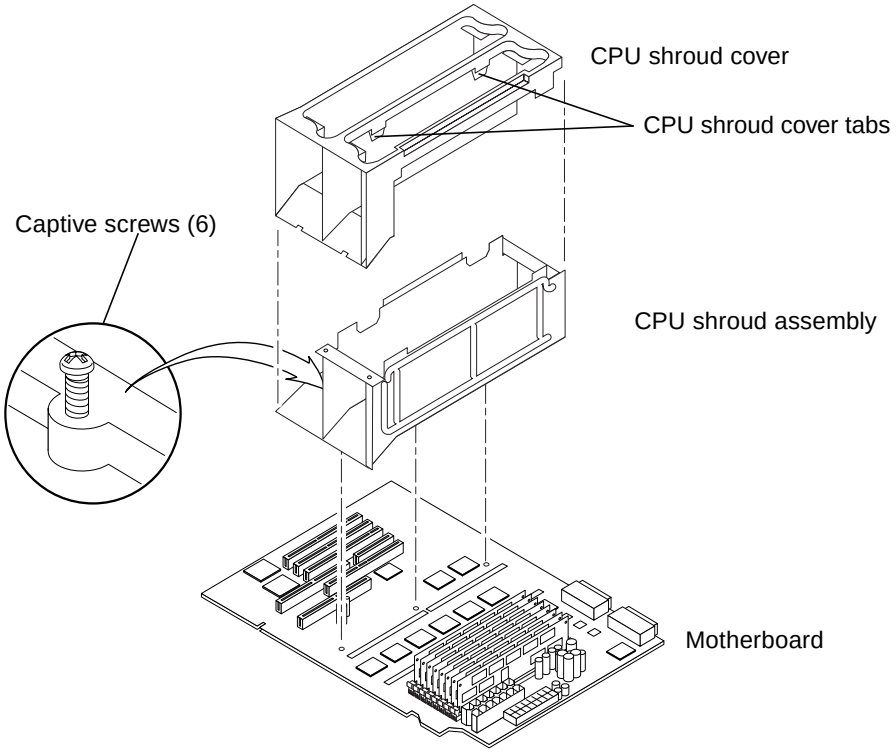


FIGURE 8-7 Removing and Replacing the CPU Shroud Assembly

8.8.2 Replacing the CPU Shroud Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Position and properly align the CPU shroud assembly on the motherboard (**FIGURE 8-7**).**
2. **Using a No. 2 Phillips screwdriver, tighten the six captive screws securing the CPU shroud assembly to the motherboard.**
3. **Replace the CPU module(s).**

   See Section 8.1.2 “Replacing a CPU Module” on page 8-3.
4. **Replace the CPU shroud cover (**FIGURE 8-7**).**

5. **Detach the antistatic wrist strap, replace the access panel, and power on the system.**

   See Chapter 9 “Finishing Replacement Procedures.”

CHAPTER 9

Finishing Replacement Procedures

This chapter describes the tasks you must do after you finish removing and replacing internal system components. The chapter also explains how to externally control standby operation.

This chapter covers the following topics:

9.1 Replacing the Access Panel

Perform the following procedure to replace the access panel and power on the system. if necessary, view the ShowMe How video clip located on the Sun Blade 1000 Hardware Documentation CD-ROM.

Caution – If the access panel is installed incorrectly, the power interlock circuit will remain activated. Ensure that the access panel is installed correctly.

1. **Remove the antistatic strap.**
2. **Hold the access panel, centering it over the chassis opening (**FIGURE 9-1**).**
3. **Position the access panel lightly onto the chassis until the access panel hooks engage the chassis rail.**
4. **Press the top edge of the access panel until it clicks into place.**
5. **Be sure that the access panel clicks into both sides of the chassis top.**
6. **Replace the lock block (if necessary) (**FIGURE 9-2**).**

7. **Reconnect all external peripherals.**
8. **Reconnect power cords on all external peripherals.**
9. **Connect the power cord to the wall socket and to the system.**

.

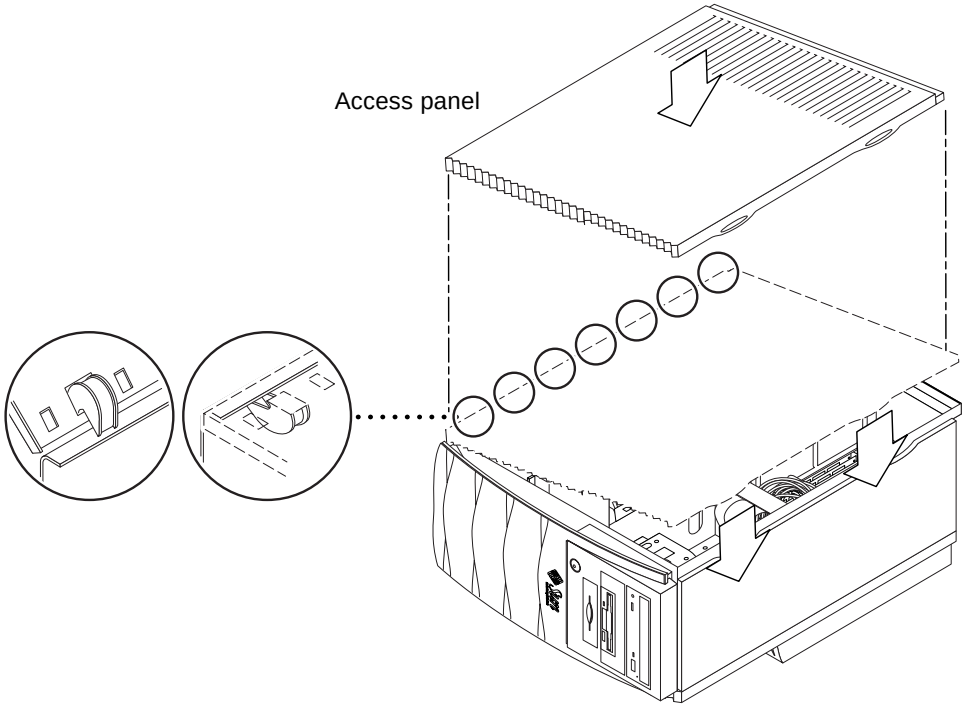


FIGURE 9-1 Replacing the Access Panel

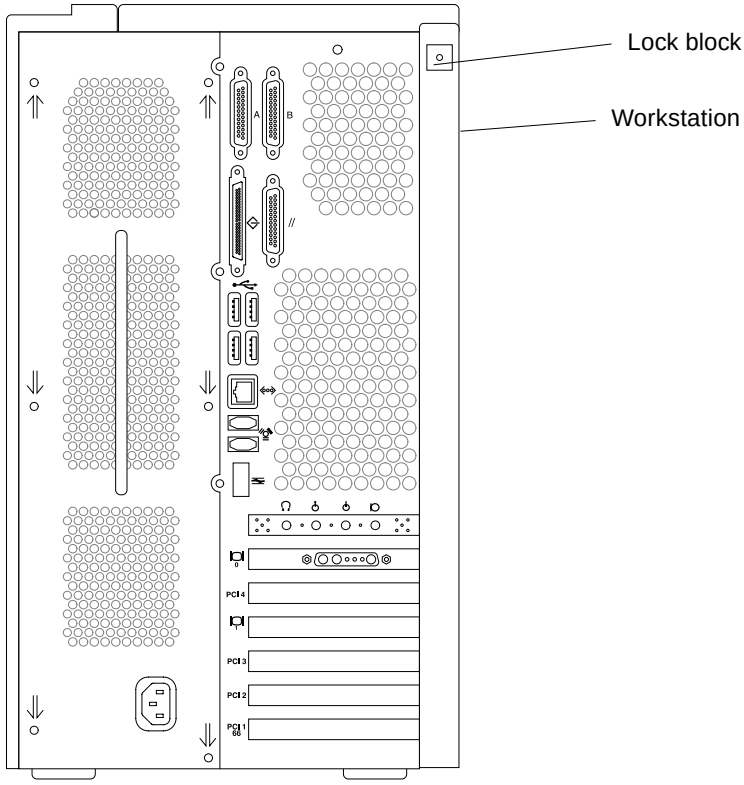


FIGURE 9-2 Lock Block Location

10. Turn on the power to all connected peripherals.

Note – Peripheral power is activated prior to system power so that the system can recognize the peripherals when it is activated.

9.2 Powering On the System

Power on the system as follows:

1. **Turn on power to the monitor and to all external devices.**
2. **Press the power switch on the front panel and release it (**FIGURE 9-3**).**
3. **After several seconds, verify that the Sun logo on the system front panel energizes immediately, verify that the power indicator LED on the power switch is energized and listen to verify that the system fans are spinning.**

Note – The power indicator LED on the power switch will energize after the system begins the internal boot process.

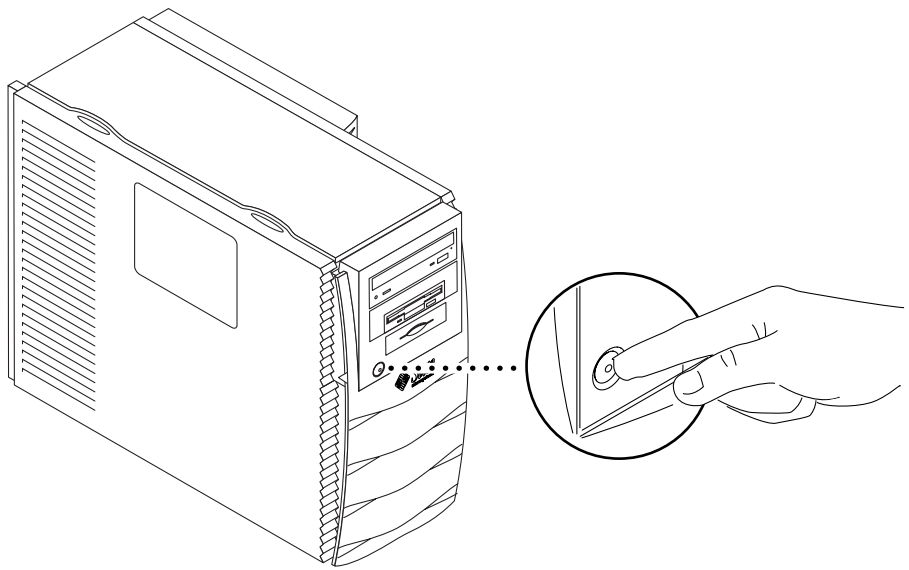


FIGURE 9-3 System Power Switch

CHAPTER 10

OpenBoot Emergency Procedures

The introduction of USB keyboards with Sun's newest desktop systems has made it necessary to change some of the OpenBoot™ emergency procedures. Specifically, the Stop-N, Stop-D, and Stop-F commands that are available on systems that have standard (non-USB) keyboards and are not supported on systems that have USB keyboards. The following sections describe the OpenBoot emergency procedures for systems with standard keyboards and for newer systems with USB keyboards.

10.1 OpenBoot Emergency Procedures for Systems with Standard (non-USB) Keyboards

When issuing any of these commands, hold down the keys immediately after turning on the power to your system, and keep them pressed for a few seconds until the keyboard LEDs flash.

Command	Description
Stop	Bypass POST. This command does not depend on security-mode. (Note: Some systems bypass POST as a default; in such cases, use Stop-D to start POST).
Stop-A	Abort.
Stop-D	Enter the diagnostic mode (set `diag-switch?` to `true`).
Stop-F	Enter Forth on TTYA instead of probing. Use fexit to continue with the initialization sequence. This command is useful if your hardware is broken.
Stop-N	Reset NVRAM contents to default values.

10.2 OpenBoot Emergency Procedures for Systems with USB Keyboards

The following paragraphs describe how to perform the functions of the Stop-commands on systems that have USB keyboards.

10.2.1 Stop-A

Stop-A (Abort) works the same as it does on systems with standard keyboards, except that it does not work during the first few seconds after the machine is reset.

10.2.2 Stop-N Functionality

1. **After turning on the power to your system, wait until the front panel power button LED begins to blink and you hear an audible beep.**
2. **Quickly press the front panel power button twice (similar to the way you would double-click a mouse).**

   A screen similar to the following is displayed to indicate that you have successfully reset NVRAM contents to the default values. If a screen similar to the following does not appear, repeat steps 1 and 2.

```
Sun Blade 1000 2 (2 X UltraSPARC-III), Keyboard Present
OpenBoot 4.0, 256 MB memory installed, Serial #12134241.
Ethernet address 8:0:20:b9:27:61, Host ID: 80b92761.


Safe NVRAM mode, the following nvram configuration variables have
been overridden:
   'diag-switch?' is true
   'use-nvramrc?' is false
   'input-device', 'output-device' are defaulted
   'ttya-mode', 'ttyb-mode' are defaulted

These changes are temporary and the original values will be restored
after the next hardware or software reset.

ok
```

Some NVRAM configuration parameters are reset to their defaults. They include parameters that are more likely to cause problems, such as TTYA settings. These NVRAM settings are only reset to their defaults for this power cycle. If you do nothing other than resetting the system at this point, the values are not permanently changed. Only settings that you change manually at this point become permanent. All other customized NVRAM settings are retained.

Typing **`set-defaults`** discards any customized NVRAM values and permanently restores the default settings for all NVRAM configuration parameters.

Note – Once the power button LED stops blinking and stays lit, pressing the power button again will power off the system.

10.2.3 Stop-F Functionality

The Stop-F functionality is not available in systems with USB keyboards.

10.2.4 Stop-D Functionality

The Stop-D (diags) key sequence is not supported on systems with USB keyboards, however, the Stop-D functionality can be closely emulated by using the power button double-tap (see Stop-N Functionality), since this temporarily sets `diag-switch?` to `true`. If you want the diagnostic mode turned on permanently, type:

```
ok setenv diag-switch? true
```

APPENDIX **A**

Product Specifications

This appendix provides product specifications for the Sun Blade 1000 system.

A.1 Physical Specifications

TABLE A-1 System Physical Specifications

Specification	U.S.A.	Metric
Height	17.8 in.	452 mm
Width	10.0 in.	254 mm
Depth	23.7 in.	602 mm
Weight (approximate)	70.0 lbs	32 Kg

A.2 Electrical Specifications

TABLE A-2 Electrical Specifications

Parameter	Value
AC input	100 to 240 Vac, 47 to 63 Hz, 0.8 KVA
DC output	670W (maximum)
Output 1	+3.3 VDC, 90A
Output 2	+5.0 VDC, 70A
Output 3	+12.0 VDC, 8.0A
Output 4	-12.0 VDC, 0.4A
Output 5	5.0 VDC, 1.5A

A.3 Environmental Requirements

TABLE A-3 Environmental Requirements

Environmental Factor	Operating Parameters	Non-operating Parameters
Temperature (with tape drive)	41 to 95 degrees F (5 to 35 degrees C)	-40 to 140 degrees F (-40 to 60 degrees C)
Temperature (without tape drive)	41 to 104 degrees F (5 to 40 degrees C)	-40 to 140 degrees F (-40 to 60 degrees C)
Humidity	5 to 90% at 104 degrees F (40 degrees C) noncondensing	5 to 93% at 104 degrees F (40 degrees C)
Altitude (with tape drive)	10,000 ft (3 km) at 86 degrees F (30 degrees C)	40,000 ft (12 km) at 32 degrees F (0 degrees C)
Altitude (without tape drive)	10,000 ft (3 km) at 95 degrees F (35 degrees C)	40,000 ft (12 km) at 32 degrees F (0 degrees C)
Maximum dwells at extremes	16 hr	16 hr

APPENDIX **B**

Signal Descriptions

This appendix describes the system motherboard connector signals and pin assignments.

B.1 Power Connectors

The motherboard has seven power connectors. The following table lists these power connectors, the connector use, and the supporting figure and table. FIGURE C-15 on page C-39 identifies the motherboard connector location.

TABLE B-1 Power Connectors

Connector	Use	Supporting Figure	Supporting Table
J3603	Power from power supply	FIGURE B-1 on page B-2	TABLE B-2 on page B-2
J3601	Power from power supply	FIGURE B-2 on page B-3	TABLE B-3 on page B-3
J3302	Power to PCI fan	FIGURE B-3 on page B-4	TABLE B-4 on page B-4
J3303	Power to CPU fan	FIGURE B-4 on page B-4	TABLE B-5 on page B-4
J3602	Power to combined cable assembly	FIGURE B-5 on page B-5	TABLE B-6 on page B-5
J3608	Power to peripheral power cable assembly	FIGURE B-6 on page B-5	TABLE B-7 on page B-5

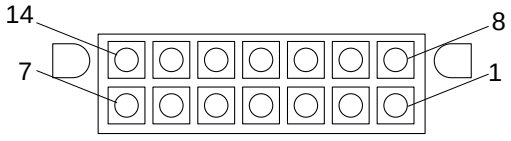


FIGURE B-1 Power Supply Connector J3603

TABLE B-2 Power Supply Connector J3603 Pin Description

Pin	Signal	Description
1	POWERON_L	Power on
2	-12 VDC	-12 VDC
3	+5 VDC Return (SENSE)	+5 VDC Return
4	+3.3 VDC Return (SENSE)	+3.3 VDC Return
5	RETURN	Return
6	RETURN	Return
7	Spare	Spare

TABLE B-2 Power Supply Connector J3603 Pin Description *(Continued)*

Pin	Signal	Description
8	POWER_OK	Power ok
9	PS_FAN	Fan power
10	+5 VDC (SENSE)	+5 VDC (Sense)
11	+3.3 VDC (SENSE)	+3.3 VDC (Sense)
12	+12 VDC	+12 VDC
13	+12 VDC	+12 VDC
14	+5 VDC_STBY	+5 VDC standby

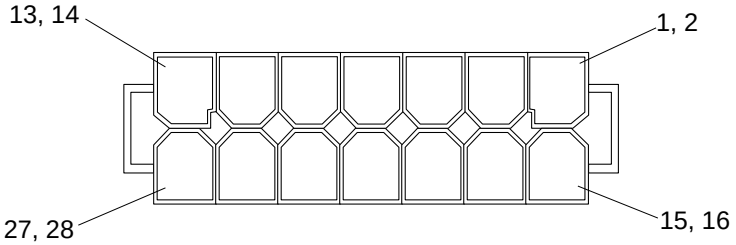


FIGURE B-2 Power Supply Connector J3601

TABLE B-3 Power Supply Connector J3601 Pin Description

Pin	Signal	Description
1, 2	+3.3 VDC	+3.3 VDC
3, 4	+3.3 VDC	+3.3 VDC
5, 6	+3.3 VDC	+3.3 VDC
7, 8	+3.3 VDC	+3.3 VDC
9, 10	+5 VDC	+5 VDC
11, 12	+5 VDC	+5 VDC
13, 14	+5 VDC	+5 VDC
15, 16	RETURN +3.3 VDC	+3.3 VDC Return
17, 18	RETURN +3.3 VDC	+3.3 VDC Return
19, 20	RETURN +3.3 VDC	+3.3 VDC Return
21, 22	RETURN +3.3 VDC	+3.3 VDC Return

TABLE B-3 Power Supply Connector J3601 Pin Description *(Continued)*

Pin	Signal	Description
23, 24	RETURN +5 VDC	+5 VDC Return
25, 26	RETURN +5 VDC	+5 VDC Return
27, 28	RETURN +5 VDC	+5 VDC Return

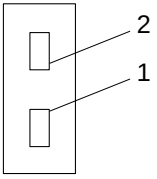


FIGURE B-3 PCI Fan Connector J3302

TABLE B-4 PCI Fan Connector J3302 Pin Description

Pin	Signal	Description
1	FAN_V_OUT0	Fan voltage
2	GND	Ground

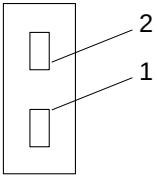


FIGURE B-4 CPU Fan Connector J3303

TABLE B-5 CPU Fan Connector J3303 Pin Description

Pin	Signal	Description
1	FAN_V_OUT1	Fan voltage
2	GND	Ground

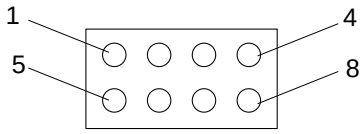


FIGURE B-5 Combined Cable Assembly Connector J3602

TABLE B-6 Combined Cable Assembly Connector J3602 Pin Description

Pin	Signal	Description
1	VCC	Voltage at the common collector
2	SPEAKER_OUT+	Speaker out +
3	SWITCH_L	Switch low
4	POWERON_L	Power on low
5	SYS LED	System LED
6	SPEAKER_OUT-	Speaker out–
7	GND	Ground
8	INTERLOCK_L	Interlock low

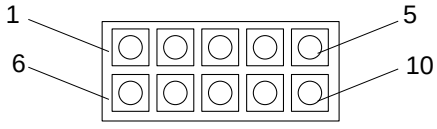


FIGURE B-6 Peripheral Power Cable Assembly Connector J3608

TABLE B-7 Peripheral Power Cable Assembly Connector J3608 Pin Description

Pin	Signal	Description
1	VCC	Voltage at the common collector
2	VCC	Voltage at the common collector
3	VCC	Voltage at the common collector
4	+12 VDC	+12 VDC
5	+12 VDC	+12 VDC
6	GND	Ground
7	GND	Ground

TABLE B-7 Peripheral Power Cable Assembly Connector J3608 Pin Description

Pin	Signal	Description
8	GND	Ground
9	GND	Ground
10	GND	Ground

B.2 Serial Ports A and B

The serial port A and B connectors (J2001) are DB-25 connectors located on the motherboard back panel.

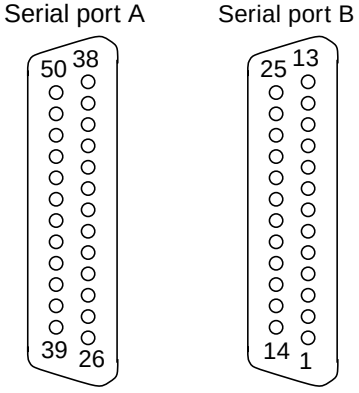


FIGURE B-7 Serial Port A and B Connector Pin Configuration

TABLE B-8 Serial Port A and B Connector Pin Assignments

Pin	Signal	Description
1	NC	Not connected
2	SER_TDX_A_CONN	Transmit data
3	SER_RXD_A_CONN	Receive data
4	SER_RTS_A_L_CONN	Ready to send
5	SER_CTS_A_L_CONN	Clear to send

TABLE B-8 Serial Port A and B Connector Pin Assignments *(Continued)*

Pin	Signal	Description
6	SER_DSR_A_L_CONN	Data set ready
7	GND	Signal ground
8	SER_DCD_A_L-CONN	Data carrier detect
9	BUTTON_POR	Power-on reset
10	BUTTON_XIR_L	Transmit internal reset
11	+5VDC	+5 VDC
12	NC	Not connected
13	NC	Not connected
14	NC	Not connected
15	SER_TRXC_A_L_CONN	Transmit clock
16	NC	Not connected
17	SER_RXC_A_L_CONN	Receive clock
18	NC	Not connected
19	NC	Not connected
20	SER_DTR_A_L_CONN	Data terminal ready
21	NC	Not connected
22	NC	Not connected
23	NC	Not connected
24	SER_TXC_A_L_CONN	Terminal clock
25	NC	Not connected

B.3 Ultra SCSI Connector

The Ultra small computer system interface (Ultra SCSI) connector (J2202) is located on the motherboard back panel.

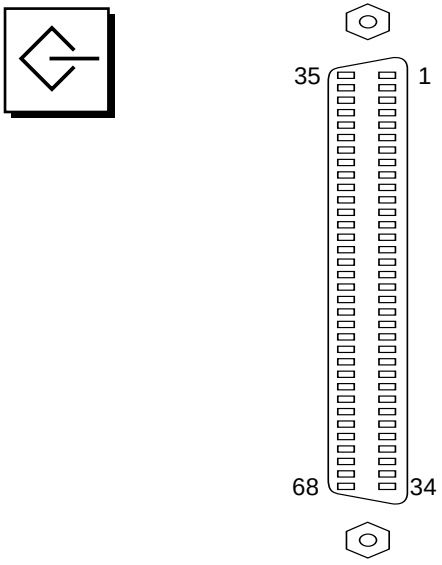


FIGURE B-8 Ultra SCSI Connector Pin Configuration

TABLE B-9 Ultra SCSI Connector Pin Assignments

Pin	Signal	Description
1	GND	Ground
2	GND	Ground
3	NC	Not connected
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	GND	Ground

TABLE B-9 Ultra SCSI Connector Pin Assignments *(Continued)*

Pin	Signal	Description
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	TERMPOWER	Termpower
18	TERMPOWER	Termpower
19	NC	Not connected
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	GND	Ground
29	GND	Ground
30	GND	Ground

TABLE B-9 Ultra SCSI Connector Pin Assignments *(Continued)*

Pin	Signal	Description
31	GND	Ground
32	GND	Ground
33	GND	Ground
34	GND	Ground
35	SCSI_B_DAT<12>	Data 12
36	SCSI_B_DAT<13>_	Data 13
37	SCSI_B_DAT<14>_	Data 14
38	SCSI_B_DAT<15>_	Data 15
39	SCSI_B_PAR<l>	Parity 1
40	SCSI_B_DAT<0>_	Data 0
41	SCSI_B_DAT<1>_	Data 1
42	SCSI_B_DAT<2>_	Data 2
43	SCSI_B_DAT<3>_	Data 3
44	SCSI_B_DAT<4>_	Data 4
45	SCSI_B_DAT<5>_	Data 5
46	SCSI_B_DAT<6>_	Data 6
47	SCSI_B_DAT<7>_	Data 7
48	SCSI_B_PAR<0>	Parity 0
49	GND	Ground
50	NC	Not connected
51	TERMPOWER_B	Terminal B power
52	TERMPOWER_B	Terminal B power
53	NC	Not connected

TABLE B-9 Ultra SCSI Connector Pin Assignments *(Continued)*

Pin	Signal	Description
54	GND	Ground
55	SCSI_B_ATN_L	Attention
56	GND	Ground
57	SCSI_B-BSY_L	Busy
58	SCSI_B_ACK_L	Acknowledge
59	SCSI_B_RESET_L	Reset
60	SCSI_B_MSG_L	Message
61	SCSI_B_SEL_L	Select
62	SCSI_B-CD_L	Command
63	SCSI_B_REQ_L	Request
64	SCSI_B_IO_L	In/out
65	SCSI_B_DAT<8>_	Data 8
66	SCSI_B_DAT<9>_	Data 9
67	SCSI_B_DAT<10>_	Data 10
68	SCSI_B_DAT<11>_	Data 11

Note – _ (underscore) signifies active low.

B.4 Parallel Port Connector

The parallel port connector (J2202) is a DB-25 connector located on the motherboard back panel.

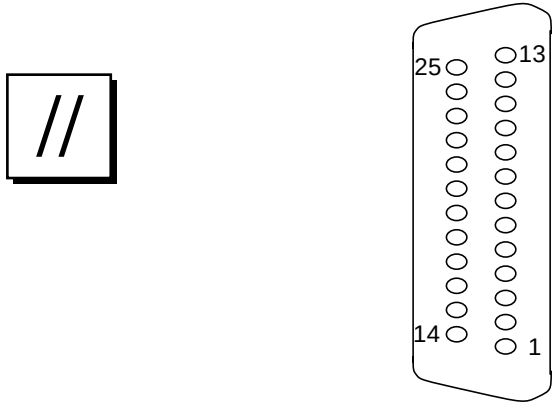


FIGURE B-9 Parallel Port Connector Pin Configuration

TABLE B-10 Parallel Port Connector Pin Assignments

Pin	Signal	Description
1	PAR_DS_L_CONN	Data strobe low
2 to 9	PP_DAT[0.7]_CONN	Data0 thru data7
10	PAR_ACK_L_CONN	Acknowledge low
11	PAR_BUSY_CONN	Busy
12	PAR_PE_CONN	Parity error
13	PAR_SELECT_L_CONN	Select low
14	PAR_AFXN_L_CONN	Auto feed low
15	PAR_ERROR_L_CONN	Error low
16	PAR_INIT_L_CONN	Initialize low
17	PAR_IN_L_CONN	Peripheral input low

TABLE B-10 Parallel Port Connector Pin Assignments *(Continued)*

Pin	Signal	Description
18	GND	Chassis ground
19	GND	Chassis ground
20	GND	Chassis ground
21	GND	Chassis ground
22	GND	Chassis ground
23	GND	Signal ground
24	GND	Signal ground
25	GND	Signal ground

B.5 Universal Serial Bus Connector

Two universal serial bus (USB) connectors (J3001, 3002) are located on the motherboard back panel.

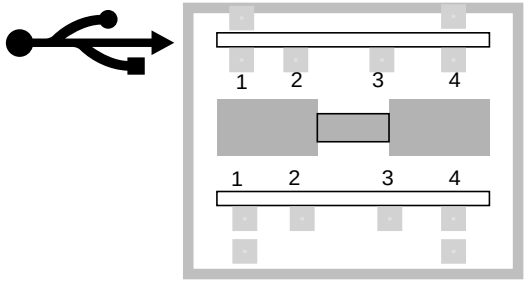


FIGURE B-10 USB Connector Pin Configuration

TABLE B-11 USB Connector Pin Assignments

Pin	Signal Name	Description
A1	USB0_VCC	+5 VDC
A2	CM_USB_D0_N	port0data_N
A3	CM_USB_D0_P	port0data_P

TABLE B-11 USB Connector Pin Assignments *(Continued)*

Pin	Signal Name	Description
A4	GND	ground
B1	USB1_VCC	+5 VDC
B2	CM_USB_D1_N	port1data_N
B3	CM_USB_D1_P	port1data_P
B4	GND	ground

B.6 IEEE 1394 Connector

Two IEEE 1394 connectors (J3201, 3203) are located on the rear panel.

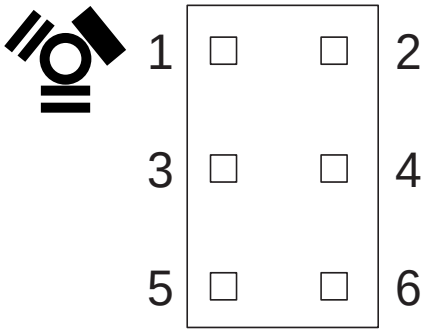


FIGURE B-11 IEEE 1394 Connector Pin Configuration

TABLE B-12 IEEE 1394 Connector Pin Assignments

Pin	Signal Name	Description
1	P1394_EX_BUSPOWER	+12 VDC / 33 VDC
2	GND	ground
3	CM_P1394_TPB1_OUT_N	TPB1_Ndata -
4	CM_P1394_TPB1_OUT_P	TPB1_Pdata +
5	CM_P1394_TPA1_OUT_N	TPA1_Ndata -
6	CM_P1394_TPA1_OUT_P	TPA2_Pdata +

B.7 Twisted-Pair Ethernet Connector

The twisted pair Ethernet (TPE) connector (J5301) is an RJ-45 connector located on the motherboard back panel.

Caution – Connect only TPE cables to the TPE connector.

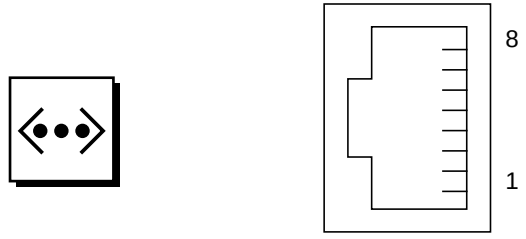


FIGURE B-12 TPEConnector Pin Configuration

TABLE B-13 TPE Connector Pin Assignments

Pin	Signal	Description
1	Common mode termination	Termination
2	Common mode termination	Termination
3	TX+	Transmit data +
4	+5VDC	+5VDC
5	TX-	Transmit data -
6	RX+	Receive data +
7	RX-	Receive data -
8	Common mode termination	Termination

B.7.1 TPE Cable-Type Connectivity

The following types of TPE cables can be connected to the TPE connector.

- For 10BASE-T applications, unshielded twisted-pair (UTP) cable:
  - Category 3 (UTP-3, voice grade)
  - Category 4 (UTP-4)
  - Category 5 (UTP-5, data grade)
- For 100BASE-T applications, UTP cable, UTP-5, data grade

B.7.2 External UTP-5 Cable Lengths

The following table lists TPE UTP-5 types, applications, and maximum lengths.

TABLE B-14 TPE UTP-5 Cables

Cable Type	Application(s)	Maximum Length (Metric)	Maximum Length (U.S.)
UTP-5, “data grade”	10BASE-T or 100BASE-T	100 meters	109 yards

B.8 Audio Connectors

The audio connectors are located on the audio card. The connectors use EIA standard 3.5-mm/0.125-inch jacks.

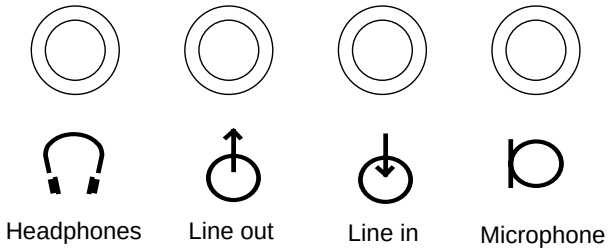


FIGURE B-13 Audio Connector Configuration

TABLE B-15 Audio Connector Line Assignment

Component	Headphones	Line Out	Line In	Microphone
Tip	Left channel	Left channel	Left channel	Left channel
Ring (center)	Right channel	Right channel	Right channel	Right channel
Shield	Ground	Ground	Ground	Ground

B.9 FC-AL Rear Panel Connector

The FC-AL connector, J2902, is located on the rear panel.

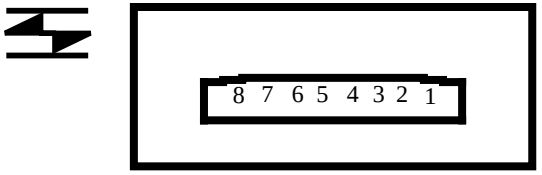


FIGURE B-14 FC-AL Connector Configuration

TABLE B-16 FC-AL Connector Pin Assignments

Pin	Signal	Description
1	T_CM_FC_TX_EX_P	Transmit data +
2	GND	ground
3	T_CM_FC_TX_EX_N	Transmit data -
4, 5	NC	
6	FC_RX_EX_N	Receive data -
7	GND	ground
8	FC_RX_EX_P	Receive data +

B.10 Graphics Card Connectors

The graphics card connector is located on the graphics card.

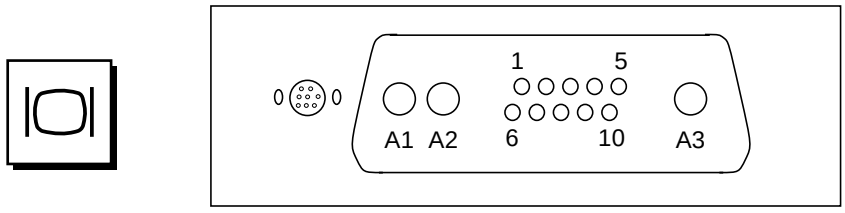


FIGURE B-15 Graphics Card Connector Pin Configuration

TABLE B-17 Graphics Card Connector Pin Assignments

Pin	Signal Name	Description
A1	R	Red
A2	G	Green
A3	B	Blue
1	Serial Read	Serial read
2	Vert Sync	Vertical sync
3	Sense <0>	Sense <0>
4	GND	Ground
5	Comp Sync	Composite sync
6	Horiz Sync	Horizontal sync
7	Serial Write	Serial write
8	Sense <1>	Sense <1>
9	Sense <2>	Sense <2>
10	GND	Ground

B.11 Smart Card Reader Connector

The smart reader connector J3604 is located on the motherboard.

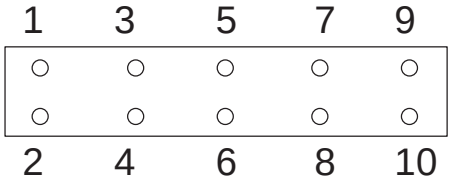


FIGURE B-16 Smart Card Reader Connector, J3604, Pin Assignments

TABLE B-18 Smart Card Reader, J3604, Pin Assignments

Pin	Signal Name	Description
1	+12 VDC	+12VDC power
2	GND	Ground
3	GND	Ground
4	I2C_SCL	I2C bus clock
5	+5 VDC	+5 VDC power
6	I2C_SDA	I2C bus data
7	GND	Ground
8	GND	Ground
9	Int_L	
10	NC	No connection

B.12 Diskette Drive Connector

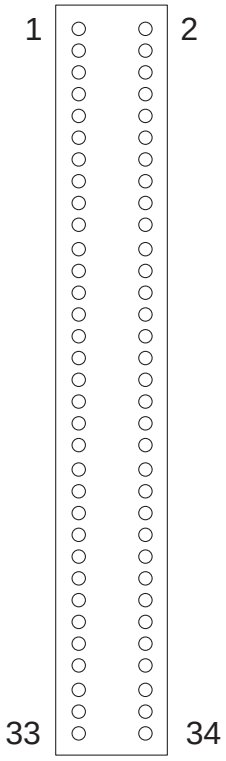


FIGURE B-17 Diskette Drive Connector, J1801

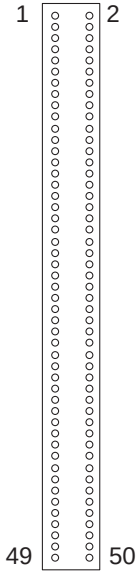
TABLE B-19 Diskette Drive Connector, J1801, Signals and Functions

Pin	Signal Name	Function
1	FLOPPY_ESECT	NC
2	MODE_SELECT	When active low, MODE_SELECT sets the drive for a 1.2-Mbyte formatted disk. When active high, MODE_SELECT sets the drive for a 1.44-Mbyte formatted disk.
4	HIGH_DENSITY_IN_L	When active low, HIGH_DENSITY_IN_L indicates that a high-density disk is inserted into the drive.
8	INDEX	When active, INDEX indicates the beginning of each track. An active pulse is sent for each disk rotation.
10, 12	DRIVE_SELECT	When set true, DRIVE_SELECT enables the drive to respond to other input signals.
16	MOTOR_ENABLE	When set low, MOTOR_ENABLE initiates the spindle motor rotation.
18	DIRECTION	When active high, DIRECTION indicates movement of the magnetic head assembly toward the outer cylinders. When active low, DIRECTION indicates movement of the magnetic head assembly toward the inner cylinders.
20	STEP	On the trailing edge, STEP moves the magnetic head in the direction specified by DIRECTION at a rate of one cylinder per pulse.
22	WRITE_DATA	WRITE_DATA supplies the disk drive with the data to be written to disk provided the WRITE_GATE signal is active low.
24	WRITE_GATE	When active low, WRITE_GATE enables the drive write circuits. When active high, WRITE_GATE enables drive read circuits.
26	TRACK0	When active low, TRACK0 indicates that the track zero sensor has been activated and that the heads are over the outermost cylinder.
28	WRITE_PROTECT	When active low, WRITE_PROTECT indicates that the inserted diskette is write-protected and that drive write operations are disabled.
30	READ_DATA	When active, READ_DATA enables data from the disk to be transferred to the host through this signal line.

TABLE B-19 Diskette Drive Connector, J1801, Signals and Functions *(Continued)*

Pin	Signal Name	Function
32	HEAD_SELECT	When low, HEAD_SELECT selects head 1. When high, HEAD_SELECT selects head 0.
34	DISK_CHANGE	When low, DISK_CHANGE indicates that the drive tape medium has been changed. DISK_CHANGE is reset when a new disk is inserted and an enable signal is sent by the host.
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33	GND	

B.13 Internal SCSI Connector



Internal SCSI Connector, J5002

TABLE B-20 Internal SCSI Connector, J5002

Pin	Signal Name
1-19, 20-22, 24, 29-31, 33-35, 37, 39, 41, 43, 45, 47, 49	GND
2, 4, 6, 8, 10, 12, 14, 16	SCSI data bus
18	SCSI_A_PAR<0>
26	Termpowr_A
32	SCSI_A_ATN_L
36	SCSI_A_BSY_L
38	SCSI_A_ACK_L
40	SCSI_A_RESET_L

TABLE B-20 Internal SCSI Connector, J5002 *(Continued)*

Pin	Signal Name
42	SCSI_A_MSG_L
44	SCSI_A_SEL_L
46	SCSI_A_CD_L
48	SCSI_A_REQ_L
50	SCSI_A_IO_L

B.14 Internal FC-AL Connector

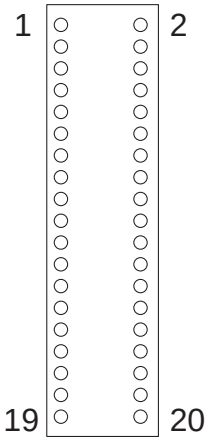


FIGURE B-18 Internal FC-AL Connector, J2901

TABLE B-21 Internal FC-AL Connector, J2901

Pin	Signal Name
1	Dr1_PB1_F_1
2	DR2PB2_F_1
3, 4, 7, 8, 11, 12, 15, 16, 19, 20	GND

TABLE B-21 Internal FC-AL Connector, J2901 *(Continued)*

Pin	Signal Name
5	T_DR2_PORT2IN_P
6	T_DR2_PORT2IN_N
9	DR2_PORT2OUT_P
10	DR2_PORT2OUT_N
13	T_DR1_PORT1IN_P
14	T_DR1_PORT1IN_N
17	DR1_PORT1OUT_P
18	DR1_PORT1OUT_N

B.15 Logo LED Connector

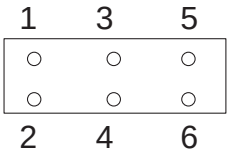


FIGURE B-19 Logo LED Connector, J3605

TABLE B-22 Logo LED Connector, J3605

Pin	Signal Name
1	LED1 anode
2	LED3 cathode
3	LED2 cathode

TABLE B-22 Logo LED Connector, J3605

Pin	Signal Name
4	LED3 anode
5	LED2 anode
6	LED1 cathode

APPENDIX **C**

Functional Description

This appendix provides functional descriptions for the following:

C.1 System

This section is organized into the following subsections:

C.1.1 System Overview

Sun customers can purchase the Sun Blade 1000 workstation as a single or dual UltraSPARC-III processor controlled desktop system. The Sun Blade 1000 uses shared-memory multiprocessor architecture with both processors installed on a single motherboard (See FIGURE C-1, a functional block diagram of the Sun Blade 1000 system).

Each UltraSPARC-III processor has a memory controller installed within the processor module. When two UltraSPARC-III modules are installed on a Sun Blade 1000 workstation, only the memory controller installed in CPU slot 0 is enabled.

The Sun Blade 1000 I/O subsystem is designed around a system bus controller (SBC) ASIC, which is a bridge between the Sun CrossBar Interconnect address bus, the UPA64S, and the 33 and 66 MHz PCI buses. The UPA64S is used exclusively to exchange blocks of graphics information between the graphics card and the SBC ASIC.

Two PCI buses interface with the FC-AL controller and any other boards that are installed in the workstation's PCI slots. A 33 MHz PCI bus (PCI-B) supports SCSI controllers that interface with the internal DVD-ROM, or tape drives. A 66 MHz PCI bus (PCI-A or EPCI for extended PCI bus) supports the Fibre Channel-Arbitrated Loop (FC-AL) controller that interfaces with the hard disk drives.

The 33 MHz PCI-B I/O buses are supported by the Peripheral Component I/O-2 (PCIO-2) ASIC. This ASIC is an interface between the 33 MHz PCI bus, the IEEE 1394 port, external universal serial buses (USB), the 10/100 Mbit Ethernet ports, the boot PROM, and the EBus.

Note – EBus is a slow byte-wide bus for low-speed devices such as the serial port controller, the audio module, the SuperI/O controller (used primarily as diskette drive and parallel port interface), and the boot PROM.

A BootBus controller (BBC) ASIC is connected to both UltraSPARC-III modules through a shared BootBus. The BBC ASIC bridges the BootBus to the EBus, to which slow I/O devices and the boot PROM are attached. The BBC ASIC incorporates an I2C bus interface and a JTAG master controller. The inter-integrated circuit (I2C) controller is used to identify the processor modules, the DIMMs and for environmental control. The JTAG master controller is used for boundary testing on the system board, ASIC, and processor testing.

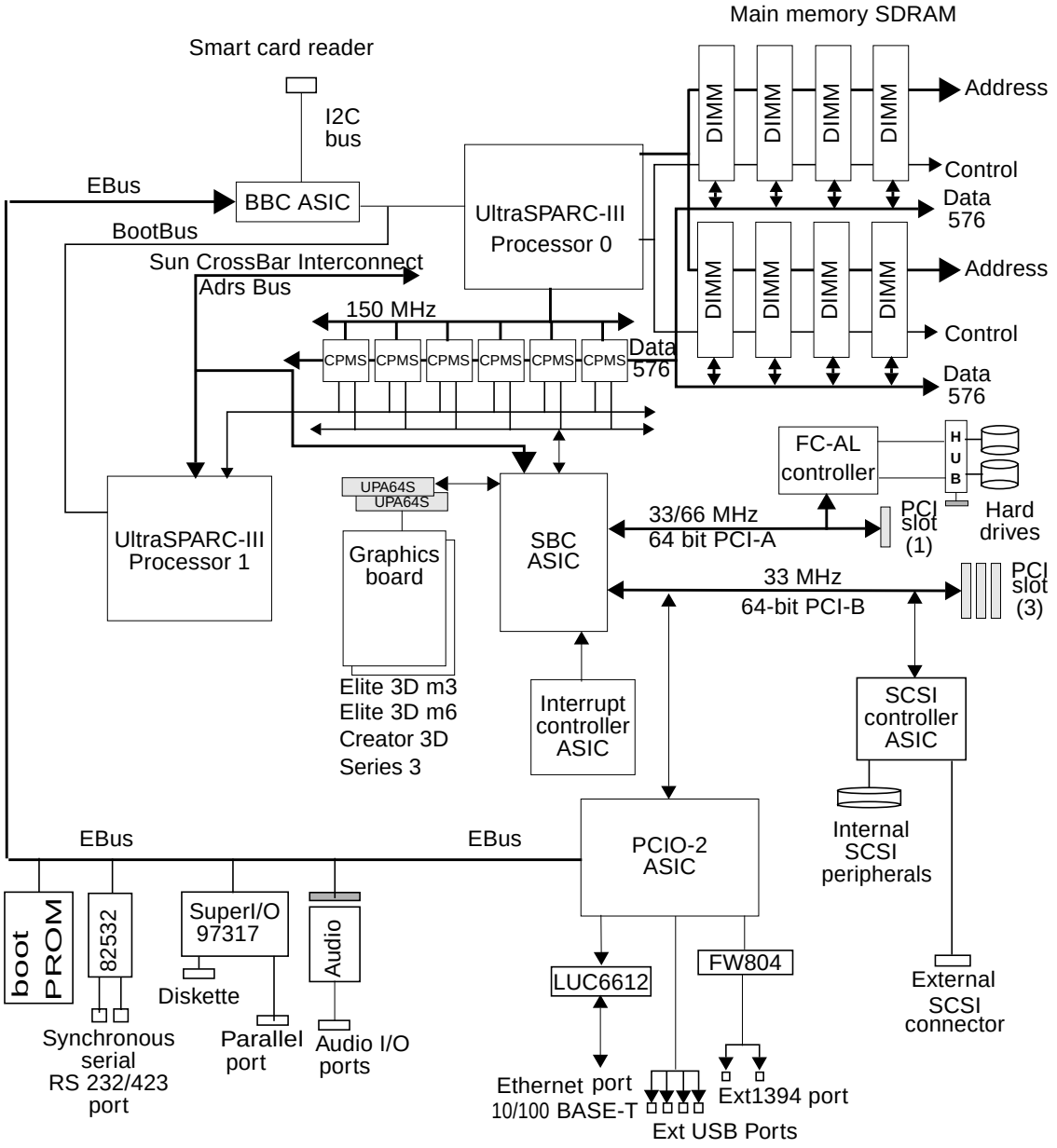


FIGURE C-1 Sun Blade 1000 System Functional Block Diagram

C.1.2 UltraSPARC-III Processor

Each UltraSPARC-III processor (CPU module) implements the SPARC V-9 architecture with the Visual Instruction Set (VIS™) extension. The CPU module also provides new VIS extensions along with prefetch instructions (FIGURE C-2 below is an UltraSPARC-III processor functional block diagram).

The CPU is physically mounted on a module that plugs vertically into the system motherboard. The module contains the processor and eight external cache SRAMs, available either as 4-Mbyte (8 x 4-Mbit) SRAMs or as 8 Mbyte (8 x 8 Mbit) SRAMs.

The module also includes a DC-to-DC converter to limit the current density in the connector at the male/female interface to provide better power regulation at the pins of the processor.

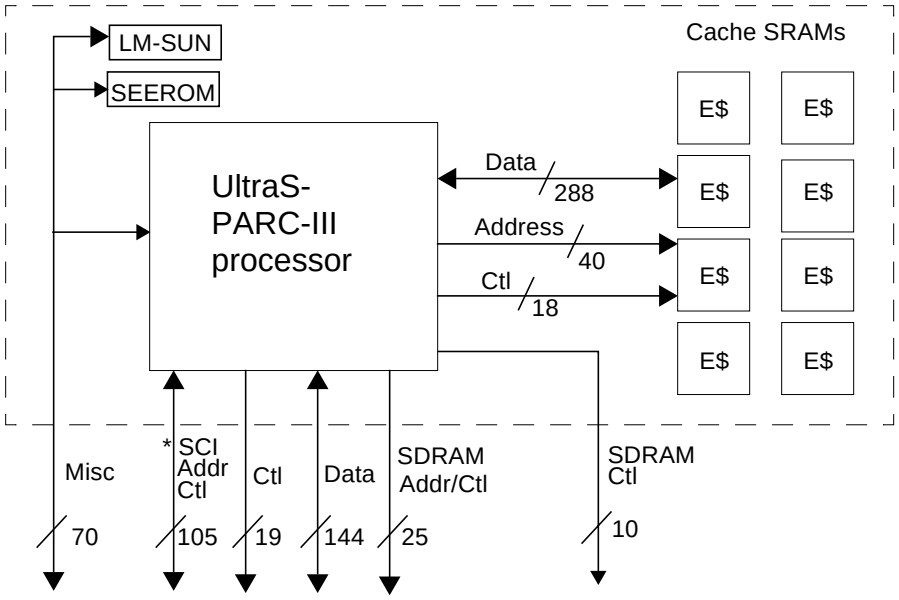


FIGURE C-2 UltraSPARC-III Processor Functional Block Diagram

The base CPU module frequency is 600 MHz. The system also supports faster processor speeds up to 1050 MHz in 150 MHz increments.

Note – The two UltraSPARC-III (CPUs) do not need to run at the same frequency.

Each CPU module plugs vertically into the motherboard through a set of two connectors. Each module is equipped with a mechanical insertion/extraction mechanism.

*Sun CrossBar Interconnect

The processors are interconnected through the Sun CrossBar Interconnect bus but the CPU module(s) only support the Sun CrossBar Interconnect address and command signals. The Sun CrossBar Interconnect address and control signals along with the data signals and the switch control signals, are routed through the module connectors.

The Ultra SPARC-III processors directly supports the main memory SDRAM. The memory controller is on the same die as the processor. The address and control signals for the SDRAM chips originate at the CPU chip pins and are routed to the motherboard through the module connectors.

The CPU module(s) contain serial EEPROMs for self-identification at boot time. The SEEPROM is interfaced through the I2C bus and provides the version of the CPU module, the size and speed of the external cache, the maximum internal frequency of the processor, and other operating parameters.

Thermal management relies on high air flow and a large heat sink radiation area to maintain uniform temperature control for the CPU module(s). The temperature of the CPU module(s) is monitored to avoid any destructive effect in case of fan failure. The CPU die contains a temperature sensing diode that is connected to a temperature controller located off of the die. This temperature controller performs the analog-to-digital temperature conversion and is interfaced through the I2C serial bus.

C.1.3 Main Memory

C.1.3.1 Organization

As shown on FIGURE C-1 on page C-3, direct access to the system main memory is controlled only by one of the two CPU modules in a multiprocessor environment. Memory is accessed from UltraSPARC Processor 0 through the Sun CrossBar Interconnect bus.

The main memory data bus is 576 bits wide which corresponds to an external cache block of 64 bytes. The systems main memory delivers an entire block of information on external cache in a single memory bus cycle. This delivery method provides up to 2.4 GBps of sustainable bandwidth.

The main memory is implemented with x144 DIMMs, also referred to as NG-DIMMs (next generation dual-in line memory modules). The system supports up to eight installed NG-DIMMs.

Note – The memory bus is clocked at half the system frequency through a clock connected directly to the CPU module.

The DIMMs also support a SEEPROM for identifying and configuring subsystem memory.

The CPU module memory controller performs reads and writes in blocks of 64 bytes. On noncacheable reads the extraneous data is dropped. On noncacheable write, the processor must perform a read-modify-write. The memory space is cached.

The memory subsystem supports logical interleaving by 1 (no interleaving), 2, and 4. The unit of interleaving is a logical bank. A group of four DIMMs corresponds to two logical banks for interleaving purposes. The interleaving is based on multiples of 64 bytes. Main memory interleaving is described in more details in Section C.1.3.3 “Interleaving” on page C-8.

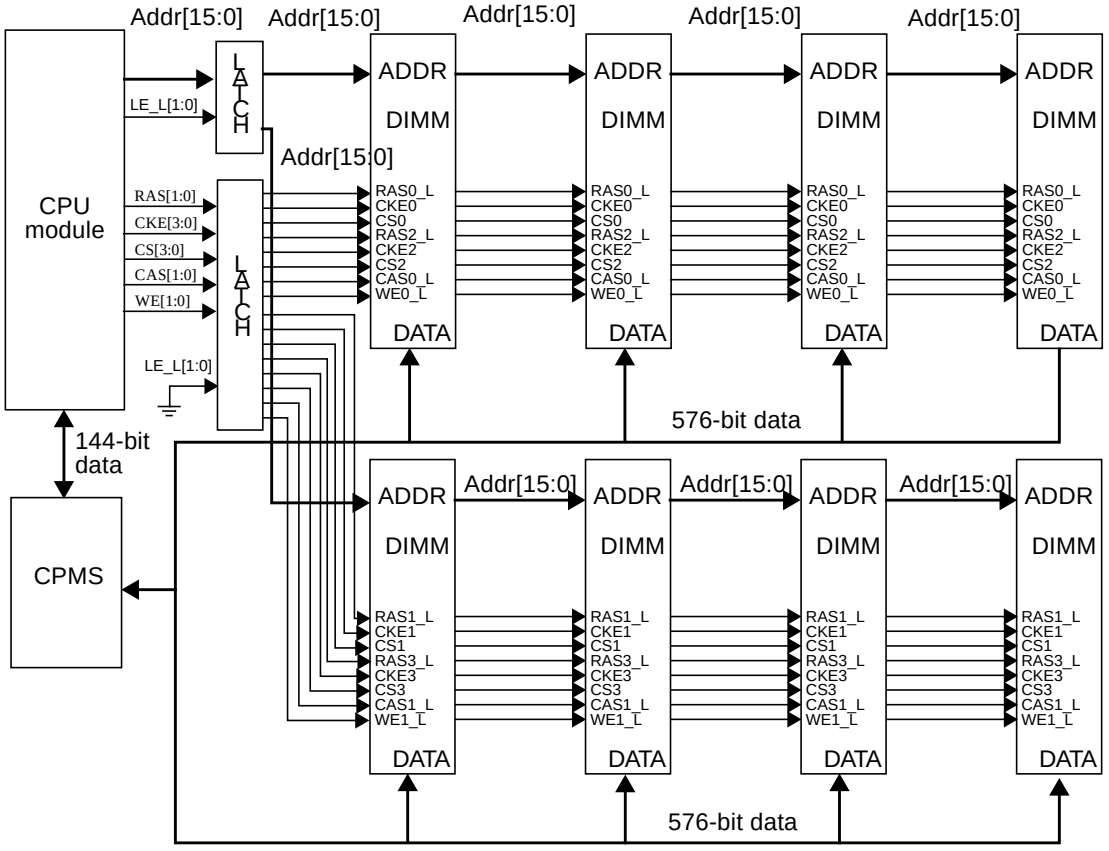


FIGURE C-3 Main Memory Functional Block Diagram

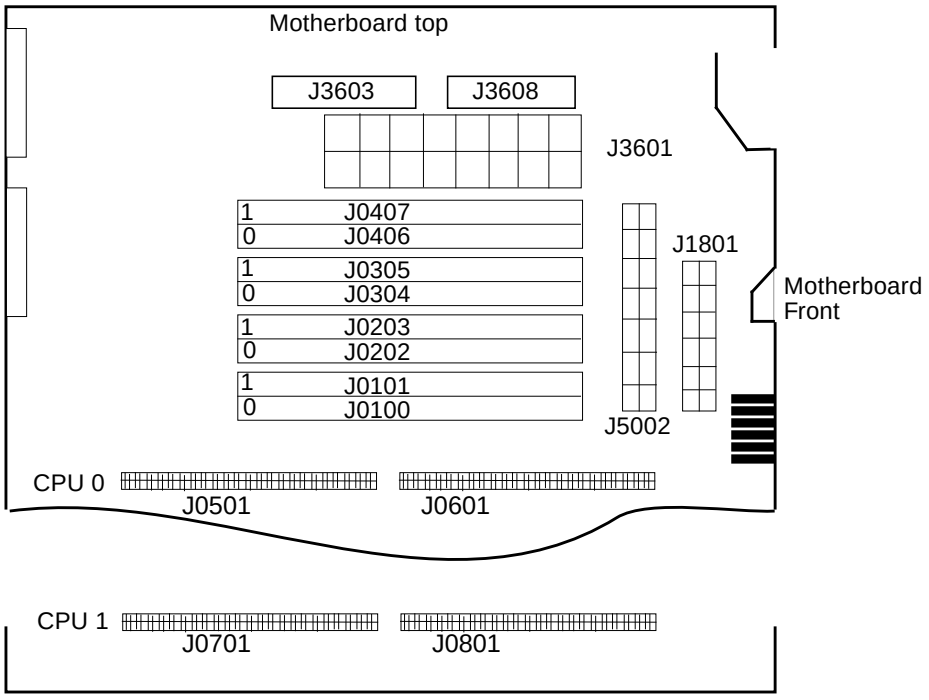


FIGURE C-4 DIMM Mapping

C.1.3.2 Memory Configuration

The following table describes various DIMMs supported by the system memory controller.

TABLE C-1 DIMMs Committed

DIMM Size	SDRAM device	Number of Logical Banks	Number of Devices	Group Size / Minimum Memory
128 Mbyte	64 Mbit (4 Mbyte x 16)	2	18	512 Mbyte
256 Mbyte	256 Mbit (16 Mbyte x 16)	2	18	1 Gbyte
1024 Mbyte	256 Mbit (2x 16 Mbyte x 8)	2	36 (stacked technology)	4 Gbyte

Main memory is populated with one or two groups of DIMMs. The following table lists the possible memory configurations.

Note – The banks in the following table are logical banks for interleaving purposes.

TABLE C-2 Memory Sizes Supported

First Group	No second group	2nd Group: 512 Mbyte	2nd Group:1 Gbyte	2nd Group: 4 Gbyte
512 Mbyte	512 Mbyte, 2 banks	1 GB, 4 banks	1.5 GB, 2banks	4.5 GB, 2 banks
1 GB	1GB, 2 banks	1.5 GB, 2 banks	4 GB, 4 banks	5 GB, 2 banks
4 GB	4 GB, 2 banks	4 GB, 2 banks	5 GB, 2 banks	8 GB, 4 banks

C.1.3.3 Interleaving

The main memory supports interleaving on 64-byte boundaries. The Sun Blade 1000 memory system supports from one to four logical banks. The DIMMs support one or two banks. For interleaving purposes, all banks are treated identically regardless of their physical location. Two successive accesses to distinct logical banks located in the same group of DIMMs are processed the same as accesses to logical banks that are in separate groups of DIMMs.

The memory controller for the Sun Blade 1000 system supports 2-way and 4-way interleaving.

The main memory is accessed only on 64-byte block reads or writes. The interleaving is based on a 64-byte addressing and the four low-order bits of a block physical address (PA[9:6]) determine the bank within a memory segment. The stride on which banks are interleaved is 64 bytes (no interleaving), 128 bytes (2-way interleaving), 256 bytes (4-way interleaving).

In only one configuration is it possible to interleave by four. Both groups must be populated with DIMMs of the same size supporting two banks.

C.1.3.4 Memory Timing

The CPU module memory controller is programmable so that different SDRAM speeds can be accommodated at different system clock frequencies and different processor clock ratios. The memory bus timing is controlled by a set of four memory timing control registers.

Memory Timing Values

The timing values for a given configuration depend on the following factors:

- Speed of the SDRAM

  The frequency of the SDRAM chip is indicated in the serial ID EEPROM on each DIMM. When two groups of 4 DIMMs are present, the SDRAM speed is considered the speed of the slowest SDRAM chip in the group.

- DIMM Implementation

  The implementation of the DIMM influences the timing parameters, in the same way that the traces on the DIMM board define the memory bus topology. The DIMM also supports a buffer for the address and control signals. The serial ID PROM identifies the DIMM and by default defines a given implementation.

- System clock frequency (Sun CrossBar Interconnect frequency)

  The memory bus clock generated by the CPU module is half the system clock frequency. The timing parameters are relative to this clock.

- System implementation

  The memory subsystem implementation also defines the timing parameters. The term “implementation” refers to the motherboard and all the chips that are part of the memory bus. A given implementation of a Sun Blade 1000 system, defines a set of timing parameters.

- Processor clock ratio

  The UltraSPARC III module is running at the clock speed which is a multiple x4, x5, or x6 of the system clock. Timing parameters are defined in terms of processor clocks, which means the processor frequency must be adjusted before programming the memory timing control registers.

C.1.4 I/O Subsystem

The I/O subsystem is designed around two bridge ASICs; SBC and PCIO-2. SBC is the bridge between the Sun CrossBar Interconnect bus, UPA64S and the two PCI buses. PCIO-2 is the bridge between the 33MHz PCI bus and USB, IEEE 1394, 10/100-Mbit Ethernet, and EBus.

C.1.4.1 SBC ASIC

The SBC ASIC supports the full Sun CrossBar Interconnect protocol. The CPU module interface to the 288-bit Sun CrossBar Interconnect data bus is through a 144-bit private data bus at 150 MHz for a maximum bandwidth of 2.4 Gbyte/sec.

SBC is composed of a Sun CrossBar Interconnect interface block and three leaf blocks:

- PCI A leaf block
- PCI B leaf block
- UPA64S leaf block

The following figure depicts the microarchitecture of the SBC ASIC:

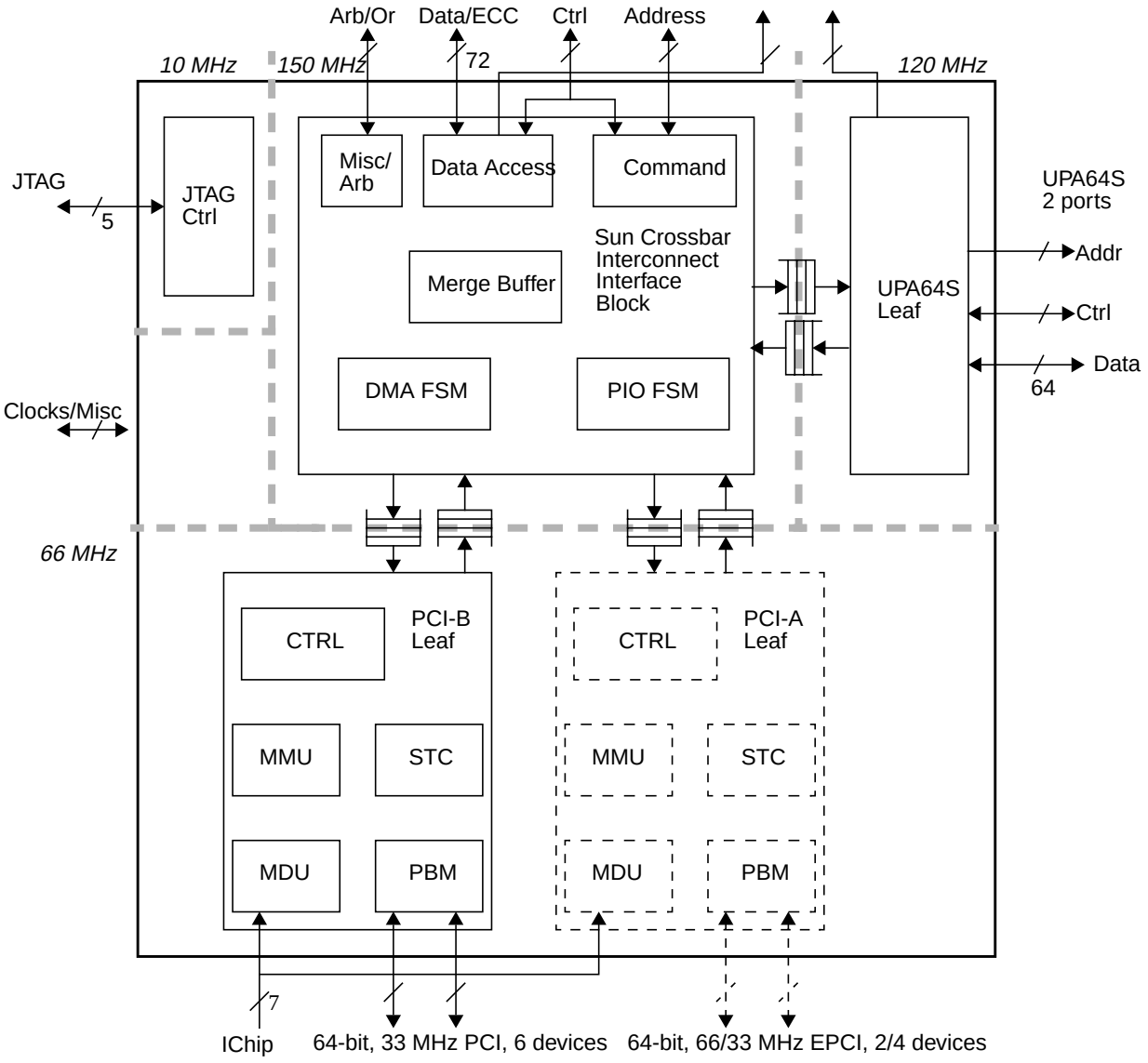


FIGURE C-5 SBC Block Diagram

The internal interface between the Sun CrossBar Interconnect interface block and the leaf blocks is fully asynchronous. This allows the frequency of Sun CrossBar Interconnect and UPA64S to be tuned according to the limitations of the system. There is no relative frequency limitation, and the frequency of a leaf can be higher than the Sun CrossBar Interconnect frequency.

UPA64S Leaf Block

The UPA64S leaf supports a slave-only UPA (UltraSPARC Port Architecture) bus segment that supports two slave graphics devices. The SBC receives PIOs (programmed I/Os) from the Sun CrossBar Interconnect interconnect and issues them onto the UPA64S bus. The data is routed from the CPMS to the Sun CrossBar Interconnect interface block, and finally to the UPA64S bus through the UPA leaf.

The UPA64S leaf is designed to sustain a stream of write PIOs at 120 MHz. This translates to a sustained bandwidth of 800 MByte/sec.

The Sun Blade 1000 supports a separate clock synthesizer for the UPA64S bus which is clocked at 120 MHz. See Section C.1.7 “UPA” on page C-18 for details.

EPCI A Leaf Block

The extended PCI (EPCI) is the 64-bit, 66 MHz PCI. The PCI A leaf is the host controller for the EPCI. It supports 3.3 V signalling only.

The PCI A leaf can support four master devices. The Sun Blade 1000 system only includes two: the EPCI slot and the FC-AL disk controller.

The microarchitecture of both PCI leaves is almost identical and the PCI A leaf also supports the logic blocks mentioned above to comply with the Sun4u/Sun5 architecture.

The EPCI high-bandwidth pluggable I/O interface sustains up to 500 Mbps in streaming DVMA mode. See Section C.1.8 “PCI Bus” on page C-18 for details.

PCI B Leaf Block

The term *PCI* refers to the 33 MHz PCI bus (PCI specification revision 2.1). The PCI B leaf is the host controller for the 64-bit wide/33 MHz PCI bus. It supports both 5 V and 3.3 V signalling, and 32-bit devices.

The PCI B leaf supports six master devices. The Sun Blade 1000 system includes only five devices: PCIO-2, three slots, and the 876 SCSI controller.

C.1.4.2 PCIO-2

The PCIO-2 contains a multi-function PCI interface and four leaves for each of the supported interfaces: Ethernet (10/100 Mbit), USB, IEEE 1394, and EBus. The figure below is a block diagram of the PCIO-2 ASIC:

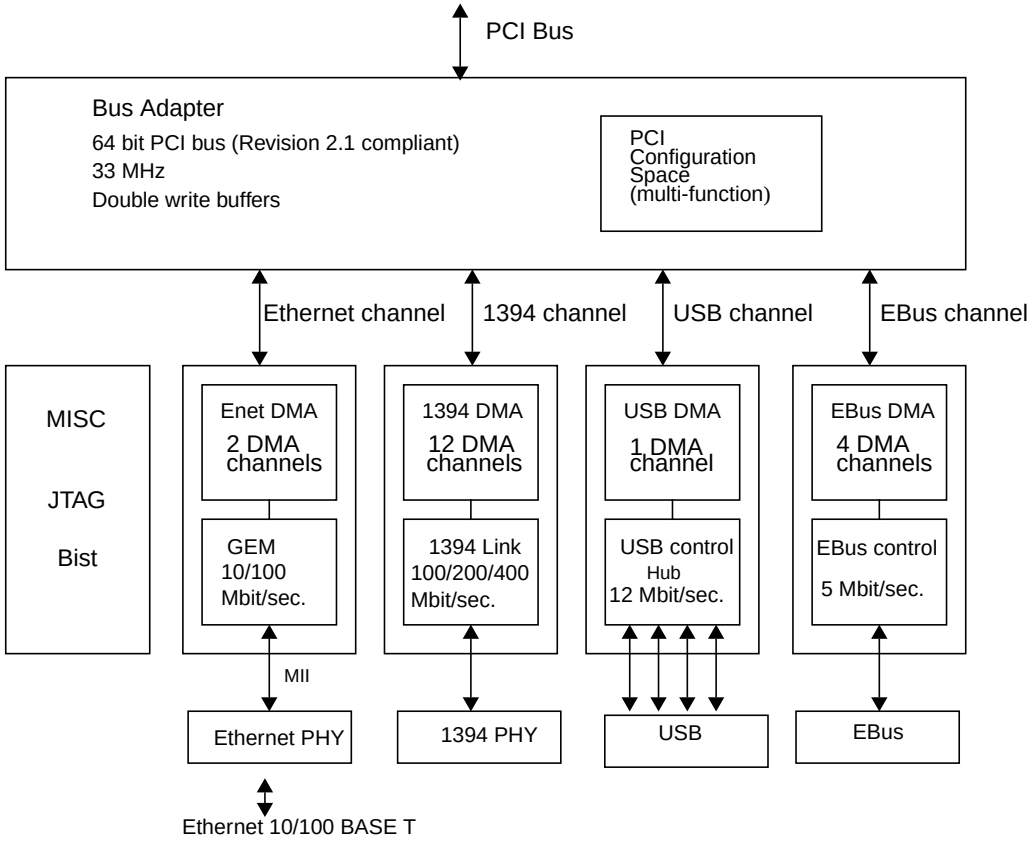


FIGURE C-6 PCIO-2 Block Diagram

PCI Interface

The PCI-B interface is 64-bit wide at 33 MHz. It supports slave (for PIO) and master (for DMA) transactions on the PCI bus. Master transactions use 256-byte burst transfers.

Note – The byte burst rate is programmable and can vary.

The PCIO-2 is a multi-function PCI device as defined by the PCI specification, and it supports a separate configuration space for each of the 4 interfaces. See Section C.1.8 “PCI Bus” on page C-18 for details.

Ethernet Leaf

The Ethernet interface supports two DMA channels for full duplex. the PCIO-2 Ethernet interfaces through PHY 6612 and COMBO magnetics and RJ45 connector. See Section C.1.14 “Ethernet” on page C-27 for details.

USB Leaf

USB (Universal Serial Bus) is a standard defined for the PC industry that provides connectivity to low-cost low-bandwidth peripherals.

USB defines a tree topology through hub devices although logically it behaves as a bus. The USB standard defines two data transfer rates: 1.5 and 12 Mbit/sec. USB supports live connect and disconnect of devices (hot-plugging).

The PCIO-2 USB channel engine has a single DMA engine with 1 K bit of internal buffering. It is the USB host controller and a hub with 4 ports. As a host controller it manages control flow, data flow and connections. The PCIO-2 USB host controller programming model is Open HCI compatible.

The Sun Blade 1000 system uses USB primarily to interface to the Sun Type-6 USB keyboard and mouse. The Type-6 USB keyboard does not include a hub and the mouse is also connected directly to a backpanel USB connector.

IEEE 1394 Leaf

IEEE 1394 is a high-performance serial bus designed for real-time data transfers supporting an isochronous transfer mode. In this mode bandwidth is guaranteed through pre-assignment.

In the Sun Blade 1000 system, IEEE 1394 is the interface for multimedia devices like digital cameras, digital video recorders, digital video/versatile disks (DVD).

IEEE 1394 is a very flexible interconnect that supports multi-master, live connect/disconnect, and dynamic node allocation. IEEE 1394 is based on a memory type addressing (geographical addressing). Each node also acts as a repeater and devices can be connected in a tree fashion.

IEEE 1394 is an IEEE standard. The IEEE 1394 trade association web site is

`http://www.1394ta.org/index.htm`.

The PCIO-2 IEEE 1394 interface supports 100, 200, and 400 Mbps transfers. The IEEE 1394 block contains six DMA engines: four for isochronous transfers and two for asynchronous transfers. The engine implements the industry standard Descriptor Based DMA Architecture (Open HCI). the PCIO-2 also implements the link layer and it interfaces directly to a PHY chip.

The Sun Blade 1000 system uses a PHY with four ports, two are used by the system. There are two IEEE 1394 connectors on the back panel.

C.1.4.3 EBus Leaf

EBus is a byte-wide I/O bus that provides the ability to interface to instruction set architecture devices. In a Sun Blade 1000 system there are five devices on this bus: the boot PROM (Flash memory), the audio module, the serial line controller, the SuperI/O chip, and the I2C controller.

The TOD clock function is implemented by the real time clock inside the SuperI/O ASIC. The nonvolatile RAM is implemented by a I2C serial EEPROM and part of the boot PROM.

The EBus channel engine also supports four DMA controllers with programmable transfer size and chained and unchained mode. Only two devices support slave DMA transfers on EBus: SuperI/O for the floppy disk interface (single DMA engine) and the parallel port (single DMA engine), and the audio CODEC for audio playback and capture (two DMA engines).

C.1.5 Interrupts

The interrupt model in an Sun Blade 1000 system follows the Sun4u/Sun5 architecture. Interrupts are delivered to the processor(s) as Mondo vectors. The CPU receives interrupt packets that are issued over the Sun CrossBar Interconnect bus. The processors can issue interrupts to each other (called cross-calls). They are issued by SBC for I/O interrupts. All interrupts that are not cross-called are referred to as I/O interrupts.

I/O interrupts are issued on separate lines by the various on-board devices, the PCI cards, and UPA cards. The interrupts are routed to an interrupt concentrator: the I-chip that encodes the interrupts and delivers them to the SBC. The SBC issues a single Sun CrossBar Interconnect interrupt transaction for each active interrupt.

The following diagram depicts the overall interrupt organization in the Sun Blade 1000 system:

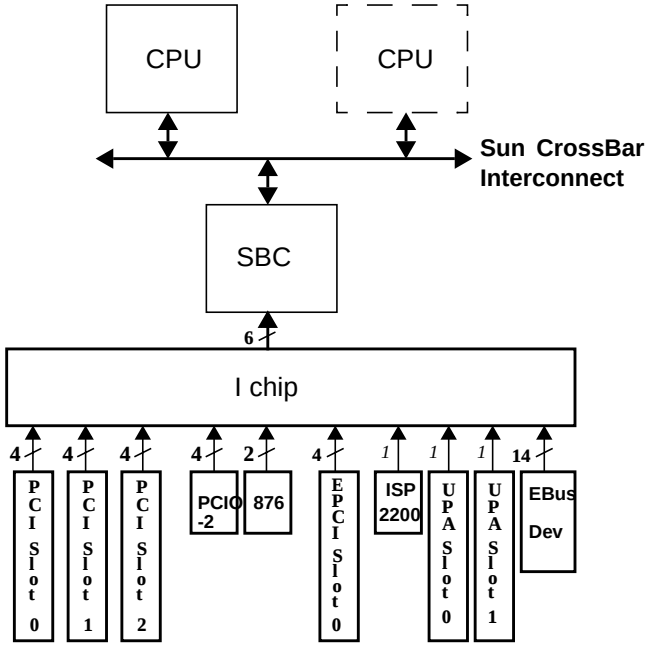


FIGURE C-7 Sun Blade 1000 System Interrupt Block Diagram

C.1.6 BootBus

The CPU modules support an alternate 8-bit bus (the BootBus) used after a reset to fetch the first instruction they execute.

The address space of the BootBus corresponds to the boot PROM addressing space as defined by the Sun4u/Sun5 architecture. The CPU issues its SPARC V9 RED_MODE trap vectors from this address space.

The following block diagram shows how the CPUs access the boot PROM through the BootBus, the BBC, and EBus:

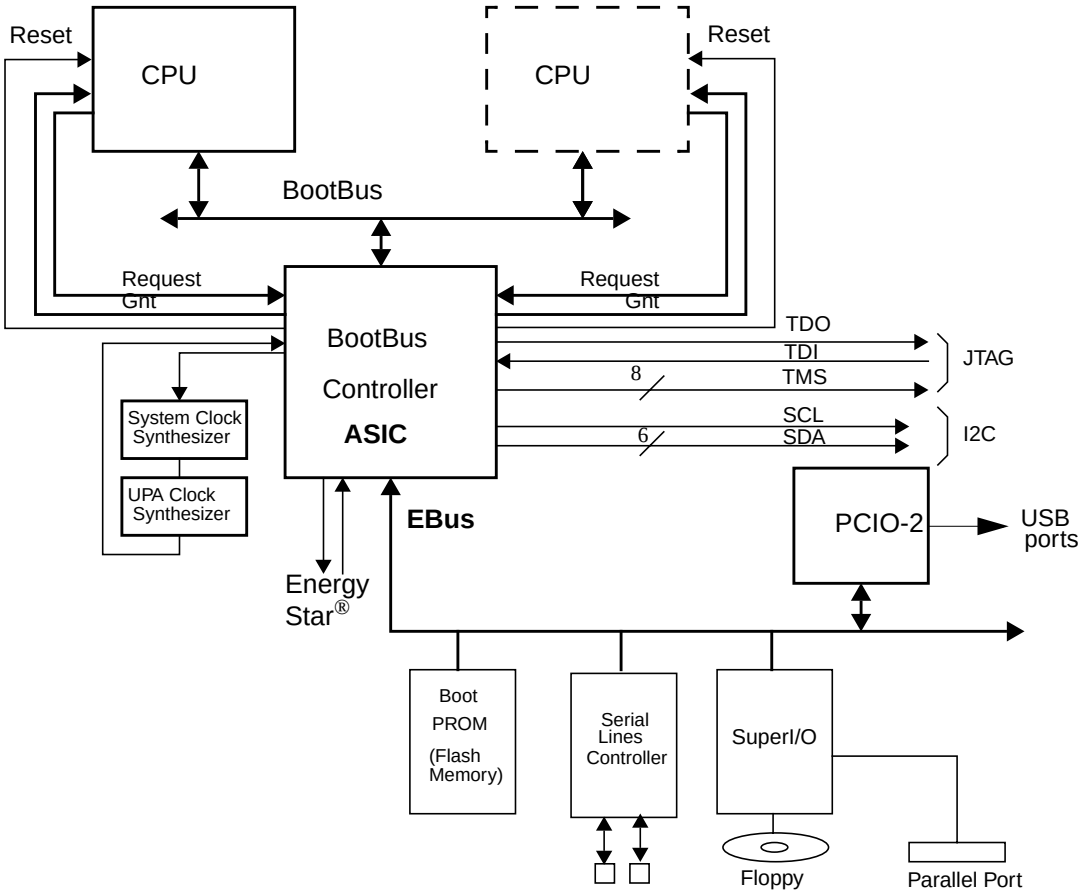


FIGURE C-8 Sun Blade 1000 Boot Structure

C.1.6.1 BootBus Controller (BBC) ASIC

The BootBus controller provides access to the boot PROM by bridging the Sun CrossBar Interconnect BootGroup signals (the BootBus) and the EBus. The boot PROM connects directly to the EBus.

The PCIO-2 is also a master on EBus. Full arbitration between the PCIO-2 and the BBC controls access to the EBus. The EBus is accessed from the BBC only during the boot sequence that is, during the execution of POST and OpenBoot PROM.

Note – When the system is running Solaris software, the kernel has no knowledge of the BootBus space.

Access to the boot PROM through the BBC is optimized for 16-byte master accesses performed by the CPU on the BootBus.

BBC is also a slave on EBus and all its internal registers are accessible through the PCIO-2. Thus software drivers running on Solaris software can access the necessary resources such as the Energy Star® software and the thermal management driver.

BBC also supports many other functions that are briefly introduced in the following subsections.

- Reset Controller

  The BBC is the reset controller in the Sun Blade 1000 system. The controller receives the reset source lines and is responsible for generating the reset signals for the CPU module(s) and the overall system. The external sources for reset include the Power Up reset from the power supply, the reset buttons on the motherboard, the SuperI/O watchdog timer, and fatal error conditions.

  The reset controller also includes registers that a processor uses to generate an external reset to itself or another processor.

- JTAG Controller

  BBC is the host for the JTAG+ controller that includes a programmable master tap controller. This allows processors to access the JTAG scan rings in the system by simply executing programmed I/O operations to the BBC master tap controller registers. The processor(s) can access the internal scan chain of all the ASICs and perform different levels of testing (boundary scan, internal scan for ATPG, RAM tests, and BIST if available).

  The JTAG+ controller allows for an external JTAG master to be connected to the motherboard for controlling all scan rings including the processor(s) scan ring(s) and the BBC internal scan ring.

- I2C Buses

  The BBC supports five master I2C buses and a single multi-master I2C bus.

  Small I2C serial EEPROMs make it possible to identify pluggable modules that cannot be identified easily through their regular data path. The DIMMs include an I2C serial EEPROM that contains information relative to the size and the speed of the DRAM. The CPU modules include an I2C EEPROM which indicates the size of the second level cache and the speed of the processor.

  Sensors on the CPU modules provide temperature data that is read through an analog-to-digital converter with an I2C interface.

  I2C is also used in the Sun Blade 1000 system for a smart card reader interface.

  The motherboard contains a socketed I2C EEPROM that contains system specific information such as the Ethernet address. This EEPROM can be transferred to a replacement motherboard. Another I2C EEPROM contains system info for a diagnostic log.

- Clock Synthesizers

  The BBC ASIC supports another serial interface to access the clock synthesizers. Synthesizers allow frequency margining on the system clock and the UPA64S clock frequency.

  After a power-on reset, the clock frequency for the system is set at a default low frequency (100 MHz). The multiplier in the CPU modules also are set at their lower value. The POST/OpenBoot PROM software determines the optimal system frequency by reading the I2C EEPROMs on the module and the motherboard. The POST/OpenBoot PROM software programs the new multiplier values in the CPU processors and adjusts the frequency of the synthesizers. A subsequent reset will activate the new multiplier values inside the processors.

Note – The Sun Blade 1000 system can accommodate two processors running at different speeds.

- Miscellaneous functions

  The BBC also supports the following functions:
  - Scratch pad memory (2 Kilobytes organized in 256 registers of 64 bits)
  - Energy Star protocol on the Sun CrossBar Interconnect bus

C.1.7 UPA

The UltraSPARC port architecture (UPA) provides a packet-based interconnect between the System Bus Controller (SBC) ASIC and the graphics cards.

C.1.8 PCI Bus

The peripheral component interconnect (PCI) bus is a 32-bit or 64-bit bus with multiplexed address and data lines. The PCI bus provides electrical interconnect between highly integrated peripheral controller components, peripheral add-on devices, and the processor/memory system.

There are two PCI buses in the Sun Blade 1000 system. The first bus is a one-slot, 3.3-VDC, 64-bit or 32-bit, 66-MHz or 33-MHz bus. The second bus is a three-slot, 5.0-VDC, 64-bit or 32-bit, 33-MHz bus. Both buses are controlled by the SBC ASIC. There are two on-board PCI devices, the SCSI controller and the PCIO-2 ASIC, on the 33-MHz PCI bus. The ISP2200A FC-AL disk controller is located on the 64-bit 66-MHz PCI bus.

C.1.8.1 PCI Cards

PCI cards come in a variety of configurations. Not all cards fit or operate in all PCI slots, so it is important to know the specifications of your PCI cards and the types of cards supported by each PCI slot in the system.

Some PCI cards are as short as 6.875 inches (17.46 cm) in length (called “short” cards), while the maximum length of PCI cards is 12.28 inches (31.19 cm, called “long” cards). Each slot in the Sun Blade 1000 system can accommodate either a long or a short card.

Older PCI cards communicate over 32-bit PCI buses, while many newer cards communicate over wider 64-bit buses.

Older PCI cards operate at 5 VDC, while newer cards are designed to operate at 3.3 VDC. Cards that require 5 volts will not operate in 3.3-volt slots, and 3.3-volt cards will not operate in 5-volt slots. “Universal” PCI cards are designed to operate on either 3.3 volts or 5 volts, so these cards can be inserted into either type of slot. The system provides three slots for 5-volt cards and one slot for a 3.3-volt card. All four PCI slots accept universal cards.

Most PCI cards operate at clock speeds of 33 MHz, while some newer cards (EPCI) operate at 66 MHz. All four PCI slots can accept 33-MHz cards.

Note – Installing a 33 MHz card into a 66 MHz EPCI will slow system performance.

66-MHz cards are restricted to the slot labelled EPCI 1. The following table lists the mapping of the PCI slots to the two PCI buses, and the type of PCI cards supported in each slot.

TABLE C-3 PCI Slot-to-PCI Bus Mapping

Connector Label	Conn. No.	PCI Bus	Slot Width (bits)/ Card Type (bits)	Clock Rates (MHz)	DC Voltage (VDC)/ Card Type
PCI 4	J2601	B	64/32 or 64	33	5/universal
PCI 3	J2501	B	64/32 or 64	33	5/universal
PCI 2	J2401	B	64/32 or 64	33	5/universal
PCI 66 1	J2301	A	64/32 or 64	66	3.3/64-bit

C.1.8.2 PCI Bus ASICs

SCSI Controller

The SCSI controller ASIC provides an interface between the 33-MHz, PCI bus and the internal and external SCSI buses. The dual SCSI bus controller provides separate connections to internal and external devices. SCSI channel A is used for internal devices and supports the SCSI fast and narrow mode. SCSI channel B is used for external devices and supports the SCSI ultra-wide mode.

FC-AL Disk Controller

The FC-AL disk controller ASIC provides an interface between the 64-bit, 66-MHz PCI bus, the two FC-AL hard drives, and an external FC-AL connector. The FC-AL controller provides connection to internal and external devices through one channel. The FC-AL loop supports up to 125 devices. See Section C.1.16 “FC-AL Subsystem” on page C-30.

C.1.9 Peripherals

The following peripherals are supported by the Sun Blade 1000 system:

C.1.9.1 DVD-ROM and Tape Drives

The DVD-ROM, and back-up devices (tape drive) are interfaced through a SCSI controller. The Sun Blade 1000 system uses a SCSI host controller on the PCI bus. This controller is used only in fast narrow mode.

Note – The DVD-ROM drive is factory set to SCSI target ID 6. Refer to the installation documentation for the DVD-ROM to change the target ID address.

C.1.9.2 Diskette Drive

The system uses a standard 1.44-Mbyte diskette drive that is 1 inch (25.40 mm) high. Refer to the *Manual Eject Diskette Drive Specifications*, part number 805-1133, for diskette information, panel descriptions, and drive specifications.

Note – The diskette drive is factory set to target address 0. Refer to the *Manual Eject Diskette Drive Specifications*, part number 805-1133, to change the target address.

SuperI/O Diskette Drive Interface

The SuperI/O ASIC contains an onboard diskette drive controller with a 16-byte first-in-first-out (FIFO) memory buffers that support burst and non-burst modes. The diskette drive controller handles data rates of 500 Kbps and 250 Kbps. See Section C.1.12 “Diskette Drive and Parallel Ports” on page C-23 for details.

C.1.9.3 Hard Drives

The system supports two internal FC-AL hard drives. Each hard drive has a single connector configuration. A drive bracket is used to mount the drives. The following table lists the hard drive features of some of the Sun Blade 1000 drives.

TABLE C-4 Internal Hard Drive Features

Form Factor Dimension	Hard Drive Capacity	RPM	Seek Time(read/write) (average)
1.00-inch (2.54-cm)	18 Gbytes	10K	7.5 msec / 8.5 msec
1.0 inch (2.54 cm)	36 GBytes	10K	7.5 msec / 8.5 msec

The *18 Gbyte 10K RPM Disk Drive Specifications*, part number 806-1057, provides installation instructions, power requirements, and performance data for the 18-Gbyte 10K RPM hard drive.

C.1.9.4 Smart Card Reader

The smart card reader is attached to the I2C bus.

C.1.10 Other Peripheral Assembly Options

The system supports other peripheral assembly options that can be installed in the system. These options can include the DVD-ROM drive and tape drives.

C.1.11 Keyboard and Mouse

The keyboard and mouse port USB interface is managed by the PCIO-2 ASIC. FIGURE C-9 shows the keyboard and mouse port interface functionality.

C.1.11.1 Keyboard and Mouse Port

The keyboard and mouse are connected to the USB connectors, located on the motherboard. Keyboard current is limited to 700 milliamperes (mA) by a resettable fuse.

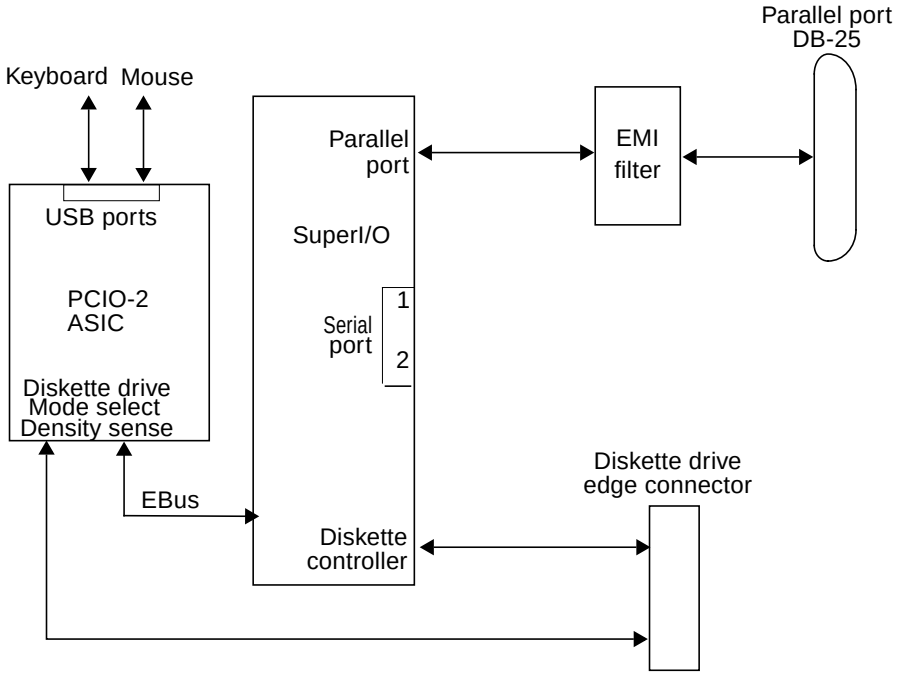


FIGURE C-9 Keyboard and Mouse, Diskette, and Parallel Port Functional Block Diagram

C.1.12 Diskette Drive and Parallel Ports

The diskette drive and parallel port are managed by the SuperI/O component.

C.1.12.1 Diskette Port

The diskette port is supported by a diskette controller, located on the SuperI/O ASIC. The diskette controller is software compatible with the DP8473, DP765A, and the N82077 diskette controllers. The SuperI/O ASIC is compatible with perpendicular recording drives (2.88-Mbyte formatted diskettes) and standard diskette drives. The diskette controller handles data rates of 2 Mbit/sec, 1 Mbit/sec, 500 Kbits/sec, and 250 Kbit/sec.

Two extra pins on the SuperI/O ASIC support all Sun standard diskette drives, including diskette drives using Density_Select and Density_Sense pins and diskette drives using a Disk_Change signal. It is DMA driven via a DMA channel in the EBus interface of the PCIO ASIC. Manual eject diskette drives (IDs of 0 or 1, respectively) are supported.

Power is supplied to the diskette drive from a separate power connector. The diskette drive operates from the 5 VDC supply and draws a maximum power of 1.1 watts operating and 44 milliwatts in standby mode.

C.1.12.2 Parallel Port

The parallel port is supported by an IEEE 1284-compliant parallel port controller located on the SuperI/O ASIC. The parallel port controller is a PC industry-standard controller that achieves a 2-Mbits/sec. (Mbps) data transfer rate. The parallel port controller interface supports the ECP protocol as well as the following:

- Centronics—Provides a widely accepted parallel port interface.
- Compatibility—Provides an asynchronous, byte-wide forward (host to peripheral) channel with data and status lines used according to their original definitions.
- Nibble mode—Provides an asynchronous, reverse (peripheral-to-host) channel, under control of the host. Data bytes are transmitted as two sequential, four-bit nibbles using four peripheral-to-host status lines.

Parallel Port Cables

The parallel port cable is IEEE 1284-compliant and consists of 18 pairs of signal wires that are double shielded with braid and foil. The maximum length of the parallel port cable is 2.2 yards (2 meters).

Electrical Characteristics

Drivers operate at nominal 5 VDC TTL levels. The maximum open circuit voltage is 5.5 VDC and the minimum is -0.5 VDC. A logic high-level signal is at least 2.4 VDC at a source current of 0.32 mA, and a logic low-level signal is no more than 0.4 VDC at a sink current of 14 mA.

Receivers also operate at nominal 5-VDC TTL levels and can withstand peak voltage transients between -2 VDC and 7 VDC without damage or improper operation. The high-level threshold is less than or equal to 2.0 VDC and the low-level threshold is at least 0.8 VDC. Sink current is less than or equal to 0.32 mA at 2.0 VDC, and source current is less than or equal to 12 mA at 0.8 VDC.

C.1.13 Serial Port

The system incorporates two serial ports. Each serial port is synchronous and asynchronous with full modem controls. All serial port functions are controlled by a serial port controller that is electrically connected to the system through the EBus. Line drivers and line receivers control the serial port signal levels and provide RS-232 and RS-423 compatibility. Each serial port interfaces through its own DB-25 connector.

The major features of each serial port include:

- Two fully functional synchronous and asynchronous serial ports
- DB-25 connectors
- Increased baud rate (to 384 Kbaud synchronous, 460.8 Kbaud asynchronous)
- Variable edge rate for greater performance
- EBus interface

The following figure shows a functional block diagram of the serial port:

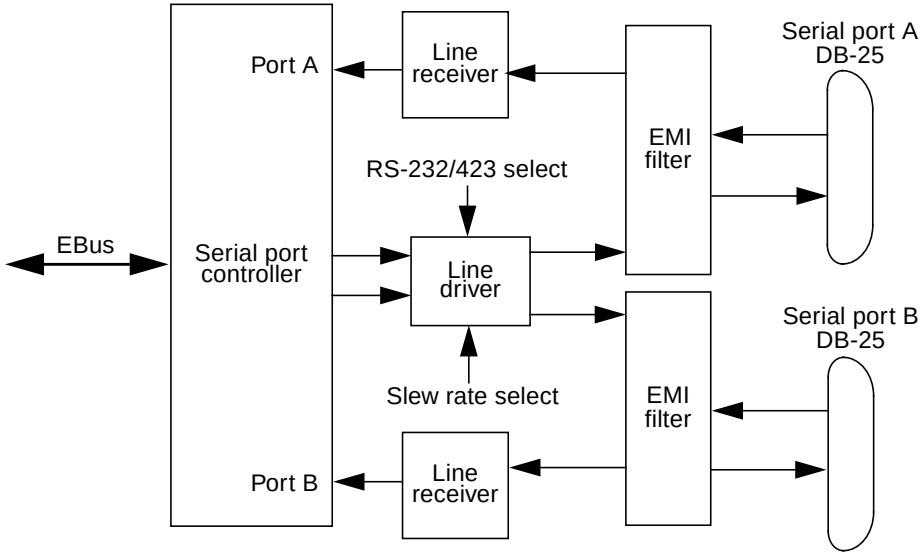


FIGURE C-10 Serial Port Functional Block Diagram

C.1.13.1 Serial Port Components

Serial port components include a serial port controller, line drivers, and receivers.

The serial port controller contains sixty-four-byte input and output buffers that are used to reduce the CPU bandwidth requirements of the serial port controller.

Note – Interrupts are generated when the buffer reaches 32 bytes or half full.

The line drivers and line receivers are compatible with both RS-232 and RS-423 protocols. Software control sets the line drivers and line receivers to either RS-232 or RS-423 protocols. The line driver slew rate is also programmable. For baud rates over 100 Kbaud, the slew rate is set to 10 VDC/µsec. For baud rates under 100 Kbaud, the slew rate is set to 5 VDC/µsec.

C.1.13.2 Serial Port Functions

Modem connection to the serial port allows access to the Internet. Synchronous X.25 modems are used for telecommunications in Europe. An ASCII text window is accessible through the serial port on non-graphic systems. Low speed printers, buttonboxes (for CAD/CAM applications), and devices that function like a mouse

are also accessible through the serial port. The additional speed of the serial port can be used to execute communications with a CSU/DSU for a partial T1 line to the Internet at 384 Kbaud.

C.1.13.3 EIA Levels

Each serial port supports both RS-232 and RS-423 protocols. RS-232 signaling levels are between -3 VDC and -15 VDC and +3 VDC and +15 VDC. A binary 1 (001_2) is anything greater than +3 VDC and a binary 0 (000_2) is anything less than -3 VDC. The signal is undefined in the transition area between -3 VDC and +3 VDC. The line driver switches at -10 VDC and +10 VDC with a maximum of -12 VDC and +12 VDC in RS-232 mode. RS-423 support is similar except that signaling levels are between -4 VDC to -6 VDC and +4 VDC and +6 VDC. The line driver switches at -5.3 VDC and +5.3 VDC with a maximum of -6 V and +6 VDC.

The preferred signaling protocol is RS-423. The higher voltages of RS-232 makes it more difficult to switch at the higher baud rates. The maximum rate for RS-232 is approximately 64 Kbaud while the maximum rate for RS-423 is 460.8 Kbaud. The system default is set to RS-232.

C.1.13.4 Synchronous Rates

The serial synchronous ports operate at any rate from 50 Kbaud to 256 Kbaud when the clock is generated from the serial port controller. When the clock is generated from an external source, the synchronous ports operate at up to 384 Kbaud. Clock generation is accurate within 1 percent for any rate that is generated between 50 Kbaud and 256 Kbaud.

C.1.13.5 Asynchronous Rates

The serial asynchronous ports support twenty baud rates that are all exact divisors of the crystal frequency (with the exception of 110, which is off by less than 1 percent). Baud rates include 50, 75, 110, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200, 38400, 57600, 76800, 115200, 153600, 230400, 307200, and 460800.

C.1.13.6 Slew Rate and Cable Length

The maximum RS-423 cable length is 118 feet (30 meters) and the maximum RS-232 cable length is 50 feet (15.24 meters). The slew rate changes depending on the speed. For speeds less than 100 Kbaud, the slew rate is set at 5 VDC per microsecond. For

rates greater than 100 Kbaud, the slew rate is increased to 10 VDC per microsecond. This allows maximum performance for the greater baud rates and better signal quality at the lesser baud rates.

C.1.14 Ethernet

The system supports 10-Mbps, 10BASE T; twisted-pair Ethernet; and 100-Mbps, 100BASE T. Twisted-pair Ethernet is provided through an 8-pin RJ45 connector. The Ethernet circuitry design is based on a Lucent PHY.

The PHY chip integrates a 100BASE-T physical coding sub-layer (PCS) and a complete 10BASE-T module in a single chip.

The 100BASE-X portion of the PHY IC consists of the following functional blocks:

- Transmitter
- Receiver
- Clock generation module
- Clock recovery module

The 10BASE-T section of the PHY IC consists of the 10-Mbps transceiver module with filters.

The 100BASE-X and 10BASE-T sections share the following functional characteristics:

- PCS control
- IEEE 802.3u auto negotiation

The following sections provide brief descriptions of the following:

- Automatic negotiation
- Connectors

C.1.14.1 Automatic Negotiation

Automatic negotiation controls the cable when a connection is established to a network device. It detects the various modes that exist in the linked partner and advertises its own abilities to automatically configure the highest performance mode of inter-operation, namely, 10BASE-T, 100BASE-TX, or 100BASE-T4 in half- and full-duplex modes.

The Ethernet port supports automatic negotiation. At power up, an on-board transceiver advertises 100BASE-TX in half-duplex mode, which is configured by the automatic negotiation to the highest common denominator based on the linked partner.

C.1.14.2 External Cables

The RJ-45 Ethernet port supports a Category 5, UTP cable for the 100BASE-T, and a Category 3, 4, or 5 UTP cable for the 10BASE-T operation.

Note – The maximum cable segment lengths for the 100BASE-TX and 10BASE-TX are 109 yards (100 meters) and 1094 yards (1000 meters), respectively.

C.1.15 Audio Card and Connector

An audio card provides various audio applications from telephone-quality speech to CD-quality music. The audio card supports four jacks of identical type: line in, line out, headphone out, and microphone in. The following table lists the major features of the audio card and the following figure illustrates a functional block diagram.

TABLE C-5 Audio Card Features

Figure Reference	Feature	Description
1	Stereo line level	Attenuated by a resistor divider network and then fed into the line inputs of the CODEC.
2	Stereo microphone input	Buffered by a non inverting operational amplifier (one operational amplifier for the left channel and one operational amplifier for the right channel). The left and right outputs are then fed into the left and right Mic. Inputs of the CODEC. A filtered +5 VDC signal is fed to the signal inputs.
3	CODEC mono-output	Fed into an active graphic equalizer to add bass boost and mid-range attenuation. Equalizer output is amplified and routed to the front mounted 16-ohm, 68-mm speaker.
4	Line output	A direct output, except E1, which enables muting of this signal. The mute function is driven from the codec PIO lines.
5	Headphone output	Buffered by an operational amplifier to give headphone drive with low impedances of 16 ohms or more. The output of the headphone out is independently mutable, driven from codec PIO lines.
6	Multimedia CODEC (MMCODEC)	Heart of the audio module. A single-chip, stereo, A/D and D/A converter based on delta-sigma conversion.

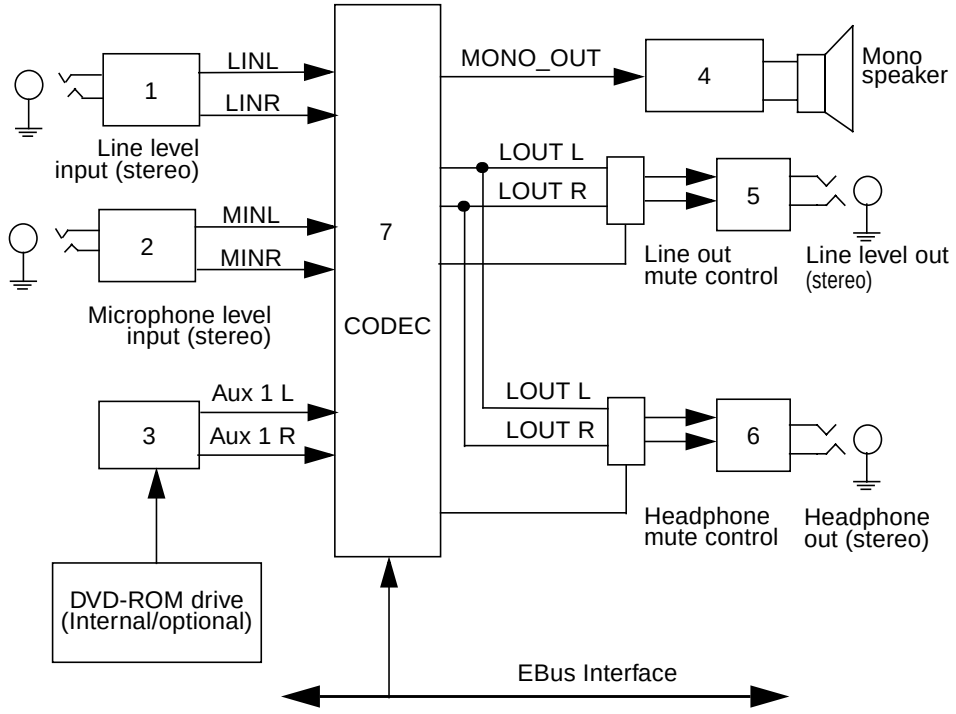


FIGURE C-11 Audio Card Functional Block Diagram

The audio card connector is a dual-position, standard-edge connector whose features include:

- 23 dual positions (46 total)
- 50-millimeter centerline
- 1.49 inches (total length)

The audio connector supports the following:

- Nine CODEC address lines
- Eight CODEC data lines
- Control lines write, read, codec chip select, PROM chip select, reset
- CODEC DMA support signals: playback request, playback acknowledge, capture request, and capture acknowledge
- CODEC power down line
- Audio analog lines DC volume control line
- Audio present
- Power / ground two +12 VDC lines, one -12 VDC line, one voltage at the common collector (VCC) line, five digital grounds, and four analog grounds
- Two spare pins

C.1.16 FC-AL Subsystem

The Sun Blade 1000 system supports FC-AL (Fibre Channel-Arbitrated Loop) as the interface for internal and external hard drives. The physical medium is copper. Optical links are not supported.

The disk drives are connected to the loop through a hub chip. The hub supports two internal connectors and the external connector. Internal signal detect circuitry automatically detects the presence of a device at the external connector which enables or disables the external port. The individual ports can also be bypassed manually by a software probe and programming a GPIO register in the FC-AL controller.

TABLE C-6 ISP2200A GPIO Bits

ISP2200A GPIO Bits	Drive Control	Input/Output Type	Default/Reset Value
<0>	External drive	Output	1*
<1>	Internal drive 1	Output	1*
<2>	Internal drive 2	Output	1*
<3>	External port detect	Input	0**
			**0 means bypass *1 means enable

The FC-AL host controller ASIC has a 64-bit, 66 MHz PCI (EPCI) interface. The controller contains the serializer / deserializer (SERDES) and the transceivers on-chip. The host controller implements the Fibre Channel protocol through a microcoded engine. The memory for the firmware is external and is implemented with synchronous 128 Kilobyte SRAM. This memory also keeps the context data for outstanding I / Os.

The figure below shows the Sun Blade 1000 disk subsystem architecture:

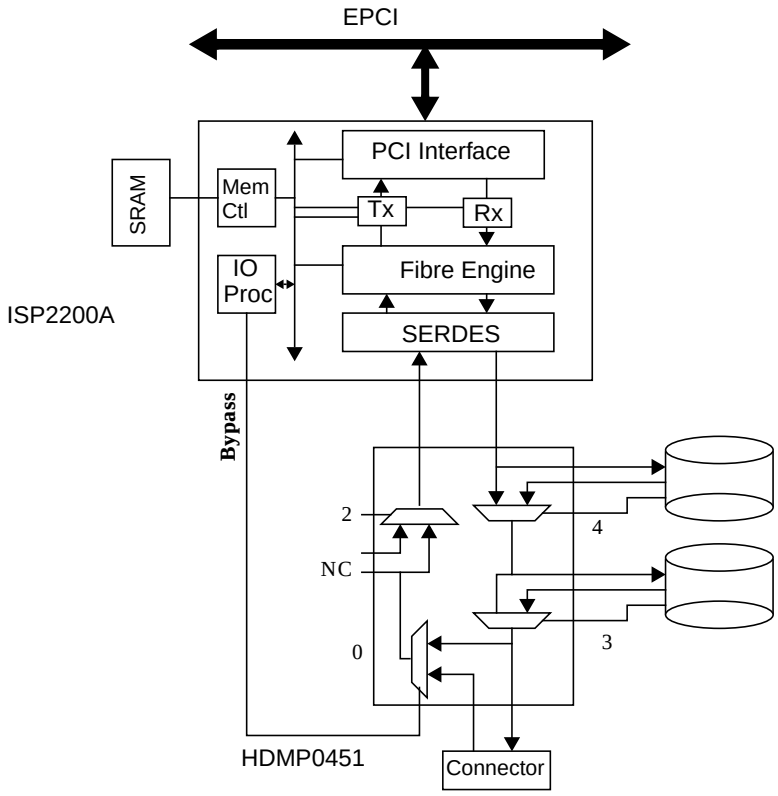


FIGURE C-12 Sun Blade 1000 FC-AL Disk subsystem

C.1.17 SCSI

The system implements a small computer system interface (SCSI) for Ultra SCSI, 40 Mbps parallel interface bus. Ultra SCSI provides the following:

- Efficient peer-to-peer I/O bus devices
- Mechanical, electrical, and timing specification definition that support transfer rates of 20 or 40 Mbytes/sec./ (corresponding to the data path width of an 8-bit, or 16-bit bus, respectively)
- Peak bandwidth of 40 Mbytes/sec./ (with implemented 16-bit bus width)

The internal SCSI bus is terminated at each end. One set of terminators is located close to the DVD-ROM drive connector on the DVD-ROM SCSI cable. A second set of terminators is located close to the internal SCSI connector. The following figure shows the SCSI bus configuration.

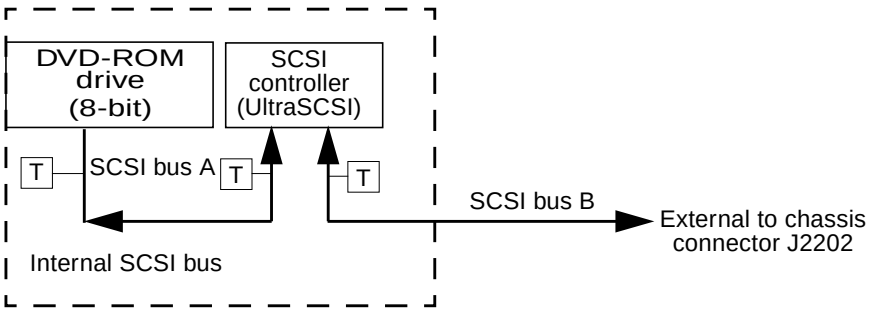


FIGURE C-13 Configuration for the SCSI Bus

C.1.17.1 Host Adapter

The host adapter is a QLogic PCI-SCSI ASIC. The host adapter and all target devices comply with the Ultra SCSI single-ended drivers and receivers characteristics. The electrical characteristics of the output buffers include:

- V_{ol} (output low) equals 0 to 0.5 VDC with Iol at 48 mA (signal asserted)
- V_{oh} (out high) equals 2.5 to 3.7 VDC (signal negated)
- t_{rise} (rising slew rate) equals 520 mV per nanosecond maximum (0.7 to 2.3 VDC)
- t_{fall} (falling slew rate) equals 520 mV per nanosecond maximum (2.3 to 0.7 VDC)

The Ultra SCSI electrical characteristics for the host adapter and target device include:

- V_{il} (input low) equals 1.0 VDC maximum (signal true)
- V_{ih} (input high) equals 1.9 VDC minimum (signal false)
- I_{il} (input low current) equals +/- 20 µA at V_i equals 0.5 VDC
- I_{ih} (input high current) equals +/- 20 µA at V_i equals 2.7 VDC
- Minimum input hysteresis equals 0.3 VDC

C.1.17.2 Supported Target Devices

The SCSI subsystem supports a maximum of three internal devices, including the host adapter, DVD-ROM drive and tape drive. The external SCSI bus supports up to 16 Ultra Wide SCSI devices.

C.1.17.3 External Cables

External Ultra SCSI-compliant SCSI cables have an impedance of 90 ohm (+/- 6 ohms) and are required for Ultra SCSI interface. The Sun implementation of Ultra SCSI requires that the total SCSI bus length be limited to no more than approximately 20 feet (6 meters) with up to 12 Sun compensated devices.

Due to the considerably short bus length, two Ultra SCSI-compliant external cables are supported, a 32-inch (0.8-meter) and 6.5-foot (2-meter).

Note – Consult your authorized Sun sales representative or service provider to order Ultra SCSI-compliant external cables.

There is also an external SCSI connector on the backpanel for legacy peripheral devices.

C.1.18 SuperI/O

The Sun Blade 1000 system uses a SuperI/O ASIC to interface to the diskette drive and the parallel port. The SuperI/O ASIC also:

- Provides the TOD/ID SEEPROM
- Interfaces with the power supply

C.2 Power Supply

The 670-watt autosensing power supply has a voltage range of 90 to 264 volts root-mean-square (VRMS) with a frequency range of 47 to 63 Hz. The maximum input current is 12 amps at 100 volts.

The power supply output voltages are listed in the following table. The power supply continues to regulate all outputs for 10 milliseconds after AC power is removed.

TABLE C-7 Power Supply Output Values for the Sun Blade 1000

Output	Voltage (VDC)	Max Current (A)	Regulation Band (V)
1	3.3	90.0	3.23 to 3.43
2	5.0	70.0	4.85 to 5.25
3	12.0	8.0	11.65 to 12.60
4	-12.0	0.4	-12.60 to -11.40
5	5.0_Standby	1.5	4.75 to 5.25

Note – The combined power of output 1 and output 2 must be less than 600 watts.

C.2.1 Control Signals

All power supply control signals are at signal levels shown in table C-8.

TABLE C-8 Power Supply Control Signal Levels

Parameter	Min	Max
V_{OH} (high-level output voltage)	3.4 VDC	
V_{OL} (low-level output voltage)		0.4 VDC
V_{IH} (high-level input voltage)	2.4 VDC	
V_{IL} (low-level input voltage)		0.8 VDC

C.2.1.1 Remote Enable Power On

A remote interface can enable the DC outputs with a low signal to the Power On input. This signal is applied to the power supply from the motherboard.

C.3 Motherboard

FIGURE C-14 shows a block diagram of the Sun Blade 1000 motherboard. TABLE C-9 describes the functions of the connectors and jumpers.

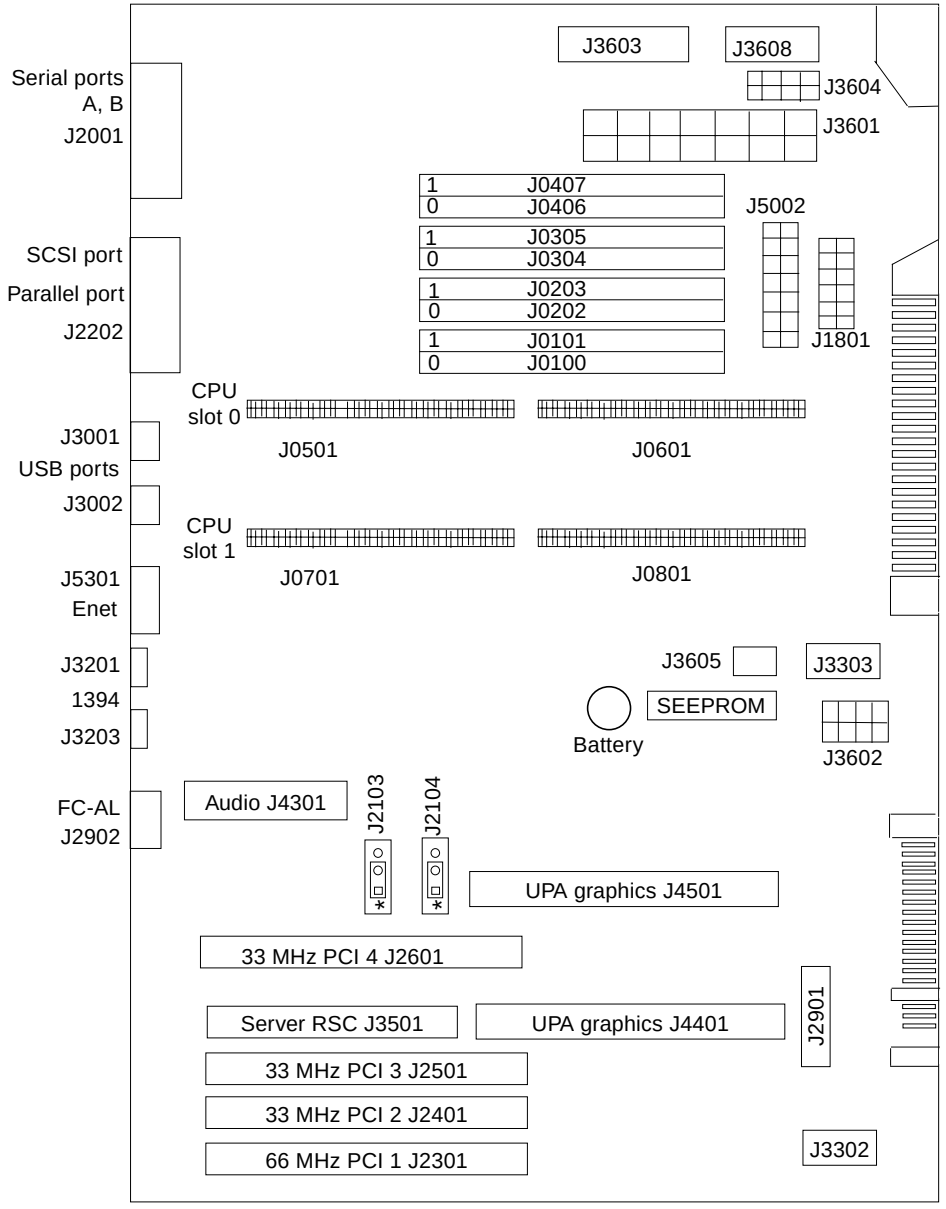


FIGURE C-14 System Motherboard Block Diagram

TABLE C-9 Motherboard Component Functions

Designation	Function
J0100	DIMM
J0101	DIMM
J0202	DIMM
J0203	DIMM
J0304	DIMM
J0305	DIMM
J0406	DIMM
J0407	DIMM
J0501	CPU connector
J0601	CPU connector
J0701	CPU connector
J0801	CPU connector
J1801	Diskette drive data connector
J2001	Serial ports A, B rear panel connector
J2103	Jumper PROM R/W See Section C.4 “Jumper Descriptions” on page C-38
J2104	Jumper PROM Select See Section C.4 “Jumper Descriptions” on page C-38
J2202	SCSI, Parallel rear panel connector
J2301	66 MHz PCI 1 connector
J2401	33 MHz PCI 2 connector
J2501	33 MHz PCI 3 connector
J2601	33 MHz PCI 4 connector
J2901	FC-AL internal connector
J2902	FC-AL rear panel connector
J3001	USB rear panel connector
J3002	USB rear panel connector
J3201	IEEE 1394 rear panel connector
J3203	IEEE 1394 rear panel connector

TABLE C-9 Motherboard Component Functions

Designation	Function
J3302	Lower fan power connector
J3303	Upper fan power connector
J3501	Server RSC connector
J3601	Power supply connector
J3602	Combined cable connector
J3603	Power supply connector
J3604	Smart card reader connector
J3605	Go-glow connector
J3608	Peripheral power cable connector
J4301	Audio card connector
J4401	UPA board connector
J4501	UPA board connector
J5002	SCSI connector
J5301	Ethernet rear panel connector

C.4 Jumper Descriptions

Jumper configurations can be changed from the default settings by setting jumper switches on the motherboard.

A jumper switch is *closed* (sometimes referred to as *shorted*) with the plastic cap inserted over two pins of the jumper. A jumper is *open* with the plastic cap inserted over one or no pin(s) of the jumper.

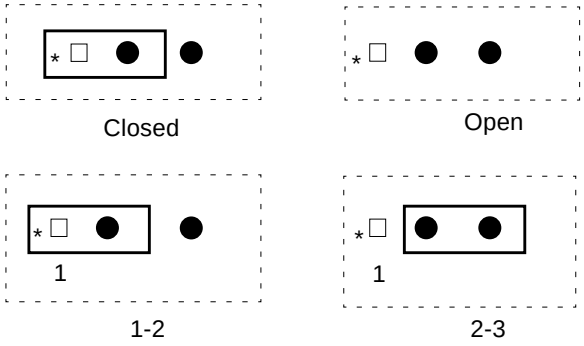


FIGURE C-15 Selected Jumper Settings

Jumper descriptions include brief overviews of flash PROM jumpers and additional system board jumper and connector blocks.

Jumpers are identified on the system board by J designations. Jumper pins are located immediately adjacent to the J designator. Pin 1 is marked with an asterisk in any of the positions shown in the figure below.

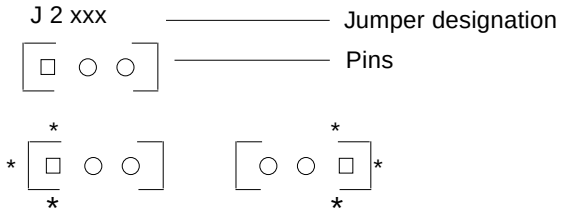


FIGURE C-16 Identifying Jumper Pins

C.4.1 Flash PROM Jumpers

Flash PROM jumpers J2103 and J2104 are for reprogramming specific code blocks and remote programming of the flash PROM. The following figure shows the flash PROM jumper locations.

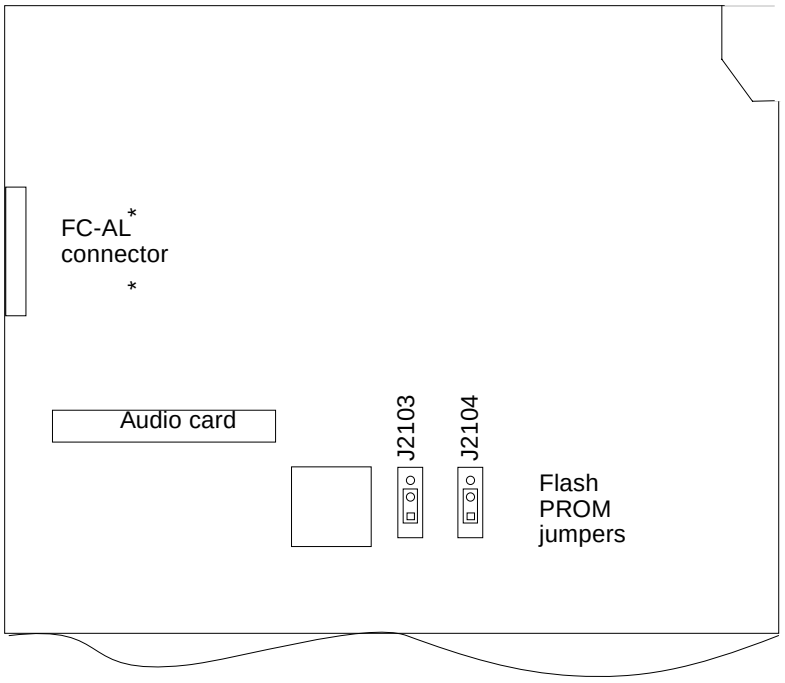


FIGURE C-17 Flash PROM Jumper Locations

TABLE C-10 Flash PROM Jumper Settings

Jumper	Pins 1 + 2 Select	Pins 2 +3 Select	Default Jumper on Pins	Signal Controlled
J2103	Write protect	Write enable	1 + 2	FLASH PROM PROG ENABLE
J2104	Select	No select	1 + 2	XOR LOGIC SET

C.5 Enclosure

The Sun Blade 1000 enclosure allows for desktop, or under-desk installation. The enclosure design complies with all necessary environmental and regulatory specifications.

C.5.1 Enclosure Basics

Overall dimensions of the enclosure are 10.0 inches x 24.4 inches x 17.8 inches (255mm x 620 mm x 452 mm). The enclosure houses:

- One 1.0-inch diskette drive or a second 1.6-inch device
- One 1.6-inch DVD-ROM or tape drive
- One 1.0-inch device slot for the smart card reader

Note – The DVD-ROM drive slot is used for an optional DVD-ROM drive or tape drive.

- Two 1-inch or 1.6-inch single-connector 3.5-inch hard drives
- Two plug-in UltraSPARC-III modules
- Eight DIMMs
- Four PCI slots
- Two UPA64S modules

C.5.2 Enclosure Features

Enclosure features include:

- Access for internal upgrades and service
- Optimized system board layout
- Graphics expansion module (UPA64S connector)
- Processor placed on plug-in module expediting upgrades
- All standard connectors and no splitter cables on rear panel

C.6 Power Management

The objective of the Environmental Protection Agency's Energy Star program is to reduce power consumption levels of electrical devices to save energy. The Energy Star specification for computers requires that after 15-30 minutes of inactivity the reduced power level be less than 15% of the maximum rated output of the power supply. The approach adopted to meet the Energy Star requirement on the previous generation of desktop platforms is to preserve an image of the system on the disk drive for fast reboot, to do an orderly shut down and to finally turn off the system. Because the system being turned off is not visible on the network, all services (email, ftp, file sharing, remote administration) that depend on network connectivity are lost.

C.6.1 Subsystems Power Management

Power management of each subsystem is controlled by the Power Management™ software and is configured through a graphical user interface (GUI). The idle time before a subsystem is power managed, can be adjusted by the user. Subsystems may also be left at full power (infinite idle time) or forced into its low power mode (zero idle time).

The following are brief descriptions of the subsystems' power management behavior. Refer to the following sections for more details on each subsystem.

C.6.1.1 UltraSPARC-III Processor(s), Main Memory, and Sun CrossBar Interconnect

This subsystem corresponds to the core of the Sun Blade 1000 system and represents most of the system power budget. Power is saved in this subsystem by lowering the system clock frequency. The Power Management software manages the frequency shifts by monitoring idle and active time as reported by the operating system. When idle time, determined by what code is being executed, reaches a certain level by software, the system clock is transitioned to a lower frequency. This is done in two steps:

1. **First, the clock is cut to 1/2, then to 1/32 of the nominal frequency.**
2. **When CPU activity increases and the idle time decreases to a certain level, the frequency is shifted back to 1/2 then to full speed.**

The external cache also supports a sleep mode that is automatically activated when the system frequency is reduced and no access is active.

C.6.1.2 EPCI Bus

Devices that support the *PCI Bus Power Management Interface Specification* are put into sleep mode. If no device has the ability to request service through an interrupt or similar signal, the clock may be completely turned off to save more power.

C.6.1.3 Storage Devices

FC-AL (hard drives), and SCSI CD-ROM and DVD-ROM devices spin down when inactive.

C.6.1.4 Audio

The audio module is put into a stand-by mode by software when it is inactive. When an application accesses the audio subsystem, the audio module reactivates.

C.6.1.5 IEEE 1394 Bus

When software determines there is no activity on the IEEE 1394 bus and there is no need to provide power to any external devices, the power provided by the system to the cable is turned off. The PHY is still on so that it acts as a repeater although the Sun Blade 1000 system is logically off the IEEE 1394 bus. This would allow external devices to still communicate on the bus while the Sun Blade 1000 system is in low-power mode.

The IEEE 1394 interface must be awakened by software when an application desires to use the IEEE 1394 bus.

C.6.1.6 USB

USB framework power, manages all USB devices. If a USB device is inactive for a period of time, USB framework puts the device into low power mode. The device is again brought into full power mode by the USB framework when a user attempts to use a device or when an application on the host starts an input or output to or from the device. All HID (Human Interface Device) hub and storage devices (example: keyboard or mouse) are power managed by default if they support wakeup. Printers are power managed only between job outputs.

Note – Activity on the USB keyboard or mouse indicates user intervention, causing USB framework power to remove the system from low power mode.

APPENDIX **D**

USB Supplement

This appendix contains information on the following topics:

D.1 USB Keyboard and Mouse

The following USB Keyboard and Mouse information is provided for your Type-6 USB keyboard and USB mouse:

- The Sleep key on the USB keyboard behaves differently than the power key on Type-5 or Type-6 keyboards. On a USB keyboard, you can SUSPEND/SHUTDOWN the system using the sleep key, but you cannot power-on the system.
- If you are using a USB keyboard that is not from Sun, the functionality that you get with a left-side keypad is unavailable.

Note – The keys for the left-side keyboard are not present on the USB keyboard.

- Multiple keyboards are not supported. The keyboards enumerate and are usable but are not plumbed as a console keyboard.
- Multiple mice are not supported. The mice enumerate and are usable, but are not plumbed as console mouse.
- The first keyboard that gets probed at boot time becomes the console keyboard. This can potentially cause confusion to customers if there are multiple keyboards plugged in at boot time.
- The first mouse probed at boot time becomes console mouse. This can potentially cause confusion to customers if there are multiple mouse plugged in at boot time.

- If you have a 3rd-party composite keyboard with PS/2 mouse, and it is the first one to be probed, it will become the console keyboard/mouse even if the PS/2 mouse is not plugged in.

Note – Therefore if another USB mouse is plugged into the system it will not work because the second mouse is not configured as the console mouse.

- On a system with multiple USB keyboards, if you unplug the console keyboard, the next available USB keyboard does not become the console keyboard. The next hot plugged keyboard will become the console keyboard.
- On a system with more than one USB mouse, if you unplug the console mouse, the next available USB mouse doesn't become the console mouse. The next hot plugged mouse will become the console mouse.
- Only a 2 or 3 button mouse is supported. A wheel on wheel mouse acts like a plain button mouse. A mouse with more than 3 button functions like a 3 button mouse.

D.2 USB Power Management

USB power management is "leaf" first and then "bottoms-up". This means that all leaf devices go into low-power mode first. Following that, the bottom-most hub goes into low-power mode first, followed by hubs in the next upper level. This follows all the way to the top root hub.

Note – As a rule of thumb, the deeper the USB device tree, the poorer USB power management becomes.

D.2.1 Storage Devices

- Use `pcfs`(7fs) and `udfs`(7fs) with USB mass storage devices. These file systems are platform neutral and data can be easily shared between platforms. UFS is also supported, but requires syncing on panic. The driver currently supports syncing.
- Each mass storage device has a device node called "`disk`". Each node receives a unique controller number. A device with multiple LUNs will get the same controller number but different "`d`" number `(/dev/[r]dsk/cXtYdZsN)`
- On hot remove mass storage drives, `/dev/[r]dsk` links remain persistent. Type **`devfsadm -C`** to remove stale links.
- System Checkpoint/Resume will fail if a file system is mounted.

D.2.2 Printer Devices

- After plugging in the printer, type **`lpadmin`** or **`printmgr`** to configure printer
- To find out which of `/dev/printers/N` is a USB printer,
  - type **`ls -l`** on `/dev/`printers and find out which symbolic links point to the `usbprn` device.
- For Lexmark™ printers choose "HP" as printer type in printmgr

D.2.3 Hot Plug

- OBP at present doesn't support hot plug of USB devices. If a user removes the USB keyboard when the system is at the OK prompt, the system will become wedged. If the USB keyboard is plugged into the system again OBP will not recognize the keyboard. You will have to power cycle the system.
- As a general rule, no USB device should be hotplugged when the system is at the OK prompt in OBP and during booting of the system until a UNIX login prompt is displayed.
- Unplugging open or busy device will not remove the entries in the `prtconf` file. The system prompts to plug in the original device. To clear the `prtconf` entries, the original device needs to be plugged into the same port, the application terminated, and then the device removed. Until then, the port remains unusable.
- After plugging in a device, check `prtconf` or `/dev/usb` before hot removing.

D.2.4 Cabling

- Never use USB cable extenders that are available on the market. Always use a hub with longer cables to connect devices.
- Always use fully-rated (12Mbps) 20/28 AWG cables for connecting devices.

D.2.5 Devices Supported

- USB keyboard and mouse. Composite keyboards with PS/2 mouse.
- Hubs:4 & 7 port, either Bus or Self powered
- Printers:
  - Lexmark Optra E310, M410, T616, W810, Color45
  - Xerox DocuPrint N2125
- Storage:
  - Iomega Zip 100, Zip 250. See man page for `scsa2usb` for a complete list of devices supported

D.2.6 Man Pages Available

- `ohci`(7D),
- `uhci`(7D),
- `hubd`(7D),
- `usb_mid`(7D),
- `hid`(7D),
- `scsa2usb`(7D),
- `usbprn`(7D),
- `usbkb`(7M),
- `usbms`(7M)

Glossary

address (1) A number used by the system software to identify a storage location. (2) In networking, a unique code that identifies a node to the network.

ASIC Application-specific integrated circuit

Asynchronous An operation that is not synchronized with the timing of any other part of the system.

ASP Authorized service provider

BIST Built in self test

boot To load the system software into memory and start it running.

boot PROM In Sun workstations, the boot PROM contains a PROM monitor program, a command interpreter used for booting, resetting, low-level configuring, and simple testing.

CDE Common desktop environment

DIMM Dual in-line memory module. A small printed circuit card that contains dynamic random-access memory chips.

DMA Direct memory address

DRAM Dynamic random-access memory. Read / write dynamic memory in which the data can be read or written in approximately the same amount of time for any memory location.

DTAG Dual tag or data tag

DVD Digital Video Disk

EEPROM Electrically erasable programmable read only memory

EMI Electromagnetic interference. Electrical characteristic that directly or indirectly contributes to a degradation in performance of an electronic system.

EPCI Extended peripheral component interconnect, a 64bit, 66MHz PCI bus

Ethernet A type of local area network that enables real-time communication between network devices, connected directly together through cables. A widely implemented network from which the IEEE 802.3 standard for contention networks was developed, Ethernet uses a bus topology (configuration) and relies on the form of access known as CSMA/CD to regulate traffic on the main communication line. Network nodes are connected by coaxial cable (in either of two varieties) or by twisted-pair wiring. See also **10BASE-T**, and **100BASE-T**.

FC-AL Fiber channel arbitrated loop

FIFO First-in, first-out

flash PROM A type of programmable read-only memory (PROM) that can be reprogrammed by a voltage pulse. See also **PROM**.

Gbyte Gigabyte, 10^9 bytes

GUI Graphical user interface

I/O Input/output

JTAG An interface from the Boot Bus Controller that enables testing of the ASICs on the motherboard.

Kbyte Kilobyte, 10^3 bytes

Leaf Any node (location in a tree structure) that is farthest from the primary node.

LED Light-emitting diode

MBps Megabyte per second

Mbps Megabit per second

Mbyte Megabyte, one million bytes

MHz Megahertz

MII Media independent interface

Network A configuration of data processing devices and software connected together for information exchange.

NG-DIMM Next generation dual inline memory module

Node An addressable point on a network. Each node in a Sun network has a different name. A node can connect a computing system, a terminal, or various other peripheral devices to the network.

ns Nanosecond, 10^{-9} seconds

NVRAM Nonvolatile random-access memory. A type of RAM that retains information when power is removed from the system. In Sun systems, contains the system hostID number and Ethernet address.

OBP OpenBoot PROM. A routine that tests the network controller, diskette drive system, memory, cache, system clock, network monitoring, and control registers.

PCI bus Peripheral component interconnect bus. A high-performance 32 or 64 bit-wide bus with multiplexed address and data lines.

PCIO PCI-to-EBus/Ethernet controller. An ASIC that bridges the PCI bus to the EBus, enabling communication between the PCI bus and all miscellaneous I/O functions, as well as the connection to slower on-board functions.

Peripheral assembly Removable media assembly. Can include a Smart card reader, CD-ROM drive, DVD-ROM drive, 4-mm tape drive, a diskette drive, and any other 3.5-inch device.

PID Process ID

POR Power on reset

POST Power on self-test. A series of tests that verify that system board components are operating properly. Initialized at system power-on or when the system is rebooted

PROM Programmable Read-Only Memory. A type of read-only memory (ROM) that allows data to be written into the device with hardware device called a PROM programmer. After the PROM has been programmed, it is dedicated to that data and cannot be reprogrammed.

SCSI Small computer system interface.

SRAM Static random access memory

STP Shielded twisted-pair

Sun Crossbar Interconnect A high speed, wide data path, super computing architecture that allows independent and simultaneous connections between major system components.

SunVTS A diagnostic application designed to test hardware.

Synchronization The action of forcing certain points in the execution sequences of two or more asynchronous processes to coincide in time.

TIP A connection that enables a remote shell window to be used as a terminal to display test data from a system.

TPE Twisted-pair Ethernet

TOD Time of day. A timekeeping integrated circuit.

TTL Transistor-transistor logic

UPA UltraSPARC port architecture. Provides graphics interconnection.

UTP Unshielded twisted-pair

VCC Voltage at the common collector (positive [+] electrical connection).

VIS Visual instruction set

VRMS Volts root-mean-square

10BASE-T An evolution of Ethernet technology that succeeded 10BASE5 and 10BASE2 as the most popular method of physical network implementation. A 10BASE-T network has a data transfer rate of 10 megabits per second and uses unshielded twisted-pair wiring with RJ-45 modular telephone plugs and sockets.

100BASE-T Also known as Fast Ethernet, an Ethernet technology that supports a data transfer rate of 100 megabits per second over special grades of twisted-pair wiring. 100BASE-T uses the same protocol as 10BASE-T. There are three subsets of the 100BASE-T technology: 100BASE-TX defines digital transmission over two pairs of shielded twisted-pair wire. 100BASE-T4 defines digital transmission over four pairs of unshielded twisted-pair wire. 100BASE-TX defines digital transmission over fiber-optic cable.

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