Sun Ultra 10 Service Manual

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Contents

Preface xix

About the Multimedia Links in This Manual xix
How This Book Is Organized xx
Using UNIX Commands xxi
Typographic Conventions xxii
Shell Prompts xxii
Related Documents xxiii
Ordering Sun Documents xxiv
Sun Welcomes Your Comments xxiv

1. Product Description 1-1
   1.1 Feature Overview 1-2
   1.2 I/O Devices 1-3
   1.3 System Description 1-4
   1.4 Replaceable Components 1-6

2. SunVTS Overview 2-1
   2.1 SunVTS Description 2-1
      2.1.1 SunVTS Requirements 2-2
      2.1.2 SunVTS References 2-2
3. **Power-On Self-Test**  3-1
   3.1  POST Overview  3-1
   3.2  Pre-POST Preparation  3-2
      3.2.1  Setting Up a TIP Connection  3-2
      3.2.2  Verifying the Baud Rate  3-4
   3.3  Initializing POST  3-5
   3.4  Maximum and Minimum POST Levels  3-7
      3.4.1  diag-level Variable Set to max  3-7
      3.4.2  diag-level Variable Set to min  3-15
      3.4.3  POST Progress and Error Reporting  3-19
   3.5  Bypassing POST  3-22
   3.6  Resetting Variables to Default Settings  3-22
   3.7  Initializing Motherboard POST  3-23

4. **Troubleshooting Procedures**  4-1
   4.1  Power-On Failure  4-2
   4.2  Video Output Failure  4-3
   4.3  Hard Drive or CD-ROM Drive Failure  4-4
   4.4  Power Supply Test  4-5
   4.5  DIMM Failure  4-7
   4.6  OpenBoot PROM On-Board Diagnostics  4-8
      4.6.1  Watch-Clock Diagnostic  4-8
      4.6.2  Watch-Net and Watch-Net-All Diagnostics  4-8
      4.6.3  Probe-IDE Diagnostic  4-10
      4.6.4  Test device alias, device path, –All Diagnostic  4-10
      4.6.5  UPA Graphics Card  4-12
   4.7  OpenBoot Diagnostics  4-13
      4.7.1  Starting the OBDiag Menu  4-13
      4.7.2  OB Diagnostics  4-17
         4.7.2.1  PCI/PCIO Diagnostic  4-18
4.7.2.2  EBus DMA/TCR Registers Diagnostic  4-19
4.7.2.3  Ethernet Diagnostic  4-19
4.7.2.4  Keyboard Diagnostic  4-20
4.7.2.5  Mouse Diagnostic  4-21
4.7.2.6  Diskette Drive (Floppy) Diagnostic  4-21
4.7.2.7  Parallel Port Diagnostic  4-22
4.7.2.8  Serial Port A Diagnostic  4-22
4.7.2.9  Serial Port B Diagnostic  4-24
4.7.2.10 NVRAM Diagnostic  4-25
4.7.2.11 Audio Diagnostic  4-25
4.7.2.12 EIDE Diagnostic  4-26
4.7.2.13 Video Diagnostic  4-26
4.7.2.14 All Above Diagnostic  4-27

4.7.3  Exiting the OB Diag Menu  4-30

5.  Preparing for Component Replacement  5-1

5.8  Safety Requirements  5-2
5.9  Safety Symbols  5-2
5.10 Safety Precautions  5-3
  5.10.1 Modification to Equipment  5-3
  5.10.2 Placement of a Sun Product  5-3
  5.10.3 Power Cord Connection  5-3
  5.10.4 Electrostatic Discharge  5-4
  5.10.5 Lithium Battery  5-4
5.11 Tools Required  5-5
5.12 Powering Off the System  5-5
5.13 Removing the System Cover  5-8
5.14 Attaching the Wrist Strap  5-10
5.15 Removing a Filler Panel  5-11
6. Major Subassemblies 6-1

6.1 Power Supply 6-1
   6.1.1 Removing the Power Supply 6-1
   6.1.2 Replacing the Power Supply 6-3

6.2 Cable Assemblies 6-4
   6.2.1 Removing the Diskette Drive Cable Assembly 6-4
   6.2.2 Replacing the Diskette Drive Cable Assembly 6-6
   6.2.3 Removing the Hard Drive Cable Assembly 6-6
   6.2.4 Replacing the Hard Drive Cable Assembly 6-7
   6.2.5 Removing the Serial/Parallel Cable Assembly 6-8
   6.2.6 Replacing the Serial/Parallel Cable Assembly 6-9
   6.2.7 Removing the Audio Cable Assembly 6-9
   6.2.8 Replacing the Audio Cable Assembly 6-10

6.3 Speaker Assembly 6-11
   6.3.1 Removing the Speaker Assembly 6-11
   6.3.2 Replacing the Speaker Assembly 6-12

6.4 CPU Fan Assembly 6-13
   6.4.1 Removing the CPU Fan Assembly 6-13
   6.4.2 Replacing the CPU Fan Assembly 6-14

6.5 Front Bezel 6-15
   6.5.1 Removing the Front Bezel 6-15
   6.5.2 Replacing the Front Bezel 6-16

6.6 Rear Hard Drive Bracket 6-17
   6.6.1 Removing the Rear Hard Drive Bracket 6-17
   6.6.2 Replacing the Rear Hard Drive Bracket 6-19

7. Storage Devices 7-1

7.1 Diskette Drive 7-1
   7.1.1 Removing the Diskette Drive 7-1
   7.1.2 Replacing the Diskette Drive 7-2
7.2 Hard Drives    7-4
  7.2.1 Removing a Hard Drive    7-4
  7.2.2 Replacing a Hard Drive    7-6
  7.2.3 Hard Drive Mirroring    7-8
    7.2.3.1 Hard Drive Mirroring Configuration    7-8
    7.2.3.2 Hardware Considerations    7-8
    7.2.3.3 Required Software and Patches    7-9
    7.2.3.4 Software Constraints    7-10
    7.2.3.5 Recovery Procedure for Broken Database Replicas    7-11

7.3 CD-ROM Drive    7-13
  7.3.1 Removing a CD-ROM Drive    7-13
  7.3.2 Replacing a CD-ROM Drive    7-14

8. Motherboard and Component Replacement    8-1
  8.1 CPU Module    8-1
    8.1.1 Removing the CPU Module    8-1
    8.1.2 Replacing the CPU Module    8-3
  8.2 NVRAM/TOD    8-4
    8.2.1 Removing the NVRAM/TOD    8-4
    8.2.2 Replacing the NVRAM/TOD    8-5
  8.3 DIMM    8-6
    8.3.1 Removing a DIMM    8-6
    8.3.2 Replacing a DIMM    8-8
  8.4 Graphics Card    8-9
    8.4.1 Removing a Graphics Card    8-9
    8.4.2 Replacing a Graphics Card    8-10
    8.4.3 Elite3D m3 and Elite3D m6 UPA Graphics Card Patch Information    8-11
  8.5 PCI Card    8-12
    8.5.1 Removing a PCI Card    8-12
    8.5.2 Replacing a PCI Card    8-13
8.6 PCI Riser Board 8-15
  8.6.1 Removing the PCI Riser Board 8-15
  8.6.2 Replacing the PCI Riser Board 8-16
8.7 Motherboard 8-17
  8.7.1 Removing the Motherboard 8-17
  8.7.2 Replacing the Motherboard 8-19

9. Illustrated Parts List 9-1

10. Finishing Replacement Procedures 10-1
  10.1 Replacing the System Cover 10-1
  10.2 Powering On the System 10-3

A. Product Specifications and Reference Information A-1
  A.1 Physical Specifications A-1
  A.2 Electrical Specifications A-2
  A.3 Modem Setup Specifications A-2
    A.3.1 Setting Up the Modem A-2
    A.3.2 Serial Port Speed Change A-3
    A.3.3 Modem Recommendations A-4
      A.3.3.1 Cable A-4
      A.3.3.2 Modem Switch Settings (AT Commands) A-4
  A.4 Environmental Requirements A-5
  A.5 Reference Information A-6
    A.5.1 CD-ROM Drive Cabling Configuration A-6
    A.5.2 Ultra 10 Hard Drive Cabling Configuration A-7
    A.5.3 Hard Drive Cabling Configuration (With Two Mirrored Drives) A-7
    A.5.4 Jumper Settings A-8
    A.5.5 CD Handling and Use A-8
      A.5.5.1 Inserting a CD into the CD-ROM Drive A-8
      A.5.5.2 Ejecting a CD From the CD-ROM Drive A-9
B. Signal Descriptions  B-1
   B.1  Power Supply Connectors  B-2
   B.2  Keyboard /Mouse Connector  B-4
   B.3  Twisted-Pair Ethernet Connector  B-5
       B.3.1  TPE Cable-Type Connectivity  B-6
       B.3.2  External UTP-5 Cable Lengths  B-6
   B.4  Serial Port A Connector  B-7
   B.5  Serial Port B Connector  B-9
   B.6  Parallel Port Connector  B-10
   B.7  Audio Connectors  B-12
   B.8  Video Connector  B-13

C. Functional Description  C-1
   C.1  System  C-1
       C.1.1  CPU Module  C-3
       C.1.2  UPA  C-4
       C.1.3  PCI-IDE Interface  C-4
           C.1.3.1  Primary PCI Bus  C-5
           C.1.3.2  Secondary PCI Buses  C-5
           C.1.3.3  APB ASIC  C-5
           C.1.3.4  PCIO ASIC  C-5
           C.1.3.5  10-/100-Mbit Ethernet  C-5
           C.1.3.6  EBus2 Interface  C-6
           C.1.3.7  EIDE Interface  C-7
           C.1.3.8  PCI-Based Graphics  C-9
       C.1.4  Memory Architecture  C-10
           C.1.4.1  DIMM Memory Configuration  C-12
           C.1.4.2  DIMM Characteristics  C-12
           C.1.4.3  Memory Address Assignment  C-13
C.1.4.4 Transceivers C-14
C.1.5 PCI Riser Board C-14
   C.1.5.1 Connector Definition C-15
   C.1.5.2 PCI Riser Board Pin Assignment C-15
C.1.6 ASICs C-19
   C.1.6.1 APB C-19
   C.1.6.2 PCIO C-19
   C.1.6.3 RISC C-20
C.1.7 EBus2 Devices C-21
   C.1.7.1 SuperIO C-22
   C.1.7.2 Serial Communications Controller C-23
   C.1.7.3 Flash PROM C-23
   C.1.7.4 NVRAM/TOD C-24
   C.1.7.5 Audio C-24
C.1.8 Power and Standby Switching C-26
   C.1.8.1 Power Switch C-26
   C.1.8.2 Keyboard Standby or Power Key C-26
   C.1.8.3 Front Panel Standby Switch C-26
C.2 Clocking C-27
   C.2.1 CPU and UPA Clocking C-27
   C.2.2 PCI Clock Generation C-27
C.3 Address Mapping C-29
   C.3.1 Port Allocations C-29
   C.3.2 UPA Graphics Address Assignments C-30
   C.3.3 PCI Address Assignments C-31
     C.3.3.1 PCI Bus A Address Assignments C-31
     C.3.3.2 PCI Bus B Address Assignments C-31
C.4 Interrupts C-32
C.5 Power C-36
   C.5.1 Onboard Voltage Regulator C-36
   C.5.2 Power Supply Memory C-36
C.5.3 Power Management  C-36
C.6 Motherboard  C-37
C.7 Jumper Descriptions  C-38
  C.7.1 Serial Port Jumpers  C-39
  C.7.2 Flash PROM Jumpers  C-39
C.8 Enclosure  C-40

D. Software Notes  D-1
  D.1 PGX24 8- or 24-Bit Graphics  D-1
    D.1.1 What Does 8-Bit or 24-Bit Frame Buffer Refer To?  D-1
    D.1.2 The Difference Between 8-Bit Mode and 24-Bit Mode on Ultra 5 Onboard Graphics  D-2
    D.1.3 How to Install PGX24 Graphics Software on Solaris 2.5.1 HW:11/97  D-2
    D.1.4 How to Install PGX24 Graphics Software on Solaris 2.6 5/98  D-3
    D.1.5 Which Mode is Running  D-4
    D.1.6 Changing From One Mode to the Other  D-4
  D.2 Solaris 2.5.1 and 2.6 Software Upgrades for Systems Faster Than 420 MHz  D-5

Glossary  Glossary-1
Figures

FIGURE 1-1 Ultra 10 Minitower System 1-2
FIGURE 1-2 Ultra 10 System Front View 1-5
FIGURE 1-3 Ultra 10 System Back View 1-5
FIGURE 3-1 Setting Up a TIP Connection 3-2
FIGURE 3-2 Sun Type-5 Keyboard 3-5
FIGURE 3-3 Sun I/O Type-6 Keyboard 3-6
FIGURE 4-1 Power Supply Connector J17 Pin Configuration 4-6
FIGURE 5-2 System Standby Switch 5-6
FIGURE 5-3 Sun Type-5 Keyboard 5-6
FIGURE 5-4 Sun I/O Type-6 Keyboard 5-7
FIGURE 5-5 System Power Switch 5-7
FIGURE 5-6 Removing and Replacing the System Cover 5-9
FIGURE 5-7 Attaching the Wrist Strap to the Chassis 5-10
FIGURE 5-8 Removing a Plastic Filler Panel 5-12
FIGURE 5-9 Removing a Metal Filler Panel 5-13
FIGURE 6-1 Removing and Replacing the Power Supply 6-2
FIGURE 6-2 Removing and Replacing the Diskette Drive Cable Assembly 6-5
FIGURE 6-3 Removing and Replacing the Hard Drive Cable Assembly 6-7
FIGURE 6-4 Removing and Replacing the Serial/Parallel Cable Assembly 6-8
FIGURE 6-5 Removing and Replacing the Audio Cable  
6-10
FIGURE 6-6 Removing and Replacing the Speaker Assembly  
6-12
FIGURE 6-7 Removing and Replacing the CPU Fan Assembly  
6-14
FIGURE 6-8 Removing and Replacing the Front Bezel  
6-16
FIGURE 6-9 Removing and Replacing the Rear Hard Drive Bracket  
6-18
FIGURE 7-1 Removing and Replacing the Diskette Drive  
7-2
FIGURE 7-2 Removing and Replacing a Primary Hard Drive (Chassis Rear)  
7-5
FIGURE 7-3 Removing and Replacing a Secondary Hard Drive (Chassis Front)  
7-6
FIGURE 7-4 Hard Drive Mirroring Configuration  
7-8
FIGURE 7-5 Removing and Replacing a CD-ROM Drive  
7-14
FIGURE 8-1 Removing and Replacing the CPU Module  
8-3
FIGURE 8-2 Removing and Replacing the NVRAM/TOD  
8-5
FIGURE 8-3 Removing and Replacing a DIMM  
8-7
FIGURE 8-4 Removing and Replacing the Graphics Card  
8-10
FIGURE 8-5 Removing and Replacing the PCI Card  
8-13
FIGURE 8-6 Removing and Replacing the PCI Riser Board  
8-16
FIGURE 8-7 Removing and Replacing the Motherboard  
8-19
FIGURE 8-8 Identifying Jumper Pins  
8-20
FIGURE 9-1 Ultra 10 System Exploded View  
9-3
FIGURE 10-1 Removing and Replacing the System Cover  
10-2
FIGURE 10-2 System Power Switch  
10-3
FIGURE 10-3 System Standby Switch  
10-4
FIGURE 10-4 Sun Type-5 Keyboard  
10-4
FIGURE 10-5 Sun I/O Type-6 Keyboard  
10-5
FIGURE A-1 CD-ROM Drive Cabling Configuration  
A-6
FIGURE A-2 Ultra 10 Hard Drive Cabling Configuration  
A-7
FIGURE A-3 Hard Drive Mirroring Configuration  
A-7
FIGURE B-1 Power Supply Connector J12 Pin Configuration  
B-2
FIGURE B-2  Keyboard/Mouse Connector Pin Configuration  B-4
FIGURE B-3  TPE Connector Pin Configuration  B-5
FIGURE B-4  Serial Port A Connector Pin Configuration  B-7
FIGURE B-5  Serial Port B Connector Pin Configuration  B-9
FIGURE B-6  Parallel Port Connector Pin Configuration  B-10
FIGURE B-7  Audio Connector Configuration  B-12
FIGURE B-8  Video Connector Pin Configuration  B-13
FIGURE C-1  System Functional Block Diagram  C-2
FIGURE C-2  UPA Graphics Functional Block Diagram  C-4
FIGURE C-3  10-/100-Mbit Ethernet Functional Block Diagram  C-6
FIGURE C-4  EIDE Interface Functional Block Diagram  C-7
FIGURE C-5  EIDE Cable Labeling  C-8
FIGURE C-6  Supported Ultra 10 Configuration  C-8
FIGURE C-7  PCI-Based Graphics Functional Block Diagram (PGX)  C-9
FIGURE C-8  PCI-Based Graphics Functional Block Diagram (PGX24)  C-9
FIGURE C-9  Memory Interface Functional Block Diagram  C-11
FIGURE C-10  System Reset Functional Block Diagram  C-21
FIGURE C-11  Standard Serial Port Functional Block Diagram  C-22
FIGURE C-12  Communications Controller Serial Ports Functional Block Diagram  C-23
FIGURE C-13  NVRAM/TOD Functional Block Diagram  C-24
FIGURE C-14  Audio Circuit Functional Block Diagram  C-25
FIGURE C-15  Interrupt Scheme Block Diagram  C-33
FIGURE C-16  Motherboard Block Diagram  C-37
FIGURE C-17  Selected Jumper Settings  C-38
FIGURE C-18  Identifying Jumper Pins  C-38
FIGURE C-20  JP1/JP2 Jumper Settings for the Flash PROM  C-40
Tables

TABLE P-1 Document Organization xx
TABLE P-2 Typographic Conventions xxii
TABLE P-3 Shell Prompts xxii
TABLE P-4 Related Documents xxiii
TABLE 1-1 Supported I/O Devices 1-3
TABLE 1-2 Ultra 10 System Physical Dimensions 1-4
TABLE 1-3 Ultra 10 System Replaceable Components 1-6
TABLE 2-1 SunVTS Documentation 2-3
TABLE 3-1 Keyboard LED Error Indication Patterns 3-19
TABLE 4-1 Internal Drives Identification 4-4
TABLE 4-2 Power Supply Connector J17 Pin Assignments 4-6
TABLE 4-3 DIMM Physical Memory Address 4-7
TABLE 4-4 Selected OBP On-Board Diagnostic Tests 4-11
TABLE 8-1 DIMM Banks and Slot Pairs 8-6
TABLE 8-2 Serial Port Jumper Settings 8-20
TABLE 9-1 Ultra 10 System Replaceable Components 9-3
TABLE A-1 Ultra 10 Physical Specifications A-1
TABLE A-2 Ultra 10 System Electrical Specifications A-2
TABLE A-3 Ultra 10 System Environmental Requirements A-5
TABLE B-1 Power Supply Connector J12 Pin Assignments B-2
<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table B-2</td>
<td>Keyboard/Mouse Connector Pin Assignments</td>
<td>B-4</td>
</tr>
<tr>
<td>Table B-3</td>
<td>TPE Connector Pin Assignments</td>
<td>B-5</td>
</tr>
<tr>
<td>Table B-4</td>
<td>TPE UTP-5 Cables</td>
<td>B-6</td>
</tr>
<tr>
<td>Table B-5</td>
<td>Serial Port A Connector Pin Assignments</td>
<td>B-7</td>
</tr>
<tr>
<td>Table B-6</td>
<td>Serial Port B Connector Pin Assignments</td>
<td>B-9</td>
</tr>
<tr>
<td>Table B-7</td>
<td>Parallel Port Connector Pin Assignments</td>
<td>B-10</td>
</tr>
<tr>
<td>Table B-8</td>
<td>Audio Connector Line Assignment</td>
<td>B-12</td>
</tr>
<tr>
<td>Table B-9</td>
<td>Video Connector Pin Assignments</td>
<td>B-13</td>
</tr>
<tr>
<td>Table C-1</td>
<td>Ultra 10 CPU Module Cache and SRAM</td>
<td>C-3</td>
</tr>
<tr>
<td>Table C-2</td>
<td>Memory DIMM Configuration</td>
<td>C-12</td>
</tr>
<tr>
<td>Table C-3</td>
<td>PA Map Into RASx_L Signals</td>
<td>C-13</td>
</tr>
<tr>
<td>Table C-4</td>
<td>Memory Address Range Based on Installed DIMMs</td>
<td>C-13</td>
</tr>
<tr>
<td>Table C-5</td>
<td>PCI Riser Board Pin Summary</td>
<td>C-15</td>
</tr>
<tr>
<td>Table C-6</td>
<td>PCI Riser Board Pin Assignment</td>
<td>C-15</td>
</tr>
<tr>
<td>Table C-7</td>
<td>Audio Input Electrical Specification</td>
<td>C-25</td>
</tr>
<tr>
<td>Table C-8</td>
<td>Audio Output Electrical Specification</td>
<td>C-25</td>
</tr>
<tr>
<td>Table C-9</td>
<td>PCI Clocks</td>
<td>C-27</td>
</tr>
<tr>
<td>Table C-10</td>
<td>PCI Clock Generator Frequency Select (ICW48C60-422E)</td>
<td>C-28</td>
</tr>
<tr>
<td>Table C-11</td>
<td>PCI Clock Generator Frequency Select (CY2254A-2)</td>
<td>C-28</td>
</tr>
<tr>
<td>Table C-12</td>
<td>Port Allocations</td>
<td>C-29</td>
</tr>
<tr>
<td>Table C-13</td>
<td>UPA Address Space</td>
<td>C-30</td>
</tr>
<tr>
<td>Table C-14</td>
<td>CPU Module Internal CSR Space</td>
<td>C-30</td>
</tr>
<tr>
<td>Table C-15</td>
<td>PCI Address Assignments</td>
<td>C-31</td>
</tr>
<tr>
<td>Table C-16</td>
<td>Boot PROM/Flash PROM Address Assignments</td>
<td>C-32</td>
</tr>
<tr>
<td>Table C-17</td>
<td>Interrupt Routing</td>
<td>C-33</td>
</tr>
<tr>
<td>Table C-18</td>
<td>Serial Port Jumper Settings</td>
<td>C-39</td>
</tr>
<tr>
<td>Table C-19</td>
<td>Flash PROM Jumper Settings</td>
<td>C-40</td>
</tr>
</tbody>
</table>
Preface

The Sun Ultra 10 Service Manual provides detailed procedures that describe the removal and replacement of replaceable parts in the Sun™ Ultra™ 10 systems. The service manual also includes information about the use and maintenance of the systems. This manual is written for technicians, system administrators, authorized service providers (ASPs), and advanced computer system end users who have experience in troubleshooting and replacing hardware.

About the Multimedia Links in This Manual

Removal and replacement procedures for selected system components are also illustrated with interactive multimedia audio and video instructions in the Sun Ultra 10 ShowMe How2 multimedia documentation, which is linked to the online version of this manual. These multimedia links can be accessed wherever you see the following film-clip symbol:
How This Book Is Organized

This document is organized into chapters and appendixes as listed in the following table. A glossary is also included.

TABLE P-1   Document Organization

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Content Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>“Regulatory Compliance Statements and Declaration of Conformity,” page xxv</td>
<td>Provides regulatory compliance statements and the declaration of conformity for the product.</td>
</tr>
<tr>
<td>“Safety Agency Compliance Statements,” page xxix</td>
<td>Provides safety agency compliance statements.</td>
</tr>
<tr>
<td>Chapter 1, “Product Description”</td>
<td>Describes the major components of the system.</td>
</tr>
<tr>
<td>Chapter 2, “SunVTS Overview”</td>
<td>Describes the execution of individual tests for verifying hardware configuration and functionality.</td>
</tr>
<tr>
<td>Chapter 3, “Power-On Self-Test”</td>
<td>Describes the execution of POST and provides examples of POST output patterns.</td>
</tr>
<tr>
<td>Chapter 4, “Troubleshooting Procedures”</td>
<td>Provides troubleshooting advice and suggested corrective actions for hardware problems.</td>
</tr>
<tr>
<td>Chapter 5, “Preparing For Component Replacement”</td>
<td>Explains how to work safely when replacing system components. Provides procedures for powering off the system, removing the system cover, and attaching the wrist strap.</td>
</tr>
<tr>
<td>Chapter 6, “Major Subassemblies”</td>
<td>Provides procedures for removing and replacing major subassemblies.</td>
</tr>
<tr>
<td>Chapter 7, “Storage Devices”</td>
<td>Provides procedures for removing and replacing storage devices.</td>
</tr>
<tr>
<td>Chapter 8, “Motherboard and Component Replacement”</td>
<td>Provides procedures for removing and replacing the motherboard and various components associated with motherboard operation.</td>
</tr>
<tr>
<td>Chapter 9, “Illustrated Parts List”</td>
<td>Lists replaceable parts for the system.</td>
</tr>
<tr>
<td>Chapter 10, “Finishing Component Replacement”</td>
<td>Provides procedures for replacing the system cover and powering on the system.</td>
</tr>
<tr>
<td>Appendix A, “Product Specifications”</td>
<td>Provides specifications on power and environment, system dimensions, weight, memory mapping, and peripheral component interconnect (PCI) card slots.</td>
</tr>
</tbody>
</table>
Using UNIX Commands

For complete information on basic UNIX™ commands and procedures such as shutting down the system, booting the system, and configuring devices, refer to the following:

- *Solaris Handbook for Sun Peripherals*
- AnswerBook2™ online documentation for the Solaris™ software environment
- Other software documentation that you received with your system
Typographic Conventions

Typographic conventions used in this manual are listed in the following table.

**TABLE P-2  Typographic Conventions**

<table>
<thead>
<tr>
<th>Typeface or Symbol</th>
<th>Meaning</th>
<th>Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>AaBbCc123</td>
<td>The names of commands, files, and directories; on-screen computer output.</td>
<td>Edit your .login file.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Use ls -a to list all files.</td>
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<td></td>
<td></td>
<td>% You have mail.</td>
</tr>
<tr>
<td>AaBbCc123</td>
<td>What you type, when contrasted with on-screen computer output.</td>
<td>% su</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Password:</td>
</tr>
<tr>
<td>AaBbCc123</td>
<td>Book titles, new words or terms, words to be emphasized.</td>
<td>Read Chapter 6 in the User’s Guide.</td>
</tr>
<tr>
<td></td>
<td>Command-line variable; replace with a real name or value.</td>
<td>These are called class options.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>You must be root to do this.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>To delete a file, type rm filename.</td>
</tr>
</tbody>
</table>

Shell Prompts

The following table lists the default system prompt and superuser prompt for the C shell, Bourne shell, and Korn shell.

**TABLE P-3  Shell Prompts**

<table>
<thead>
<tr>
<th>Shell</th>
<th>Prompt</th>
</tr>
</thead>
<tbody>
<tr>
<td>C shell</td>
<td>machine_name%</td>
</tr>
<tr>
<td>C shell superuser</td>
<td>machine_name#</td>
</tr>
<tr>
<td>Bourne shell and Korn shell</td>
<td>$</td>
</tr>
<tr>
<td>Bourne shell and Korn shell</td>
<td>#</td>
</tr>
<tr>
<td>superuser</td>
<td></td>
</tr>
</tbody>
</table>
## Related Documents

Additional information for servicing the system are listed in the following table. Some of these documents are also available online on the *Solaris on Sun Hardware AnswerBook2*.

**TABLE P-4  Related Documents**

<table>
<thead>
<tr>
<th>Application</th>
<th>Title</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration</td>
<td><em>Solaris Handbook for Sun Peripherals</em></td>
<td>805-4440</td>
</tr>
<tr>
<td>Configuration</td>
<td><em>Solaris Handbook for Sun Frame Buffers</em></td>
<td>805-4441</td>
</tr>
<tr>
<td>Installation</td>
<td><em>Sun Ultra 5/10 Ultra 10 CD-ROM Drive and Hard Drive Installation Guide</em></td>
<td>805-7115</td>
</tr>
<tr>
<td>Software notes, preinstalled software</td>
<td><em>Getting Started with the Sun Ultra 10 Hardware and Software</em></td>
<td>805-0162</td>
</tr>
<tr>
<td>Specification</td>
<td><em>17-Inch Entry, 17-Inch Premium, and 20-Inch Premium Color Monitors Specifications</em></td>
<td>802-6178</td>
</tr>
<tr>
<td>Specification</td>
<td><em>Diskette Drive Specification</em></td>
<td>802-6285</td>
</tr>
</tbody>
</table>
Ordering Sun Documents

The docs.sun.com web site enables you to access Sun technical documentation on the web. You can browse the docs.sun.com archive or search for a specific book title or subject at:

http://docs.sun.com

Sun Welcomes Your Comments

We are interested in improving our documentation and welcome your comments and suggestions. You can email your comments to us at:

docfeedback@sun.com

Please include the part number of your document in the subject line of your email.
Regulatory Compliance Statements and Declaration of Conformity

Your Sun product is marked to indicate its compliance class:

• Federal Communications Commission (FCC) — USA
• Industry Canada Equipment Standard for Digital Equipment (ICES-003) - Canada
• Voluntary Control Council for Interference (VCCI) — Japan
• Bureau of Standards Metrology and Inspection (BSMI) - Taiwan

Please read the sections that correspond to the marking on your Sun product before attempting to install the product.

FCC Class A Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy, and if it is not installed and used in accordance with the instruction manual, it may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Shielded Cables: Connections between the workstation and peripherals must be made using shielded cables to comply with FCC radio frequency emission limits. Networking connections can be made using unshielded twisted-pair (UTP) cables.

Modifications: Any modifications made to this device that are not approved by Sun Microsystems, Inc. may void the authority granted to the user by the FCC to operate this equipment.

FCC Class B Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
• Reorient or relocate the receiving antenna.
• Increase the separation between the equipment and receiver.
• Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
• Consult the dealer or an experienced radio/television technician for help.

Shielded Cables: Connections between the workstation and peripherals must be made using shielded cables in order to maintain compliance with FCC radio frequency emission limits. Networking connections can be made using unshielded twisted pair (UTP) cables.

Modifications: Any modifications made to this device that are not approved by Sun Microsystems, Inc. may void the authority granted to the user by the FCC to operate this equipment.
ICES-003 Class A Notice - Avis NMB-003, Classe A
This Class A digital apparatus complies with Canadian ICES-003.
Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.

ICES-003 Class B Notice - Avis NMB-003, Classe B
This Class B digital apparatus complies with Canadian ICES-003.
Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

VCCI 基準について

クラス A VCCI 基準について
クラス A VCCI の表示があるワークステーションおよびオプション製品は、クラス A 情報技術装置です。これらの製品には、下記の項目が該当します。

この装置は、情報処理装置等電波障害自主規制協議会(VCCI)の基準に基づくクラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

クラス B VCCI 基準について
クラス B VCCI の表示 [ ] があるワークステーションおよびオプション製品は、クラス B 情報技術装置です。これらの製品には、下記の項目が該当します。

この装置は、情報処理装置等電波障害自主規制協議会(VCCI)の基準に基づくクラス B 情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。取扱説明書に従って正しい取り扱いをしてください。
BSMI Class A Notice

The following statement is applicable to products shipped to Taiwan and marked as Class A on the product compliance label.

警告使用者：
這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策。

Agency Compliance

The system complies with international and domestic regulatory requirements for safety, ergonomics, and electromagnetic compatibility. When installed and operated in accordance with this service manual, the EMC class marked on your system label remains the same.

German Acoustic Compliance

ACHTUNG: Der arbeitsplatzbezogene Schalldruckpegel nach DIN 45 635, Teil 1000 beträgt 70 Db(A) oder weniger.

Declaration of Conformity

The declaration of conformity for the Sun Ultra 10 product is on the following page.
Declaration of Conformity

Compliance ID: 201
Product Name: Sun Ultra 10 Family
This product has been tested and complies with:

EMC
USA — FCC Class B
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
1. This device may not cause harmful interference
2. This device must accept any interference received, including interference that may cause undesired operation.
European Union — EC
This equipment complies with the following requirements of the EMC Directive 89/336/EEC:
EN55022 / CISPR22 (1985) Class B
EN50082-1 IEC801-2 (1991) 4 kV (Direct), 8 kV (Air)
IEC801-3 (1984) 3 V/m
IEC801-4 (1988) 1.0 kV Power Lines, 0.5 kV Signal Lines
EN61000-3-2/IEC1000-3-2(1994) Pass

Safety
This equipment complies with the following requirements of the Low Voltage Directive 73/23/EEC:
EC Type Examination Certificates:
EN60950/IEC950 (1993)
EN60950 w/ Nordic Deviations

Supplementary Information
This product was tested and complies with all the requirements for the CE Mark.

/ S /  / S /
Dennis P. Symanski  DATE  John Shades  DATE
Manager, Product Compliance  Quality Assurance Manager

Sun Microsystems, Inc.  Sun Microsystems Scotland, Limited
901 San Antonio Road, M/S UMPK15-102  Springfield, Linlithgow
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Tel: 650-786-3255  Scotland, United Kingdom
Fax: 650-786-3723  Tel: 0506 670000

/ S /  / S /
Dennis P. Symanski  DATE  John Shades  DATE
Safety Agency Compliance Statements

Read this section before beginning any procedure. The following text provides safety precautions to follow when installing a Sun Microsystems product.

Safety Precautions
For your protection, observe the following safety precautions when setting up your equipment:

■ Follow all cautions and instructions marked on the equipment.
■ Ensure that the voltage and frequency of your power source match the voltage and frequency inscribed on the equipment’s electrical rating label.
■ Never push objects of any kind through openings in the equipment. Dangerous voltages may be present. Conductive foreign objects could produce a short circuit that could cause fire, electric shock, or damage to your equipment.

Symbols
The following symbols may appear in this book:

Caution – There is risk of personal injury and equipment damage. Follow the instructions.

Caution – Hot surface. Avoid contact. Surfaces are hot and may cause personal injury if touched.

Caution – Hazardous voltages are present. To reduce the risk of electric shock and danger to personal health, follow the instructions.

On – Applies AC power to the system.

Depending on the type of power switch your device has, one of the following symbols may be used:

Off - Removes AC power from the system.

Standby – The On/Standby switch is in the standby position.

Modifications to Equipment
Do not make mechanical or electrical modifications to the equipment. Sun Microsystems is not responsible for regulatory compliance of a modified Sun product.

Placement of a Sun Product

Caution – Do not block or cover the openings of your Sun product. Never place a Sun product near a radiator or heat register. Failure to follow these guidelines can cause overheating and affect the reliability of your Sun product.

Caution – The workplace-dependent noise level defined in DIN 45 635 Part 1000 must be 70Db(A) or less.

SELV Compliance
Safety status of I/O connections comply to SELV requirements.
Power Cord Connection

Caution – Sun products are designed to work with single-phase power systems having a grounded neutral conductor. To reduce the risk of electric shock, do not plug Sun products into any other type of power system. Contact your facilities manager or a qualified electrician if you are not sure what type of power is supplied to your building.

Caution – Not all power cords have the same current ratings. Household extension cords do not have overload protection and are not meant for use with computer systems. Do not use household extension cords with your Sun product.

Caution – Your Sun product is shipped with a grounding type (three-wire) power cord. To reduce the risk of electric shock, always plug the cord into a grounded power outlet.

The following caution applies only to devices with a Standby power switch:

Caution – The power switch of this product functions as a standby type device only. The power cord serves as the primary disconnect device for the system. Be sure to plug the power cord into a grounded power outlet that is nearby the system and is readily accessible. Do not connect the power cord when the power supply has been removed from the system chassis.

Lithium Battery

Caution – On Sun CPU boards, there is a lithium battery molded into the real-time clock, SGS No. MK48T59Y, MK48TXXB-XX, MK48T18-XXPCZ, M48T59W-XXPCZ, or MK48T08. Batteries are not customer replaceable parts. They may explode if mishandled. Do not dispose of the battery in fire. Do not disassemble it or attempt to recharge it.

Battery Pack

Caution – There is a sealed lead acid battery in Ultra 10 units. Portable Energy Products No. TLC02V50. There is danger of explosion if the battery pack is mishandled or incorrectly replaced. Replace only with the same type of Sun Microsystems battery pack. Do not disassemble it or attempt to recharge it outside the system. Do not dispose of the battery in fire. Dispose of the battery properly in accordance with local regulations.

System Unit Cover

You must remove the cover of your Sun computer system unit to add cards, memory, or internal storage devices. Be sure to replace the top cover before powering on your computer system.

Caution – Do not operate Sun products without the top cover in place. Failure to take this precaution may result in personal injury and system damage.

Laser Compliance Notice

Sun products that use laser technology comply with Class 1 laser requirements.
CD-ROM

Caution – Use of controls, adjustments, or the performance of procedures other than those specified herein may result in hazardous radiation exposure.

Einhaltung sicherheitsbehördlicher Vorschriften

Auf dieser Seite werden Sicherheitsrichtlinien beschrieben, die bei der Installation von Sun-Produkten zu beachten sind.

Sicherheitsvorkehrungen

Treffen Sie zu Ihrem eigenen Schutz die folgenden Sicherheitsvorkehrungen, wenn Sie Ihr Gerät installieren:

- Beachten Sie alle auf den Geräten angebrachten Warnhinweise und Anweisungen.
- Vergewissern Sie sich, daß Spannung und Frequenz Ihrer Stromquelle mit der Spannung und Frequenz übereinstimmen, die auf dem Etikett mit den elektrischen Nennwerten des Geräts angegeben sind.

Symbole

Die Symbole in diesem Handbuch haben folgende Bedeutung:

Achtung – Gefahr von Verletzung und Geräteschaden. Befolgen Sie die Anweisungen.

Achtung – Hohe Temperatur: Nicht berühren, da Verletzungsgefahr durch heiße Oberfläche besteht.

Achtung – Gefährliche Spannungen. Anweisungen befolgen, um Stromschläge und Verletzungen zu vermeiden.

Ein – Setzt das System unter Wechselstrom.

Je nach Netzschalttyp an Ihrem Gerät kann eines der folgenden Symbole benutzt werden:

Aus – Unterbricht die Wechselstromzufuhr zum Gerät.

Wartezustand (Stand-by-Position) - Der Ein-/Wartezustand-Schalter steht auf Wartezustand. Änderungen an Sun-Geräten.

Nehmen Sie keine mechanischen oder elektrischen Änderungen an den Geräten vor. Sun Microsystems, übernimmt bei einem Sun-Produkt, das geändert wurde, keine Verantwortung für die Einhaltung behördlicher Vorschriften.
Aufstellung von Sun-Geräten

**Achtung** – Um den zuverlässigen Betrieb Ihres Sun-Geräts zu gewährleisten und es vor Überhitzung zu schützen, dürfen die Öffnungen im Gerät nicht blockiert oder verdeckt werden. Sun-Produkte sollten niemals in der Nähe von Heizkörpern oder Heizluftklappen aufgestellt werden.

**Achtung** – Der arbeitsplatzbezogene Schalldruckpegel nach DIN 45 635 Teil 1000 beträgt 70Db(A) oder weniger.

Einhaltung der SELV-Richtlinien

Die Sicherung der I/O-Verbindungen entspricht den Anforderungen der SELV-Spezifikation.

Anschluß des Netzkabels

**Achtung** – Sun-Produkte sind für den Betrieb an Einphasen-Stromnetzen mit geerdetem Nullleiter vorgesehen. Um die Stromschlaggefahr zu reduzieren, schließen Sie Sun-Produkte nicht an andere Stromquellen an. Ihr Betriebsleiter oder ein qualifizierter Elektriker kann Ihnen die Daten zur Stromversorgung in Ihrem Gebäude geben.

**Achtung** – Nicht alle Netzkabel haben die gleichen Nennwerte. Herkömmliche, im Haushalt verwendete Verlängerungskabel besitzen keinen Überlastungsschutz und sind daher für Computersysteme nicht geeignet.

**Achtung** – Ihr Sun-Gerät wird mit einem dreidrigen Netzkabel für geerdete Netzsteckdosen geliefert. Um die Gefahr eines Stromschlags zu reduzieren, schließen Sie das Kabel nur an eine fachgerecht verlegte, geerdete Steckdose an.

Die folgende Warnung gilt nur für Geräte mit Wartezustand-Netzschalter:


Lithiumbatterie


Batterien

Gehäuseabdeckung

Sie müssen die obere Abdeckung Ihres Sun-Systems entfernen, um interne Komponenten wie Karten,
Speicherchips oder Massenspeicher hinzuzufügen. Bringen Sie die obere Gehäuseabdeckung wieder an, bevor Sie Ihr System einschalten.

**Achtung** – Bei Betrieb des Systems ohne obere Abdeckung besteht die Gefahr von Stromschlag und Systemschäden.

Einhaltung der Richtlinien für Laser
Sun-Produkte, die mit Laser-Technologie arbeiten, entsprechen den Anforderungen der Laser Klasse 1.

**Class 1 Laser Product**
Luokan 1 Laserlaite
Klasse 1 Laser Apparat
Laser Klasse 1

**CD-ROM**

**Warnung** – Die Verwendung von anderen Steuerungen und Einstellungen oder die Durchführung von Prozeduren, die von den hier beschriebenen abweichen, können gefährliche Strahlungen zur Folge haben.

Conformité aux normes de sécurité
Ce texte traite des mesures de sécurité qu’il convient de prendre pour l’installation d’un produit Sun Microsystems.

Mesures de sécurité
Pour votre protection, veuillez prendre les précautions suivantes pendant l’installation du matériel :

- Suivre tous les avertissements et toutes les instructions inscrites sur le matériel.
- Vérifier que la tension et la fréquence de la source d’alimentation électrique correspondent à la tension et à la fréquence indiquées sur l’étiquette de classification de l’appareil.

**Symboles**
Vous trouverez ci-dessous la signification des différents symboles utilisés :

- **Attention** – risques de blessures corporelles et de dégâts matériels. Veuillez suivre les instructions.

- **Attention** – surface à température élevée. Évitez le contact. La température des surfaces est élevée et leur contact peut provoquer des blessures corporelles.

- **Attention** – présence de tensions dangereuses. Pour éviter les risques d’électrocution et de danger pour la santé physique, veuillez suivre les instructions.

- **MARCHE** – Votre système est sous tension (courant alternatif).

- **ARRET** – Votre système est hors tension (courant alternatif).

- **VEILLEUSE** – L'interrupteur Marche/ Veilleuse est en position « Veilleuse ».

Modification du matériel
Ne pas apporter de modification mécanique ou électrique au matériel. Sun Microsystems n’est pas responsable de la conformité réglementaire d’un produit Sun qui a été modifié.
Positionnement d’un produit Sun

Attention: – pour assurer le bon fonctionnement de votre produit Sun et pour l’empêcher de surchauffer, il convient de ne pas obstruer ni recouvrir les ouvertures prévues dans l’appareil. Un produit Sun ne doit jamais être placé à proximité d’un radiateur ou d’une source de chaleur.

Attention: – Le niveau de pression acoustique au poste de travail s’élève selon la norme DIN 45 635 section 1000, à 70 dB (A) ou moins.

Conformité SELV
Sécurité: les raccordements E/S sont conformes aux normes SELV.

Connexion du cordon d’alimentation

Attention: – les produits Sun sont conçus pour fonctionner avec des alimentations monophasées munies d’un conducteur neutre mis à la terre. Pour écarter les risques d’électrocution, ne pas brancher de produit Sun dans un autre type d’alimentation secteur. En cas de doute quant au type d’alimentation électrique du local, veuillez vous adresser au directeur de l’exploitation ou à un électricien qualifié.

Attention: – tous les cordons d’alimentation n’ont pas forcément la même puissance nominale en matière de courant. Les rallonges d’usage domestique n’offrent pas de protection contre les surcharges et ne sont pas prévues pour les systèmes d’ordinateurs. Ne pas utiliser de rallonge d’usage domestique avec votre produit Sun.

Attention: – votre produit Sun a été livré équipé d’un cordon d’alimentation à trois fils (avec prise de terre). Pour écarter tout risque d’électrocution, branchez toujours ce cordon dans une prise mise à la terre.

L’avertissement suivant s’applique uniquement aux systèmes équipés d’un interrupteur VEILLEUSE:

Attention: – le commutateur d’alimentation de ce produit fonctionne comme un dispositif de mise en veille uniquement. C’est la prise d’alimentation qui sert à mettre le produit hors tension. Veillez donc à installer le produit à proximité d’une prise murale facilement accessible. Ne connectez pas la prise d’alimentation lorsque le châssis du système n’est plus alimenté.

Batterie au lithium

Bloc-batterie

Attention: – Les unités Ultra 10 contiennent une batterie étanche au plomb (produits énergétiques portatifs n°TLC02V50). Il existe un risque d’explosion si ce bloc-batterie est manipulé de façon erronée ou mal mis en place. Ne remplacez ce bloc que par un bloc-batterie Sun Microsystems du même type. Ne le démontez pas et n’essayez pas de le recharger hors du système. Ne faites pas brûler la batterie mais mettez-la au rebut conformément aux réglementations locales en vigueur.

Couvercle

Pour ajouter des cartes, de la mémoire, ou des unités de stockage internes, vous devrez démonter le couvercle de l’unité système Sun. Ne pas oublier de remettre ce couvercle en place avant de mettre le système sous tension.

Attention: – il est dangereux de faire fonctionner un produit Sun sans le couvercle en place. Si l’on néglige cette précaution, on encourt des risques de blessures corporelles et de dégâts matériels.

Conformité aux certifications Laser

Les produits Sun qui font appel aux technologies lasers sont conformes aux normes de la classe 1 en la matière.

CD-ROM

Attention: – L’utilisation de contrôles, de réglages ou de performances de procédures autre que celle spécifiée dans le présent document peut provoquer une exposition à des radiations dangereuses.

Normativas de seguridad

El siguiente texto incluye las medidas de seguridad que se deben seguir cuando se instale algún producto de Sun Microsystems.

Precauciones de seguridad

Para su protección observe las siguientes medidas de seguridad cuando maneje su equipo:

- Siga todas los avisos e instrucciones marcados en el equipo.
- Asegúrese de que el voltaje y la frecuencia de la red eléctrica concuerden con las descritas en las etiquetas de especificaciones eléctricas del equipo.
- No introduzca nunca objetos de ningún tipo a través de los orificios del equipo. Pueden haber voltajes peligrosos. Los objetos extraños conductores de la electricidad pueden producir cortocircuitos que provoquen un incendio, descargas eléctricas o daños en el equipo.

Símbolos

En este libro aparecen los siguientes símbolos:

Precaución – Existe el riesgo de lesiones personales y daños al equipo. Siga las instrucciones.

Precaución – Superficie caliente. Evite el contacto. Las superficies están calientes y pueden causar daños personales si se tocan.
Según el tipo de interruptor de encendido que su equipo tenga, es posible que se utilice uno de los siguientes símbolos:

Encendido – Aplica la alimentación de CA al sistema.

Apagado - Elimina la alimentación de CA del sistema.

En espera – El interruptor de Encendido/En espera se ha colocado en la posición de En espera.

Modificaciones en el equipo
No realice modificaciones de tipo mecánico o eléctrico en el equipo. Sun Microsystems no se hace responsable del cumplimiento de las normativas de seguridad en los equipos Sun modificados.

Ubicación de un producto Sun

Precaución – Para asegurar la fiabilidad de funcionamiento de su producto Sun y para protegerlo de sobrecalentamientos, no deben obstruirse o taparse las rejillas del equipo. Los productos Sun nunca deben situarse cerca de radiadores o de fuentes de calor.

Precaución – De acuerdo con la norma DIN 45 635, Parte 1000, se admite un nivel de presión acústica para puestos de trabajo máximo de 70Db(A).

Cumplimiento de la normativa SELV
El estado de la seguridad de las conexiones de entrada/salida cumple los requisitos de la normativa SELV.

Conexión del cable de alimentación eléctrica

Precaución – Los productos Sun están diseñados para trabajar en una red eléctrica monofásica con toma de tierra. Para reducir el riesgo de descarga eléctrica, no conecte los productos Sun a otro tipo de sistema de alimentación eléctrica. Póngase en contacto con el responsable de mantenimiento o con un electricista cualificado si no está seguro del sistema de alimentación eléctrica del que se dispone en su edificio.

Precaución – No todos los cables de alimentación eléctrica tienen la misma capacidad. Los cables de tipo doméstico no están provistos de protecciones contra sobrecargas y por tanto no son apropiados para su uso con computadores. No utilice alargadores de tipo doméstico para conectar sus productos Sun.

Precaución – Con el producto Sun se proporciona un cable de alimentación con toma de tierra. Para reducir el riesgo de descargas eléctricas conectelo siempre a un enchufe con toma de tierra.
La siguiente advertencia se aplica solamente a equipos con un interruptor de encendido que tenga una posición “En espera”:

**Precaución** – El interruptor de encendido de este producto funciona exclusivamente como un dispositivo de puesta en espera. El enchufe de la fuente de alimentación está diseñado para ser el elemento primario de desconexión del equipo. El equipo debe instalarse cerca del enchufe de forma que este último pueda ser fácil y rápidamente accesible. No conecte el cable de alimentación cuando se ha retirado la fuente de alimentación del chasis del sistema.

**Batería de litio**

**Precaución** – En las placas de CPU Sun hay una batería de litio insertada en el reloj de tiempo real, tipo SGS Núm. MK48T59Y, MK48TXXB-XX, MK48T18-XXXPCZ, M48T59W-XXXPCZ, o MK48T08. Las baterías no son elementos reemplazables por el propio cliente. Pueden explotar si se manipulan de forma errónea. No arroje las baterías al fuego. No las abra o intente recargarlas.

**Paquete de pilas**

**Precaución** – Las unidades Ultra 10 contienen una pila de plomo sellada, Productos de energía portátil n° TLC02V50. Existe riesgo de estallido si el paquete de pilas se maneja sin cuidado o se sustituye de manera indebida. Las pilas sólo deben sustituirse por el mismo tipo de paquete de pilas de Sun Microsystems. No las desmonte ni intente recargarlas fuera del sistema. No arroje las pilas al fuego. Deséchelas siguiendo el método indicado por las disposiciones vigentes.

**Tapa de la unidad del sistema**

Debe quitar la tapa del sistema cuando sea necesario añadir tarjetas, memoria o dispositivos de almacenamiento internos. Asegúrese de cerrar la tapa superior antes de volver a encender el equipo.

**Aviso de cumplimiento con requisitos de láser**

Los productos Sun que utilizan la tecnología de láser cumplen con los requisitos de láser de Clase 1.
GOST-R Certification Mark

Nordic Lithium Battery Cautions

Norge

ADVAREL – Lithiumbatteri —

Sverige


Danmark

ADVAREL! – Litiumbatteri —
Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

Suomi

Product Description

The Ultra 10 systems are uniprocessor devices that use the family of UltraSPARC™ processors. They support high-performance CPU module (UltraSPARC-III) processing and high-performance graphics. FIGURE 1-1 illustrates the Ultra 10 minitower-style system.

This chapter contains the following topics:

- Section 1.1 “Feature Overview” on page 1-2
- Section 1.2 “I/O Devices” on page 1-3
- Section 1.3 “System Description” on page 1-4
- Section 1.4 “Replaceable Components” on page 1-6
1.1 Feature Overview

The Ultra 10 system provides the following features:

- Minitower-style enclosure
- 250-watt power supply
- UltraSPARC-III processor module (CPU module)/advanced PCI bridge (APB) application-specific integrated circuit (ASIC)
- 480-MHz, 440-MHz, 360-MHz, 333-MHz, or 300-MHz CPU module
- 1-gigabyte (Gbyte) memory (maximum)
- Four PCI slots (PCI riser board expansion with four long PCI cards)
- 33-megahertz (MHz), 32-bit peripheral component interconnect (PCI)
- One dedicated front-access 5.25-inch bay
- One optional front-access 5.25-inch bay
- Up to two enhanced integrated drive electronic (IDE) hard drives
- Front access Personal Computer Memory Card International Association (PCMCIA) bay (two Type II or one Type III slot(s))
- CD-ROM drive
- CD quality audio
1.44-megabyte (Mbyte) manual-eject diskette drive
- PGX on-board graphics or PGX24 PCI on-board graphics

**Note** – Systems with PGX24 graphics have either "PGX24" or "Series 3" printed on the serial number label that is affixed to the front bezel.

- One UltraSPARC port architecture (UPA) graphics slot
- Two serial ports
- One parallel port
- 10-/100-megabit per second Ethernet

**Note** – This manual covers all versions of the Ultra 10. You can determine which version you have from the information printed on the serial number label that is affixed to the front bezel. If the label contains:
* Serial number only - Ultra 10 system,
* Serial number and PGX24 - Ultra 10 Model 333 or Model 360,
* Serial number and Series 3 - Ultra 10 Model 440 or Model 480

### 1.2 I/O Devices

The Ultra 10 workstations use the I/O devices listed in **TABLE 1-1**.

<table>
<thead>
<tr>
<th>I/O Device</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>17-inch (43-cm) color monitor</td>
<td>1280 x 1024 resolution, 76- or 66-Hz refresh rate, 110 dots per inch (dpi)</td>
</tr>
<tr>
<td>20-inch (51-cm) color monitor</td>
<td>1152 x 900 resolution, 76- or 66-Hz refresh rate, 84 dpi</td>
</tr>
<tr>
<td></td>
<td>1280 x 1024 resolution, 76- or 66-Hz refresh rate, 93 dpi</td>
</tr>
<tr>
<td></td>
<td>960 x 680 resolution, 112-Hz refresh rate, 70 dpi</td>
</tr>
<tr>
<td>24-inch (61-cm) color monitor</td>
<td>1920 x 1200 resolution, 70-Hz refresh rate, 103 dpi</td>
</tr>
<tr>
<td></td>
<td>1600 x 1000 resolution, 76- or 66-Hz refresh rate, 86 dpi</td>
</tr>
<tr>
<td></td>
<td>1400 x 900 resolution, 76-Hz refresh rate, 77 dpi</td>
</tr>
<tr>
<td></td>
<td>1280 x 800 resolution, 76-Hz refresh rate, 69 dpi</td>
</tr>
</tbody>
</table>
### 1.3 System Description

System components are housed in a minitower-style enclosure. Overall chassis dimensions for the Ultra 10 system are listed in the following table.

<table>
<thead>
<tr>
<th>I/O Device</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microphone</td>
<td>SunMicrophone™ II (optional)</td>
</tr>
<tr>
<td>Keyboard</td>
<td>Sun Type-5: AT 101 or UNIX layout available; Sun Type 6: AT 101 layout</td>
</tr>
<tr>
<td>Mouse</td>
<td>Sun Type-5, 3-button optomechanical mouse; Sun Type-6, 3-button crossbow mouse</td>
</tr>
</tbody>
</table>

#### TABLE 1-2  Ultra 10 System Physical Dimensions

<table>
<thead>
<tr>
<th>Unit</th>
<th>Width</th>
<th>Height</th>
<th>Depth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ultra 10</td>
<td>6.93 inches (17.60 cm)</td>
<td>15.75 inches (40.00 cm)</td>
<td>16.54 inches (42.00 cm)</td>
</tr>
<tr>
<td>Minitower enclosure</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

System electronics are contained on a single printed circuit board (motherboard). The motherboard contains the CPU module, memory modules, system control ASICs, and I/O ASICs.

The following figures illustrate the Ultra 10 system front and back views.
Chapter 1 Product Description

FIGURE 1-2 Ultra 10 System Front View

FIGURE 1-3 Ultra 10 System Back View
1.4 Replaceable Components

The following table lists the Ultra 10 system replaceable components. A brief description of each listed component is also provided.

**Note** – Consult your authorized Sun sales representative or service provider prior to ordering a replacement part.

<table>
<thead>
<tr>
<th>Component Description</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manual eject floppy</td>
<td>Diskette drive</td>
</tr>
<tr>
<td>Speaker assembly</td>
<td>Speaker assembly</td>
</tr>
<tr>
<td>Fan assembly</td>
<td>CPU fan, 92-mm</td>
</tr>
<tr>
<td>CD-ROM drive</td>
<td>CD-ROM drive</td>
</tr>
<tr>
<td>16-Mbyte DIMM</td>
<td>60-ns, 16-Mbyte DIMM</td>
</tr>
<tr>
<td>32-Mbyte DIMM</td>
<td>60-ns, 32-Mbyte DIMM</td>
</tr>
<tr>
<td>64-Mbyte DIMM</td>
<td>60-ns, 64-Mbyte DIMM</td>
</tr>
<tr>
<td>128-Mbyte DIMM</td>
<td>60-ns, 128-Mbyte DIMM</td>
</tr>
<tr>
<td>256-Mbyte DIMM</td>
<td>60-ns, 256-Mbyte DIMM</td>
</tr>
<tr>
<td>32-Mbyte DIMM</td>
<td>50-ns, 32-Mbyte DIMM</td>
</tr>
<tr>
<td>64-Mbyte DIMM</td>
<td>50-ns, 64-Mbyte DIMM</td>
</tr>
<tr>
<td>128-Mbyte DIMM</td>
<td>50-ns, 128-Mbyte DIMM</td>
</tr>
<tr>
<td>256-Mbyte DIMM</td>
<td>50-ns, 256-Mbyte DIMM</td>
</tr>
<tr>
<td>CPU module</td>
<td>300-MHz, 512-Kbyte external cache</td>
</tr>
<tr>
<td>CPU module</td>
<td>333-MHz, 2-Mbyte external cache</td>
</tr>
<tr>
<td>CPU module</td>
<td>360-MHz, 2-Mbyte external cache</td>
</tr>
</tbody>
</table>
TABLE 1-3  Ultra 10 System Replaceable Components (Continued)

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU module</td>
<td>440-MHz, 2-MKbyte external cache</td>
</tr>
<tr>
<td>CPU module</td>
<td>480-MHz, 2-Mbyte external cache</td>
</tr>
<tr>
<td>Motherboard</td>
<td>System board</td>
</tr>
<tr>
<td>NVRAM/TOD</td>
<td>Time of day, 48T59, with carrier</td>
</tr>
<tr>
<td>PCI card</td>
<td>Generic</td>
</tr>
<tr>
<td>PCI riser board</td>
<td>4-slot PCI riser board</td>
</tr>
<tr>
<td>Hard drive</td>
<td>Disk drive, 9.1-Gbyte, 7200 RPM</td>
</tr>
<tr>
<td>Hard drive bracket</td>
<td>9.1-Gbyte rear hard drive bracket</td>
</tr>
<tr>
<td>Power supply</td>
<td>Power supply, 250 watts</td>
</tr>
<tr>
<td>Graphics card</td>
<td>Vertical, double buffer plus Z (DBZ) UPA graphics</td>
</tr>
<tr>
<td>Graphics card</td>
<td>Vertical, single-buffer UPA graphics card</td>
</tr>
<tr>
<td>Graphics card</td>
<td>Vertical, double-buffer UPA graphics card</td>
</tr>
<tr>
<td>Graphics card</td>
<td>Elite3D m3 UPA graphics card</td>
</tr>
<tr>
<td>Graphics card</td>
<td>Elite3D m6 UPA graphics card</td>
</tr>
<tr>
<td>Front bezel</td>
<td>System front bezel</td>
</tr>
<tr>
<td>Audio cable assembly</td>
<td>Cable assembly.</td>
</tr>
<tr>
<td>Service kit</td>
<td>Includes diskette drive cable assembly, hard drive cable</td>
</tr>
<tr>
<td></td>
<td>assembly, serial/parallel cable assembly, and CD-ROM drive</td>
</tr>
<tr>
<td></td>
<td>drive cable assembly</td>
</tr>
</tbody>
</table>

**Note** – The Ultra 10 diskette drive cable assembly, hard drive cable assembly, serial/parallel cable assembly, and CD-ROM drive cable assembly are part of service kit 370-3266 and cannot be ordered separately.
SunVTS Overview

This chapter contains an overview of the SunVTS™ diagnostic tool.

This chapter contains the following topics:
■ Section 2.1 “SunVTS Description” on page 2-1
■ Section 2.1.1 “SunVTS Requirements” on page 2-2
■ Section 2.1.2 “SunVTS References” on page 2-2

2.1 SunVTS Description

SunVTS is Sun’s online Validation Test Suite. SunVTS is a comprehensive software diagnostic package that tests and validates hardware by verifying the connectivity and functionality of most hardware controllers, devices, and platforms.

SunVTS can be tailored to run on various types of systems ranging from desktops to servers with many customizable features to meet the varying requirements of many diagnostic situations.

Use SunVTS to validate a system during development, production, receiving inspection, troubleshooting, periodic maintenance, and system or subsystem stressing.
SunVTS executes multiple diagnostic tests from one graphical user interface (GUI) that provides test configuration and status monitoring. The user interface can run in the CDE or OPEN LOOK environments or through a TTY-mode interface for situations when running a GUI is not possible.

The SunVTS interface can run on one system to display the SunVTS test session of another system on the network.

SunVTS is distributed with each SPARC™ Solaris™ operating environment release. It is located on the Sun Computer Systems Supplement CD.

### 2.1.1 SunVTS Requirements

Your system must meet the following requirements to run SunVTS:

- The SunVTS packages must be installed. The main package is SUNWvts. There are additional supporting packages that differ based on the version of the Solaris operating environment that is installed. For specific details, refer to the corresponding SunVTS documentation (described below).
- The system must be booted to the multiuser level (level 3).
- To run SunVTS with a GUI, that GUI must be installed. Otherwise, run SunVTS with the TTY-mode interface.

### 2.1.2 SunVTS References

For more information about using SunVTS, refer to the SunVTS documentation that corresponds to the Solaris software version that you are running.

The SunVTS documents are part of the Solaris on Sun Hardware AnswerBook collection. This AnswerBook collection is preinstalled on the hard disk of new systems. It is also distributed on the Software Supplement CD that is part of each Solaris Media Kit release and is also accessible at http://docs.sun.com.

The following list describes the content of each SunVTS document:

- **SunVTS User’s Guide** – describes how to install, configure, and run the SunVTS diagnostic software.
- **SunVTS Quick Reference Card** – provides an overview of how to use the SunVTS CDE interface.
- **SunVTS Test Reference Manual** – provides details about each individual SunVTS test.
CHAPTER 3

Power-On Self-Test

This chapter describes how to initiate power-on self-test (POST) diagnostics.

This chapter contains the following topics:
- Section 3.1 “POST Overview” on page 3-1
- Section 3.2 “Pre-POST Preparation” on page 3-2
- Section 3.3 “Initializing POST” on page 3-5
- Section 3.4 “Maximum and Minimum POST Levels” on page 3-7
- Section 3.5 “Bypassing POST” on page 3-22
- Section 3.6 “Resetting Variables to Default Settings” on page 3-22
- Section 3.7 “Initializing Motherboard POST” on page 3-23

3.1 POST Overview

POST is useful in determining if a portion of the system has failed and should be replaced. POST detects approximately 95 percent of system faults and is located in the motherboard OpenBoot™ PROM (OBP). The setting of two NVRAM variables, diag-switch? and diag-level, determines whether POST is executed and to what level (see Section 3.3 “Initializing POST” on page 3-5).
3.2 Pre-POST Preparation

Pre-POST preparation includes:

- Setting up a TIP connection to another workstation or terminal to view POST progress and error messages. See Section 3.2.1 “Setting Up a TIP Connection” on page 3-2.

- Verifying baud rates between a workstation and a monitor or terminal. See Section 3.2.2 “Verifying the Baud Rate” on page 3-4.

If a terminal or a monitor is not connected to serial port A (default port) of a workstation to be tested, the keyboard light-emitting diodes (LEDs) are used to determine error conditions. See Section 3.4.3 “POST Progress and Error Reporting” on page 3-19.

3.2.1 Setting Up a TIP Connection

A TIP connection enables a remote shell window to be used as a terminal to display test data from a tested system. Serial port A or serial port B of a tested system is connected to another Sun workstation monitor or TTY-type terminal.

To set up a TIP connection, proceed as follows:

1. Connect serial port A of the tested system to serial port B of a second Sun workstation using a serial null modem cable (connect cable pins 2-3, 3-2, 7-20, and 20-7). See FIGURE 3-1.

![FIGURE 3-1 Setting Up a TIP Connection](image)
2. At the second Sun workstation, check the `/etc/remote` file by changing to the `/etc` directory and editing the `remote` file. The following sample `remote` file text shows connection to serial port B:

```
hardwire: /dv=/dev/term/b:br#9600:el=^C^S^Q^U^D:ie=%$:oe=^D:
```

3. To use serial port A:
   
a. Copy and paste the `remote` file text that shows connection to serial port B.
   
b. Modify the pasted text as follows to change the connection to serial port A:

```
hardwire: /dv=/dev/term/a:br#9600:el=^C^S^Q^U^D:ie=%$:oe=^D:
```

4. In a shell window on the second Sun workstation, type `tip hardwire`.

```
% tip hardwire
connected
```

The shell window becomes a TIP window directed to serial port A of the tested system. When power is applied to the tested system, POST messages are displayed in this shell window.

5. When POST is completed, disconnect the TIP connection as follows:
   
a. Open another shell window at the second workstation.
   
b. Type `ps -a` to view the active TIP line and process ID (PID) number.
   
c. Type the following to disconnect the TIP hardwire process.

```
% kill -9 PID#
```
3.2.2 Verifying the Baud Rate

To verify the baud rate between the tested system and a terminal or another Sun workstation monitor:

1. Open a shell window.
2. Type `eeprom`.
3. Verify the following serial port default settings:

   ttyb-mode = 9600,8,n,1
   ttya-mode = 9600,8,n,1

**Note** – Ensure that the settings are consistent with TTY-type terminal or workstation monitor settings.
3.3 Initializing POST

POST can be initialized in two ways:

- By setting the diag-switch? to true and the diag-level to max or min, followed by power-cycling the system
- By simultaneously pressing the keyboard Stop and D keys while power is applied to the system

To set the diag-switch? to true and power-cycle the system:

1. At the system prompt, type:

```
ok% setenv diag-switch? true
```

2. At the keyboard (Sun Type-5 or Sun I/O Type-6), power-cycle the system by simultaneously pressing the Shift key and the Standby (Power) key. After a few seconds, press the Standby (Power) key again (see FIGURE 3-2 or FIGURE 3-3).

![Sun Type-5 Keyboard Diagram](image)

**FIGURE 3-2** Sun Type-5 Keyboard
3. Verify the following:
   - The display prompt is no longer displayed.
   - The monitor power-on indicator flashes on and off.
   - The keyboard Caps Lock key indicator flashes on and off.

4. When the POST is complete, type the following at the system prompt:

   ```
   ok% setenv diag-switch? false
   ```
3.4 Maximum and Minimum POST Levels

Two levels of POST are available: maximum (max) level and minimum (min) level. The system initiates the selected level of POST based upon the setting of diag-level, an NVRAM variable. The default setting for diag-level is max.

To set the diag-level variable to min before power-cycling the system, type:

```
ok% setenv diag-level min
```

To return to the default setting:

```
ok% setenv diag-level max
```

An example of a max-level POST output on serial port A is provided in Section 3.4.1 “diag-level Variable Set to max” on page 3-7. An example of a min-level POST output on serial port A is provided in Section 3.4.2 “diag-level Variable Set to min” on page 3-15.

3.4.1 diag-level Variable Set to max

When you set the diag-level variable to max, POST enables an extended set of diagnostic-level tests. This mode requires approximately two minutes to complete (with 128 Mbytes of DIMM installed). CODE EXAMPLE 3-1 shows a typical serial port A POST output with diag-level set to max.

**Note** – Video output is disabled while POST is initialized.

```
CODE EXAMPLE 3-1  diag-level Variable Set to max

Power On Selftest Completed
Software Power ON0.0000.0000.0000 ffff.ffff.f00b.4100
0002.3333.0200.001b
@(#) Sun Ultra 5/10 UPA/PCI 3.9 P2.1 Version 9 created 1997/08/05 16:24
Clearing E$ Tags Done
Clearing I/D TLBs Done
Probing Memory Done
```
MEM BASE = 0000.0000.0000.0000
MEM SIZE = 0000.0000.1000.0000
11-Column Mode Enabled
MMUs ON
Copy Done
PC = 0000.01ff.f000.20ec
PC = 0000.0000.0000.2130
Decompressing into Memory Done
Size = 0000.0000.0007.5300
ttya initialized
Reset Control: BXIR:0 BPOR:0 SXIR:0 SPOR:1 POR:0
UltraSPARC-IIi 2-2 module
Probing Memory Bank #0 128 + 128 : 256 Megabytes
Probing Memory Bank #2 0 + 0 : 0 Megabytes
Probing Floppy: drive detected on ID0
Probing EBUS SUNW,CS4231
Probing UPA Slot at 1e,0 SUNW,ffb
Probing /pci@1f,0/pci@1,1 at Device 2 SUNW,m64B
Probing /pci@1f,0/pci@1,1 at Device 3 ide disk cdrom
Probing /pci@1f,0/pci@1,1 at Device 1 Nothing there
Probing /pci@1f,0/pci@1,1 at Device 2 Nothing there
Probing /pci@1f,0/pci@1,1 at Device 3 Nothing there
Probing /pci@1f,0/pci@1,1 at Device 4 Nothing there
Reset Control: BXIR:0 BPOR:0 SXIR:0 SPOR:1 POR:0
UltraSPARC-IIi 2-2 module
Probing Memory Bank #0 128 + 128 : 256 Megabytes
Probing Memory Bank #2 0 + 0 : 0 Megabytes
Probing Floppy: drive detected on ID0
Probing EBUS SUNW,CS4231
Probing UPA Slot at 1e,0 SUNW,ffb
Probing /pci@1f,0/pci@1,1 at Device 2 SUNW,m64B
Probing /pci@1f,0/pci@1,1 at Device 3 ide disk cdrom
Probing /pci@1f,0/pci@1,1 at Device 1 Nothing there
Probing /pci@1f,0/pci@1,1 at Device 2 Nothing there
Probing /pci@1f,0/pci@1,1 at Device 3 Nothing there
Probing /pci@1f,0/pci@1,1 at Device 4 Nothing there

Sun Ultra 5/10 UPA/PCI (UltraSPARC-IIi 300MHz), No Keyboard
OpenBoot 3.9 P2.1 , 256 MB memory installed, Serial #9337477.
Ethernet address 8:0:20:8e:7a:85, Host ID: 808e7a85.

ok Hardware Power ON

@(#) Sun Ultra 5/10 UPA/PCI  3.9 P2.1  Version 9 created 1997/08/05 16:24
Probing keyboard Done
%o0 = 0000.0000.0000.4001

Executing Power On SelfTest

@(#) Sun Ultra 5/10 (Darwin) POST 2.1.1 (Build No. 293) 08/21/97: 15:59

CPU: UltraSPARC-LC (MHz: 301 Ecache Size: 512KB)

Init POST BSS
    Init System BSS
    NVRAM
        NVRAM Battery Detect Test
        NVRAM Scratch Addr Test
        NVRAM Scratch Data Test
    DMMU TLB Tags
        DMMU TLB Tag Access Test
    DMMU TLB RAM
        DMMU TLB RAM Access Test
    Probe Ecache
        Probe Ecache
    Ecache Tests
        Ecache RAM Addr Test
        Ecache Tag Addr Test
        Ecache RAM Test
        Ecache Tag Test

All CPU Basic Tests
    V9 Instruction Test
    CPU Tick and Tick Compare Reg Test
    CPU Soft Trap Test
    CPU Softint Reg and Int Test

All Basic MMU Tests
    DMMU Primary Context Reg Test
    DMMU Secondary Context Reg Test
    DMMU TSB Reg Test
    DMMU Tag Access Reg Test
    DMMU VA Watchpoint Reg Test
    DMMU PA Watchpoint Reg Test
    IMMU TSB Reg Test
    IMMU Tag Access Reg Test

All Basic Cache Tests
    Dcache RAM Test
    Dcache Tag Test
    Icache RAM Test
CODE EXAMPLE 3-1  diag-level Variable Set to max (Continued)

Power On Selftest Completed
  Icache Tag Test
  Icache Next Test
  Icache Predecode Test

Sabre MCU Control & Status Regs Init and Tests
  Init Sabre MCU Control & Status Regs
  Initializing SC registers in SabreIO

Memory Probe and Init
  Probe Memory
    INFO:  256MB Bank 0
    bank 2:  0MB
    frequency = 301, refvalue = 146, no_of_banks = 1
    INFO:  MC0 = 0x00000000.80001192, MC1 = 0x00000000.0c4aab14

  Malloc Post Memory
  Memory Addr w/ Ecache
  Load Post In Memory
  Run POST from MEM

...........

  loaded POST in memory
  Map PROM/STACK/NVRAM in DMMU
  Update Master Stack/Frame Pointers

All FPU Basic Tests
  FPU Regs Test
  FPU Move Regs Test
  FPU State Reg Test
  FPU Functional Test
  FPU Trap Test

UPA Data Bus Line Test

Memory Tests
  Init Memory
    INFO:  256MB at bank 0 stack 0 (2 dimms per bank)

.........................................................

.........................................................

INFO:  0MB at bank 0 stack 1
INFO:  0MB at bank 2 stack 0
INFO:  0MB at bank 2 stack 1

Memory Addr w/ Ecache Test
INFO:  256MB at bank 0 stack 0 (2 dimms per bank)
INFO:  0MB at bank 0 stack 1
INFO:  0MB at bank 2 stack 0
INFO:  0MB at bank 2 stack 1

ECC Memory Addr Test
INFO:  256MB at bank 0 stack 0 (2 dimms per bank)
INFO:  0MB at bank 0 stack 1
INFO:  0MB at bank 2 stack 0
INFO:  0MB at bank 2 stack 1

Block Memory Addr Test
Power On Selftest Completed
INFO: 256MB at bank 0 stack 0 (2 dimms per bank)
INFO: 0MB at bank 0 stack 1
INFO: 0MB at bank 2 stack 0
INFO: 0MB at bank 2 stack 1
Block Memory Test
INFO: 256MB at bank 0 stack 0 (2 dimms per bank)
Write 0x33333333.33333333
................................................................
................................................................
Read
................................................................
................................................................
Write 0x55555555.55555555
................................................................
................................................................
Read
................................................................
................................................................
Write 0xcccccccc.cccccccc
................................................................
................................................................
Read
................................................................
................................................................
Write 0xaaaaaaaa.aaaaaaaa
................................................................
................................................................
Read
................................................................
................................................................
INFO: 0MB at bank 0 stack 1
INFO: 0MB at bank 2 stack 0
INFO: 0MB at bank 2 stack 1
ECC Blk Memory Test
INFO: 256MB at bank 0 stack 0 (2 dimms per bank)
Write 0xa5a5a5a5.a5a5a5a5
................................................................
................................................................
Read
................................................................
................................................................
Write 0x96969696.96969696
................................................................
................................................................
CODE EXAMPLE 3-1  diag-level Variable Set to max (Continued)
CODE EXAMPLE 3-1  diag-level Variable Set to max (Continued)

Power On Selftest Completed
Read
...........................................................................................
...........................................................................................
Write 0xbbbbbbbb.bbbbbbbb
...........................................................................................
...........................................................................................
Read
...........................................................................................
...........................................................................................
Write 0xdddddddd.dddddddd
...........................................................................................
...........................................................................................
Read
...........................................................................................
...........................................................................................

INFO:  0MB at bank 0 stack 1
INFO:  0MB at bank 2 stack 0
INFO:  0MB at bank 2 stack 1

All Basic Sabre MMU Tests
  Init Sabre
  PIO Decoder and BCT Test
  PCI Byte Enable Test
  Interrupt Map (short) Reg Test
  Interrupt Set/Clr Reg Test
  Sabre IOMMU Regs Test
  Sabre IOMMU RAM Address Test
  Sabre IOMMU CAM Address Test
  IOMMU TLB Compare Test
  IOMMU TLB Flush Test
  PBMA PCI Config Space Regs Test
  PBMA Control/Status Reg Test
  PBMA Diag Reg Test
  Sabre IO Regs Test

All Advanced CPU Tests
  DMMU Hit/Miss Test
  IMMU Hit/Miss Test
  DMMU Little Endian Test
  IU ASI Access Test
  FP O ASI Access Test
  Ecache Thrash Test

All CPU Error Reporting Tests
  CPU Data Access Trap Test
  CPU Addr Align Trap Test
  DMMU Access Priv Page Test
Power On Selftest Completed
DMMU Write Protected Page Test
All Advanced Sabre IOMMU Tests
  Init Sabre
  Consist DMA Rd, IOMMU miss Ebus Test
  Consist DMA Rd, IOMMU hit Ebus Test
  Consist DMA Wr, IOMMU miss Ebus Test
  Consist DMA Wr, IOMMU hit Ebus Test
  Pass-Thru DMA Rd, Ebus device Test
  Pass-Thru DMA Wr, Ebus device Test
  Consist DMA Rd, IOMMU LRU Lock Ebus Test
  Consist DMA Wr, IOMMU LRU Locked Ebus Test
All Basic Cheerio Tests
  Cheerio Ebus PCI Config Space Test
  Cheerio Ethernet PCI Config Space Test
  Cheerio Init
All Sabre IOMMU Error Reporting Tests
  Init Sabre
  PIO Read, Master Abort Test
  PIO Read, Target Abort Test

Status of this POST run: PASS
manufacturing mode=OFF
Time Stamp [hour:min:sec] 00:02:01  [month/date year] 08/22 1997

Power On Selftest Completed
Software Power ON0.0000.0000.0000 ffff.ffff.f00b.4100
0002.3333.0200.001b

@(#) Sun Ultra 5/10 UPA/PCI 3.9 P2.1 Version 9 created 1997/08/05 16:24
Clearing E$ Tags Done
Clearing I/D TLBs Done
Probing Memory Done
MEM BASE = 0000.0000.0000.0000
MEM SIZE = 0000.0000.1000.0000
11-Column Mode Enabled
MMUs ON
Copy Done
PC = 0000.01ff.f000.20ec
PC = 0000.0000.0000.2130
Decompressing into Memory Done
Size = 0000.0000.0007.5300

CODE EXAMPLE 3-1  diag-level Variable Set to max (Continued)
TTYa initialized
Reset Control: BXIR:0 BPOR:0 SXIR:0 SPOR:1 POR:0
UltraSPARC-IIi 2-2 module
Probing Memory Bank #0 128 + 128 : 256 Megabytes
Probing Memory Bank #2 0 + 0 : 0 Megabytes
Probing Floppy: drive detected on ID0
Probing EBUS SUNW,CS4231
Probing UPA Slot at 1e,0 SUNW,ffb
Probing /pci01f,0/pci01,1 at Device 2 SUNW,m64B
Probing /pci01f,0/pci01,1 at Device 3 ide disk cdrom
Probing /pci01f,0/pci01 at Device 1 Nothing there
Probing /pci01f,0/pci01 at Device 2 Nothing there
Probing /pci01f,0/pci01 at Device 3 Nothing there
Probing /pci01f,0/pci01 at Device 4 Nothing there
Reset Control: BXIR:0 BPOR:0 SXIR:0 SPOR:1 POR:0
UltraSPARC-IIi 2-2 module
Probing Memory Bank #0 128 + 128 : 256 Megabytes
Probing Memory Bank #2 0 + 0 : 0 Megabytes
Probing Floppy: drive detected on ID0
Probing EBUS SUNW,CS4231
Probing UPA Slot at 1e,0 SUNW,ffb
Probing /pci01f,0/pci01,1 at Device 2 SUNW,m64B
Probing /pci01f,0/pci01,1 at Device 3 ide disk cdrom
Probing /pci01f,0/pci01 at Device 1 Nothing there
Probing /pci01f,0/pci01 at Device 2 Nothing there
Probing /pci01f,0/pci01 at Device 3 Nothing there
Probing /pci01f,0/pci01 at Device 4 Nothing there

Sun Ultra 5/10 UPA/PCI (UltraSPARC-IiI 300MHz), No Keyboard
OpenBoot 3.9 P2.1 , 256 MB memory installed, Serial #9337477.
Ethernet address 8:0:20:8e:7a:85, Host ID: 8087a85.

ok
3.4.2 diag-level Variable Set to min

When you set the diag-level variable to min, POST enables an abbreviated set of diagnostic-level tests. This mode requires approximately one minute to complete (with 128 Mbytes of DIMM installed). CODE EXAMPLE 3-2 shows a serial port A POST output with diag-level set to min.

**Note** – Video output is disabled while POST is initialized.

**CODE EXAMPLE 3-2**   diag-level Variable Set to min

```
@(#) Sun Ultra 5/10 UPA/PCI 3.9 P2.1 Version 9 created 1997/08/05 16:24
Probing keyboard Done
%o0 = 0000.0000.0000.2001

Executing Power On SelfTest

@(#) Sun Ultra 5/10 (Darwin) POST 2.1.1 (Build No. 293) 08/21/97: 15:59

CPU: UltraSPARC-LC (MHz: 301 Ecache Size: 512KB)

Init POST BSS
   Init System BSS
NVRAM
   NVRAM Battery Detect Test
   NVRAM Scratch Addr Test
   NVRAM Scratch Data Test
DMMU TLB Tags
   DMMU TLB Tag Access Test
DMMU TLB RAM
   DMMU TLB RAM Access Test
Probe Ecache
   Probe Ecache
Ecach  e Tests
   Ecach  e RAM Addr Test
   Ecach  e Tag Addr Test
All CPU Basic Tests
   V9 Instruction Test
   CPU Soft Trap Test
   CPU Softint Reg and Int Test
All Basic MMU Tests
   DMMU Primary Context Reg Test
   DMMU Secondary Context Reg Test
```
### CODE EXAMPLE 3-2

<table>
<thead>
<tr>
<th>diag-level Variable Set to min (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>@(#) Sun Ultra 5/10 UPA/PCI 3.9 P2.1 Version 9 created 1997/08/05 16:24</td>
</tr>
<tr>
<td>DMMU TSB Reg Test</td>
</tr>
<tr>
<td>IMMU TSB Reg Test</td>
</tr>
<tr>
<td>All Basic Cache Tests</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Sabre MCU Control &amp; Status Regs Init and Tests</td>
</tr>
<tr>
<td>Init Sabre MCU Control &amp; Status Regs</td>
</tr>
<tr>
<td>Initializing SC registers in SabreIO</td>
</tr>
<tr>
<td>Memory Probe and Init</td>
</tr>
<tr>
<td>INFO:</td>
</tr>
<tr>
<td>bank 2: frequency = 301, refvalue = 146, no_of_banks = 1</td>
</tr>
<tr>
<td>INFO: MCD = 0x00000000.80000192, MC1 = 0x00000000.0c4aab14</td>
</tr>
<tr>
<td>Malloc Post Memory</td>
</tr>
<tr>
<td>Load Post In Memory</td>
</tr>
<tr>
<td>..................</td>
</tr>
<tr>
<td>Map PROM/STACK/NVRAM in DMMU</td>
</tr>
<tr>
<td>All FPU Basic Tests</td>
</tr>
<tr>
<td>FPU Move Regs Test</td>
</tr>
<tr>
<td>Memory Tests</td>
</tr>
<tr>
<td>INFO:</td>
</tr>
<tr>
<td>........................................................</td>
</tr>
<tr>
<td>INFO:</td>
</tr>
<tr>
<td>INFO:</td>
</tr>
<tr>
<td>INFO:</td>
</tr>
<tr>
<td>ECC Memory Addr Test</td>
</tr>
<tr>
<td>INFO:</td>
</tr>
<tr>
<td>INFO:</td>
</tr>
<tr>
<td>INFO:</td>
</tr>
<tr>
<td>All Basic Sabre MMU Tests</td>
</tr>
</tbody>
</table>

---

3-16   Sun Ultra 10 Service Manual • February 2000
Chapter 3 Power-On Self-Test

CODE EXAMPLE 3-2  diag-level Variable Set to min (Continued)

@(#) Sun Ultra 5/10 UPA/PCI  3.9 P2.1  Version 9 created 1997/08/05 16:24

Interrupt Map (short) Reg Test
Interrupt Set/Clr Reg Test
Sabre IOMMU Regs Test
Sabre IOMMU RAM Address Test
Sabre IOMMU CAM Address Test
PBMA PCI Config Space Regs Test
PBMA Control/Status Reg Test
PBMA Diag Reg Test
Sabre IO Regs Test
All Advanced CPU Tests
  IU ASI Access Test
  FPU ASI Access Test
All CPU Error Reporting Tests
  CPU Data Access Trap Test
  CPU Addr Align Trap Test
  DMMU Access Priv Page Test
  DMMU Write Protected Page Test
All Advanced Sabre IOMMU Tests
  Init Sabre
  Consist DMA Rd, IOMMU miss Ebus Test
All Basic Cheerio Tests
  Cheerio Ebus PCI Config Space Test
  Cheerio Ethernet PCI Config Space Test
  Cheerio Init
All Sabre IOMMU Error Reporting Tests
  Init Sabre
  PIO Read, Master Abort Test
  PIO Read, Target Abort Test

Status of this POST run: PASS
manufacturing mode=OFF

Power On Selftest Completed
Software Power ON0.0000.0000.0000 ffff.ffff.f00b.4100
0002.3333.0200.001b

@(#) Sun Ultra 5/10 UPA/PCI  3.9 P2.1  Version 9 created 1997/08/05 16:24
Clearing E$ Tags  Done
Clearing I/D TLBs Done
Probing Memory Done
MEM BASE = 0000.0000.0000.0000
MEM SIZE = 0000.0000.1000.0000
11-Column Mode Enabled
MMUs ON
Copy Done
PC = 0000.01ff.f000.20ec
PC = 0000.0000.0000.2130
Decompressing into Memory Done
Size = 0000.0000.0007.5300
ttya initialized
Reset Control: BXIR:0 BPOR:0 SXIR:0 SPOR:1 POR:0
UltraSPARC-IIi 2-2 module
Probing Memory Bank #0 128 + 128 : 256 Megabytes
Probing Memory Bank #2 0 + 0 : 0 Megabytes
Probing Floppy: drive detected on ID0
Probing EBUS SUNW,CS4231
Probing UPA Slot at 1e,0 SUNW,ffb
Probing /pci@1f,0/pci@1,1 at Device 2 SUNW,m64B
Probing /pci@1f,0/pci@1,1 at Device 3 ide disk cdrom
Probing /pci@1f,0/pci@1 at Device 1 Nothing there
Probing /pci@1f,0/pci@1 at Device 2 Nothing there
Probing /pci@1f,0/pci@1 at Device 3 Nothing there
Probing /pci@1f,0/pci@1 at Device 4 Nothing there
Reset Control: BXIR:0 BPOR:0 SXIR:0 SPOR:1 POR:0
UltraSPARC-IIi 2-2 module
Probing Memory Bank #0 128 + 128 : 256 Megabytes
Probing Memory Bank #2 0 + 0 : 0 Megabytes
Probing Floppy: drive detected on ID0
Probing EBUS SUNW,CS4231
Probing UPA Slot at 1e,0 SUNW,ffb
Probing /pci@1f,0/pci@1,1 at Device 2 SUNW,m64B
Probing /pci@1f,0/pci@1,1 at Device 3 ide disk cdrom
Probing /pci@1f,0/pci@1 at Device 1 Nothing there
Probing /pci@1f,0/pci@1 at Device 2 Nothing there
Probing /pci@1f,0/pci@1 at Device 3 Nothing there
Probing /pci@1f,0/pci@1 at Device 4 Nothing there

Sun Ultra 5/10 UPA/PCI (UltraSPARC-IIi 300MHz), No Keyboard
OpenBoot 3.9 P2.1 , 256 MB memory installed, Serial #9337477.
Ethernet address 8:0:20:8e:7a:85, Host ID: 808e7a85.

ok
3.4.3 POST Progress and Error Reporting

When POST is initialized, the Caps Lock key on the Sun Type-5 or Type-6 keyboard flashes on and off to indicate that POST is active (see FIGURE 3-2 or FIGURE 3-3). Additional POST progress indications are also visible when a TTY-type terminal or a TIP line is connected between serial port A (default port) of the tested system and a second Sun workstation.

If an error occurs during POST execution, the keyboard Caps Lock key indicator stops flashing and an error code pattern is indicated using the Caps Lock, Compose, Scroll Lock, and Num Lock key indicators (see FIGURE 3-2 or FIGURE 3-3). The error code pattern indicates a particular system hardware failure. If a keyboard error code pattern is displayed, determine the meaning of the pattern by using TABLE 3-1.

Note – An error code might be visible for only a few seconds. Observe the Caps Lock, Compose, Scroll Lock, and Num Lock key indicators closely while POST is active.

<table>
<thead>
<tr>
<th>Caps Lock</th>
<th>Compose</th>
<th>Scroll Lock</th>
<th>Num Lock</th>
<th>Bit Value</th>
<th>Meaning of Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>Blink</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>x000(2)</td>
<td>POST in progress</td>
</tr>
<tr>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>0000(2)</td>
<td>POST successfully completed</td>
</tr>
<tr>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>1001(2)</td>
<td>System board failed</td>
</tr>
<tr>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>1010(2)</td>
<td>No memory found</td>
</tr>
<tr>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>1011(2)</td>
<td>Reserved</td>
</tr>
<tr>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>1100(2)</td>
<td>Reserved</td>
</tr>
<tr>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>1101(2)</td>
<td>Reserved</td>
</tr>
<tr>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>1110(2)</td>
<td>Bad CPU</td>
</tr>
<tr>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>1111(2)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

In most cases, POST also attempts to send a failure message to the POST monitoring system. CODE EXAMPLE 3-3 shows the typical appearance of an error message.
**Note** – The system does not automatically boot if a POST error occurs; it halts at the `ok` prompt to indicate a failure.

### CODE EXAMPLE 3-3  Typical Error Code Failure Message

```markdown
@@(#) Sun Ultra 5/10 UPA/PCI 3.9 P2.1 Version 9 created 1997/08/05 16:24
Probing keyboard Done
%0 = 0000.0000.0000.2001

Executing Power On SelfTest

@@(#) Sun Ultra 5/10 (Darwin) POST 2.1.1 (Build No. 293) 08/21/97: 15:59

CPU: UltraSPARC-LC (MHz: 301 Ecache Size: 512KB)

Init POST BSS
  Init System BSS
NVRAM
  NVRAM Battery Detect Test
  NVRAM Scratch Addr Test
  NVRAM Scratch Data Test
DMMU TLB Tags
  DMMU TLB Tag Access Test
DMMU TLB RAM
  DMMU TLB RAM Access Test
Probe Ecache
  Probe Ecache
Ecache Tests
  Ecache RAM Addr Test
  Ecache Tag Addr Test
All CPU Basic Tests
  V9 Instruction Test
  CPU Soft Trap Test
  CPU Softint Reg and Int Test
All Basic MMU Tests
  DMMU Primary Context Reg Test
  DMMU Secondary Context Reg Test
  DMMU TSB Reg Test
  DMMU Tag Access Reg Test
  IMMU TSB Reg Test
  IMMU Tag Access Reg Test
All Basic Cache Tests
  Dcache RAM Test
```
CODE EXAMPLE 3-3  Typical Error Code Failure Message (Continued)

```plaintext
@(#) Sun Ultra 5/10 UPA/PCI 3.9 P2.1 Version 9 created 1997/08/05 16:24
Icache RAM Test
Sabre MCU Control & Status Regs Init and Tests
  Init Sabre MCU Control & Status Regs
  Initializing SC registers in SabreIO
Memory Probe and Init
  Probe Memory
    INFO: All the memory banks in 10 bit column mode
    INFO: 32MB Bank 0
    frequency = 301, refvalue = 73, no_of_banks = 2
    INFO: MC0 = 0x00000000.80000549, MC1 = 0x00000000.0c4aab14
  Malloc Post Memory
  Memory Addr w/ Ecache
  Load Post In Memory
  Run POST from MEM
  .........
  loaded POST in memory
  Map PROM/STACK/NVRAM in DMMU
  Update Master Stack/Frame Pointers
All FPU Basic Tests
  FPU Regs Test
  FPU Move Regs Test
UPA Data Bus Line Test
Memory Tests
  Init Memory
    INFO: 32MB at bank 0 stack 0 (2 dimms per bank)
  .................
    INFO: 0MB at bank 0 stack 1
    ERROR: DIMM Undetected on some sockets on the board!
    ERROR: DIMM Undetected on some sockets on the board!
ECC Memory Addr Test
    INFO: 32MB at bank 0 stack 0 (2 dimms per bank)
    INFO: 0MB at bank 0 stack 1
    ERROR: DIMM Undetected on some sockets on the board!
    ERROR: DIMM Undetected on some sockets on the board!
```

Chapter 3    Power-On Self-Test  3-21
3.5  Bypassing POST

To bypass POST:

1. Prior to powering on the system, press and hold the Stop key on the keyboard (FIGURE 3-2 or FIGURE 3-3).

2. With the Stop key held down, turn on the system by pressing the Standby (Power) key.

   **Note** – Press and hold the Stop key for approximately 5 seconds.

3.6  Resetting Variables to Default Settings

To set the system NVRAM parameters to the original default settings:

1. Press and hold the Stop and N keys while powering on the system (FIGURE 3-2 or FIGURE 3-3).

2. Continue to hold the Stop and N keys until the system banner displays on the monitor.
3.7 Initializing Motherboard POST

To initialize the motherboard POST:

1. **Power off the system.**

2. Simultaneously press and hold the Stop and D keys, then press the Standby (Power) key (FIGURE 3-2 or FIGURE 3-3).

   **Note** – Video output is disabled while motherboard POST is initialized.

   **Note** – To view the POST output results, you must set up a TIP connection. See Section 3.2.1 “Setting Up a TIP Connection” on page 3-2.

3. Verify the keyboard Caps Lock key LED flashes on and off to indicate the system has enabled POST.

4. If a failure occurs during POST, a keyboard key LED other than the Caps Lock key LED might light, indicating a failed system component.
   
   See Section 3.4.3 “POST Progress and Error Reporting” on page 3-19.

   **Note** – The most probable cause of this type of failure is the motherboard. However, optional system components could also cause POST to fail.

5. Before replacing the motherboard, remove any optional components, such as PCI cards, then repeat the POST.

   **Note** – Non-optional components such as DIMMs, the motherboard, the power supply, and the keyboard must be installed for POST to execute properly. Removing the optional system components and retesting the system isolates the possibility that those components are the cause of the failure.
Troubleshooting Procedures

This chapter describes how to troubleshoot possible hardware problems and includes suggested corrective actions.

This chapter contains the following topics:

- Section 4.1 “Power-On Failure” on page 4-2
- Section 4.2 “Video Output Failure” on page 4-3
- Section 4.3 “Hard Drive or CD-ROM Drive Failure” on page 4-4
- Section 4.4 “Power Supply Test” on page 4-5
- Section 4.5 “DIMM Failure” on page 4-7
- Section 4.6 “OpenBoot PROM On-Board Diagnostics” on page 4-8
- Section 4.7 “OpenBoot Diagnostics” on page 4-13
4.1 Power-On Failure

This section provides examples of power-on failure symptoms and suggested actions. Perform the suggested actions until you isolate the problem.

Symptom 1
The system does not power on when you press the keyboard Standby (Power).

Actions
1. Check the keyboard connection to ensure that the keyboard is properly connected to the system.
2. Check the power cord to ensure that it is properly connected to the system and to the wall receptacle.
3. Verify that the system power switch is set to on.
4. Verify that the wall receptacle is supplying power to the system.
5. Check the voltage-line select switch to ensure that it is set correctly.
6. Press the front panel standby switch. If the system powers on, the keyboard might be defective or the system might be unable to accept the keyboard power-on signal.
7. Power off the system (if necessary) and press the keyboard Standby (Power) key again. If the system powers on, no further action is required. If the system does not power on, the CPU module might not be correctly seated.
8. Inspect the CPU module to ensure correct seating.
9. Press the keyboard Standby (Power) key again. If the system powers on, no further action is required. If the system does not power on, the keyboard might be defective.
10. Connect a spare Sun Type-5 or Sun I/O Type-6 keyboard to the system and press the Standby (Power) key.
11. If the system still does not power up, the system power supply might be defective. See Section 4.4 “Power Supply Test” on page 4-5.
Symptom 2
The system attempts to power on but does not boot or initialize the monitor.

Actions

1. Press the keyboard Standby (Power) key and watch the keyboard. The keyboard LEDs should light briefly and you should hear a tone from the keyboard.

2. If you do not hear a keyboard tone or if the keyboard LEDs do not light briefly, the system power supply may be defective. See Section 4.4 “Power Supply Test” on page 4-5.

3. If a you hear a keyboard tone and the keyboard LEDs light briefly but the system still fails to initialize, see Section 3.7 “Initializing Motherboard POST” on page 3-23.

4.2 Video Output Failure

This section provides video output failure symptoms and suggested actions. Perform the suggested actions until you isolate the problem.

Symptom
The video does not display at the system monitor.

Actions

1. Check the monitor power cord to ensure that the cord is connected to the monitor and to the wall receptacle.

2. Verify that the wall receptacle is supplying power to the monitor.

3. Check the video cable connection between the monitor and the motherboard video output connector.

4. Check that the CPU module is properly seated.

5. If video still does not display on the monitor, the monitor, graphics card, or motherboard video chip may be defective.
4.3 Hard Drive or CD-ROM Drive Failure

This section provides hard drive and CD-ROM drive failure symptoms and suggested actions. Perform the suggested actions until you isolate the problem.

**Symptoms**
- A hard drive read, write, or parity error is reported by the operating system or a customer application.
- A CD-ROM drive read error or parity error is reported by the operating system or a customer application.

**Action**
- Replace the drive indicated by the failure message. The operating system identifies the internal drives as shown in TABLE 4-1.

**TABLE 4-1 Internal Drives Identification**

<table>
<thead>
<tr>
<th>Operating Environment Address</th>
<th>Drive Physical Location and Target</th>
</tr>
</thead>
<tbody>
<tr>
<td>c0t0d0s#</td>
<td>Master (primary) hard drive, target 0</td>
</tr>
<tr>
<td>c0t1d0s#</td>
<td>Slave (secondary) hard drive, target 1 (optional)</td>
</tr>
<tr>
<td>c0t6d0s#</td>
<td>CD-ROM drive, target 6 (optional)</td>
</tr>
</tbody>
</table>

*Note* – The # symbol in the operating system address examples may be a numeral between 0 and 7 that describes the slice or partition on the drive.

**Symptom**
Hard drive or CD-ROM drive fails to respond to commands.

**Action**
Test the drive response to the `probe-ide` command as follows:

1. To bypass POST, **type** `setenv diag-switch? false` **at the ok prompt.**
2. **At the system ok prompt, type:**

   ```
   ok% reset-all
   ok% probe-ide
   ```
If the hard drive responds correctly to `probe-ide` command, the message shown in CODE EXAMPLE 4-4 on page 4-10 is displayed, which means that the system EIDE controller has successfully probed the device. This is an indication that the motherboard is operating correctly.

- If an optional hard drive is installed and one drive does not respond to the EIDE controller probe but the other does, replace the unresponsive drive.
- If the `probe-ide` test fails to show the device in the message, replace the drive (see Section 7.2.2 “Replacing a Hard Drive” on page 7-6). If replacing the hard drive does not correct the problem, replace the motherboard.

### 4.4 Power Supply Test

The section describes how to test the power supply. FIGURE 4-1 and TABLE 4-2 describe power supply connector J17.

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

2. Remove the PCI card from riser board connector 2 (adjacent to the power supply), if necessary for clearance. Disconnect the ribbon cables from the motherboard to expose connectors J17.

3. Power on the system.
   See Section 10.2 “Powering On the System” on page 10-3.

   **Caution** – With the system cover removed and the system powered on, there is unprotected access to voltage and energy levels that are potentially hazardous to equipment and personnel. If you are unsure how to safely proceed, please seek the assistance of qualified service personnel.

4. Using a digital voltage meter (DVM), check the power supply output voltages as follows:

   **Note** – Power supply connector J17 must remain connected to the motherboard.

   a. With the negative probe of the DVM placed on a connector ground (Gnd) pin, position the positive probe on each power pin.

   b. Verify voltage and signal availability as listed in TABLE 4-2.

5. If any power pin signal is not present with the power supply active and properly connected to the motherboard, replace the power supply.
**FIGURE 4-1**  Power Supply Connector J17 Pin Configuration

**TABLE 4-2**  Power Supply Connector J17 Pin Assignments

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+3.3V</td>
<td>+3.3 VDC</td>
</tr>
<tr>
<td>2</td>
<td>+3.3V</td>
<td>+3.3 VDC</td>
</tr>
<tr>
<td>3</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>4</td>
<td>+5V</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>5</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>6</td>
<td>+5V</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>7</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>8</td>
<td>PWR_OK</td>
<td>Power okay</td>
</tr>
<tr>
<td>9</td>
<td>5VSB</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>+12V</td>
<td>+12 VDC</td>
</tr>
<tr>
<td>11</td>
<td>+3.3V</td>
<td>+3.3 VDC</td>
</tr>
<tr>
<td>12</td>
<td>-12V</td>
<td>-12 VDC</td>
</tr>
<tr>
<td>13</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>14</td>
<td>PS_ON</td>
<td>Power supply on</td>
</tr>
<tr>
<td>15</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>16</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>17</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
</tbody>
</table>
6. After you finish testing the power supply, remove the wrist strap, replace the system cover, and power on the system as described in Chapter 10.

4.5 DIMM Failure

At times, the operating environment, diagnostic program, or POST might not display a DIMM location (U number) as part of a memory error message. In this situation, the only available information is a physical memory address and failing byte (or bit). The following table lists physical memory addresses that can be used to locate a defective DIMM.

<table>
<thead>
<tr>
<th>DIMM Slot</th>
<th>DIMM Pair  (non-interleave)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIMM0</td>
<td>00000000 - 0xffffffff</td>
</tr>
<tr>
<td>DIMM1</td>
<td></td>
</tr>
<tr>
<td>DIMM2</td>
<td>10000000 - 1xffffffff</td>
</tr>
<tr>
<td>DIMM3</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TABLE 4-2 Power Supply Connector J17 Pin Assignments (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin</td>
</tr>
<tr>
<td>-----</td>
</tr>
<tr>
<td>18</td>
</tr>
<tr>
<td>19</td>
</tr>
<tr>
<td>20</td>
</tr>
</tbody>
</table>
4.6 OpenBoot PROM On-Board Diagnostics

The following sections describe the OpenBoot PROM (OBP) on-board diagnostics. To execute the OBP on-board diagnostics, the system must be at the ok prompt. The OBP on-board diagnostics are described as follows:

- Section 4.6.1 “Watch-Clock Diagnostic” on page 4-8
- Section 4.6.2 “Watch-Net and Watch-Net-All Diagnostics” on page 4-8
- Section 4.6.3 “Probe-IDE Diagnostic” on page 4-10
- Section 4.6.4 “Test device alias, device path, -All Diagnostic” on page 4-10
- Section 4.6.5 “UPA Graphics Card” on page 4-12

4.6.1 Watch-Clock Diagnostic

The watch-clock diagnostic reads a register in the NVRAM/TOD chip and displays the result as a seconds counter. During normal operation, the seconds counter repeatedly increments from 0 to 59 until interrupted by pressing any key on the Sun keyboard. The watch-clock diagnostic is initialized by typing the watch-clock command at the ok prompt. The following code example identifies the watch-clock diagnostic output message.

**CODE EXAMPLE 4-1** Watch-Clock Diagnostic Output Message

```
ok watch-clock
Watching the 'seconds' register of the real time clock chip.
It should be 'ticking' once a second.
Type any key to stop.
49
ok
```

4.6.2 Watch-Net and Watch-Net-All Diagnostics

The watch-net and watch-net-all diagnostics monitor Ethernet packets on the Ethernet interfaces connected to the system. Good packets received by the system are indicated by a period (.). Errors such as the framing error and the cyclic redundancy check (CRC) error are indicated with an “X” and an associated error description. The watch-net diagnostic is initialized by typing the watch-net command at the ok prompt and the watch-net-all diagnostic is initialized by typing...
the `watch-net-all` command at the `ok` prompt. The following code example identifies the `watch-net` diagnostic output message. CODE EXAMPLE 4-3 identifies the `watch-net-all` diagnostic output message.

**CODE EXAMPLE 4-2**  Watch-Net Diagnostic Output Message

```plaintext
ok watch-net
Hme register test --- succeeded.
Internal loopback test -- succeeded.
Transceiver check -- Using Onboard Transceiver - Link Up.
passed
Using Onboard Transceiver - Link Up.
Looking for Ethernet Packets.
',.' is a Good Packet. 'X' is a Bad Packet.
Type any key to stop.
..................................................
................................................................
................................................................
........................................................
answered
ok
```

**CODE EXAMPLE 4-3**  Watch-Net-All Diagnostic Output Message

```plaintext
ok watch-net-all
 pci@1f,0/pci@1,1/network@1,1
Hme register test --- succeeded.
Internal loopback test -- succeeded.
Transceiver check -- Using Onboard Transceiver - Link Up.
passed
Using Onboard Transceiver - Link Up.
Looking for Ethernet Packets.
',.' is a Good Packet. 'X' is a Bad Packet.
Type any key to stop.
........
................................................................
................................................................
....................................
answered
ok
```
4.6.3 Probe-IDE Diagnostic

The probe-ide diagnostic transmits an inquiry command to internal and external IDE devices connected to the system's on-board IDE interface. If the IDE device is connected and active, the target address, unit number, device type, and manufacturer name are displayed. Initialize the probe-ide diagnostic by typing the probe-ide command at the ok prompt. The following code example identifies the probe-ide diagnostic output message.

CODE EXAMPLE 4-4  Probe-IDE Diagnostic Output Message

<table>
<thead>
<tr>
<th>ok probe-ide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device 0 ( Primary Master )</td>
</tr>
<tr>
<td>ATA Model: ST34342A</td>
</tr>
<tr>
<td>Device 1 ( Primary Slave )</td>
</tr>
<tr>
<td>ATA Model: ST34342A</td>
</tr>
<tr>
<td>Device 2 ( Secondary Master )</td>
</tr>
<tr>
<td>Removable ATAPI Model: CRD-8160B</td>
</tr>
<tr>
<td>Device 3 ( Secondary Slave )</td>
</tr>
<tr>
<td>Removable ATAPI Model:</td>
</tr>
<tr>
<td>ok</td>
</tr>
</tbody>
</table>

4.6.4 Test device alias, device path, –All Diagnostic

The test diagnostic, when combined with a device alias or device path, enables a device self-test diagnostic program. If a device has no self-test program, the message No selftest method for device name is displayed. To enable the self-test program for a device, type the test command followed by the device alias or device path name.

The following code example identifies the test diagnostic output message. Test diagnostics are initialized by typing the test device alias or device path command at the ok prompt. TABLE 4-4 lists the types of tests that can be used, a brief description of each test, and preparation.
Note – The diskette drive (floppy) is selected as the test alias name example.

**CODE EXAMPLE 4-5**  Test Diagnostic Output Message

```
ok test floppy

Testing floppy disk system. A formatted disk should be in the drive.
Test succeeded.
ok
```

**TABLE 4-4**  Selected OBP On-Board Diagnostic Tests

<table>
<thead>
<tr>
<th>Type of Test</th>
<th>Description</th>
<th>Preparation</th>
</tr>
</thead>
<tbody>
<tr>
<td>test screen</td>
<td>Tests the system video graphics hardware and the monitor.</td>
<td>Diag-switch? NVRAM parameter must be true for the test to execute.</td>
</tr>
<tr>
<td>test floppy</td>
<td>Tests the diskette drive response to commands.</td>
<td>A formatted diskette must be inserted into the diskette drive.</td>
</tr>
<tr>
<td>test net</td>
<td>Performs an internal/external loopback test of the system auto-selected Ethernet interface.</td>
<td>An Ethernet cable must be attached to the system and to an Ethernet tap or hub.</td>
</tr>
<tr>
<td>test ttya</td>
<td>Outputs an alphanumeric test pattern on the system serial ports: ttya, serial port A; ttyb, serial port B</td>
<td>A terminal must be connected to the port being tested to observe the output.</td>
</tr>
<tr>
<td>test ttyb</td>
<td></td>
<td></td>
</tr>
<tr>
<td>test keyboard</td>
<td>Executes the keyboard selftest.</td>
<td>Four keyboard LEDs should flash once and a message should be displayed: Keyboard Present.</td>
</tr>
<tr>
<td>test -all</td>
<td>Sequentially tests system-configured devices containing selftest.</td>
<td>Tests are sequentially executed in device-tree order (viewed with the show-devs command).</td>
</tr>
</tbody>
</table>
4.6.5 UPA Graphics Card

The UPA graphics card contains a built-in diagnostic test that is enabled through the OBP. The UPA graphics card built-in diagnostic test verifies basic graphics functionality without rebooting the operating system software.

To execute the built-in diagnostic test, the system must be at the `ok` prompt.

To initialize the UPA graphics card diagnostic:

1. **At the `ok` prompt, type:**

   ```bash
   ok% setenv diag-switch? true
   diag-switch? = true
   ok% setenv diag-switch? true
   ```

2. **At the `ok` prompt, type:**

   ```bash
   ok% test screen
   Verifying Console Mode for Frame Buffer Board
   This will take a few minutes
   Verifying Frame Buffer Memory used for console mode
   This will take about two minutes
   FFB Frame Buffer functional test passed
   ok%
   ```

3. **When the UPA graphics card on-board diagnostics are completed, type:**

   ```bash
   ok% setenv diag-switch? false
   diag-switch? = false
   ```
4.7 OpenBoot Diagnostics

The OpenBoot diagnostic (OBDiag) is a menu-driven diagnostic tool that verifies:

- Internal I/O system
- Ethernet
- Keyboard
- Mouse
- Diskette drive (floppy)
- Parallel port
- Serial ports
- NVRAM
- Audio
- EIDE
- Video

OBDiag performs root-cause failure analysis on the referenced devices by testing internal registers, confirming subsystem integrity, and verifying device functionality.

Note – The OBDiag test result data captured in the following code examples represent the test result data that is output when the system being tested is connected to a remote shell window through a tip connection. When the system being tested is tested in a stand-alone configuration, the test result data may differ.

4.7.1 Starting the OBDiag Menu

1. At the ok prompt, type:

```
ok% setenv mfg-mode on
mfg-mode = on
```

2. At the ok prompt, type:

```
ok% setenv diag-switch? true
diag-switch? = true
```
3. At the `ok` prompt, type:

```
ok% setenv auto-boot? false
auto-boot? = false
```

4. At the `ok` prompt, type:

```
ok% reset-all
```

5. Verify that the platform resets, as shown in CODE EXAMPLE 4-6.

**CODE EXAMPLE 4-6**  Reset Verification

```
ok setenv mfg-mode on
mfg-mode = on
ok setenv diag-switch? true
diag-switch? = true
ok setenv auto-boot? false
auto-boot? = false
ok reset-all
Resetting...

Software Power ON

@(#) Sun Ultra 5/10 UPA/PCI 3.11 Version 9 created 1998/03/06
10:31
Clearing E$ Tags Done
Clearing I/D TLBs Done
Probing Memory Done
MEM BASE = 0000.0000.2000.0000
MEM SIZE = 0000.0000.1000.0000
11-Column Mode Enabled
MMUs ON
Copy Done
PC = 0000.01ff.f000.1ffc
PC = 0000.0000.0000.2040
Decompressing into Memory Done
Size = 0000.0000.0006.e160
ttya initialized
Reset Control: BXIR:0 BPOR:0 SXIR:0 SPOR:1 POR:0
UltraSPARC-IIi 2-2 module
Probing Memory Bank #0 256 + 256: 512 Megabytes
Probing Memory Bank #2 0 + 0: 0 Megabytes
Probing UPA Slot at 1e,0 SUNW,ffb
```
### CODE EXAMPLE 4-6  Reset Verification (Continued)

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI0/0</td>
<td>Memory Bank #0: 256 + 256: 512 Megabytes</td>
</tr>
<tr>
<td>PCI0/1</td>
<td>Memory Bank #2: 0 + 0: 0 Megabytes</td>
</tr>
<tr>
<td>PCI0/2</td>
<td>UltraSPARC-III 2-2 module</td>
</tr>
<tr>
<td>PCI0/3</td>
<td>Reset Control: BXIR:0 BPOR:0 SXIR:0 SPOR:1 POR:0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI0/0</td>
<td>UltraSPARC-III 2-2 module</td>
</tr>
<tr>
<td>PCI0/1</td>
<td>Reset Control: BXIR:0 BPOR:0 SXIR:0 SPOR:1 POR:0</td>
</tr>
<tr>
<td>PCI0/2</td>
<td>Memory Bank #2: 0 + 0: 0 Megabytes</td>
</tr>
<tr>
<td>PCI0/3</td>
<td>Memory Bank #0: 256 + 256: 512 Megabytes</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI0/0</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 0</td>
</tr>
<tr>
<td>PCI0/1</td>
<td>Probing /pci@0f,0/pci@0l,1 at Device 1 pci</td>
</tr>
<tr>
<td>PCI0/2</td>
<td>Probing /pci@0f,0/pci@0l,1 at Device 2 SUNW,m64B</td>
</tr>
<tr>
<td>PCI0/3</td>
<td>Probing /pci@0f,0/pci@0l,1 at Device 3 ide disk</td>
</tr>
<tr>
<td>PCI0/4</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 4</td>
</tr>
<tr>
<td>PCI0/5</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 5</td>
</tr>
<tr>
<td>PCI0/6</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 6</td>
</tr>
<tr>
<td>PCI0/7</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 7</td>
</tr>
<tr>
<td>PCI0/8</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 8</td>
</tr>
<tr>
<td>PCI0/9</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 9</td>
</tr>
<tr>
<td>PCI0/10</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device a</td>
</tr>
<tr>
<td>PCI0/11</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device b</td>
</tr>
<tr>
<td>PCI0/12</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device c</td>
</tr>
<tr>
<td>PCI0/13</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device d</td>
</tr>
<tr>
<td>PCI0/14</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device e</td>
</tr>
<tr>
<td>PCI0/15</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device f</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI0/0</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 0</td>
</tr>
<tr>
<td>PCI0/1</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 1</td>
</tr>
<tr>
<td>PCI0/2</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 2</td>
</tr>
<tr>
<td>PCI0/3</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 3</td>
</tr>
<tr>
<td>PCI0/4</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 4</td>
</tr>
<tr>
<td>PCI0/5</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 5</td>
</tr>
<tr>
<td>PCI0/6</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 6</td>
</tr>
<tr>
<td>PCI0/7</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 7</td>
</tr>
<tr>
<td>PCI0/8</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 8</td>
</tr>
<tr>
<td>PCI0/9</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device 9</td>
</tr>
<tr>
<td>PCI0/10</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device a</td>
</tr>
<tr>
<td>PCI0/11</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device b</td>
</tr>
<tr>
<td>PCI0/12</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device c</td>
</tr>
<tr>
<td>PCI0/13</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device d</td>
</tr>
<tr>
<td>PCI0/14</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device e</td>
</tr>
<tr>
<td>PCI0/15</td>
<td>Probing /pci@0f,0/pci@0l/pci@0l at Device f</td>
</tr>
</tbody>
</table>
6. At the `ok` prompt, type `obdiag`. Verify that the OBDiag menu is displayed, as shown in CODE EXAMPLE 4-7.

7. At the OBDiag menu prompt, type `16` to enable script-debug messages.

8. At the OBDiag menu prompt, type `18` to disable external loopback tests.

CODE EXAMPLE 4-6  Reset Verification (Continued)

```
Probing /pci@1f,0/pci@1/pci@1 at Device c Nothing there
Probing /pci@1f,0/pci@1/pci@1 at Device d Nothing there
Probing /pci@1f,0/pci@1/pci@1 at Device e Nothing there
Probing /pci@1f,0/pci@1/pci@1 at Device f Nothing there
Probing /pci@1f,0/pci@1 at Device 2 Nothing there
Probing /pci@1f,0/pci@1 at Device 3 Nothing there
Probing /pci@1f,0/pci@1 at Device 4 Nothing there

Sun Ultra 5/10 UPA/PCI (UltraSPARC-IIi 300MHz), No Keyboard
OpenBoot 3.11, 512 MB memory installed, Serial #9337777.
Ethernet address 8:0:20:8e:7b:b1, Host ID: 808e7bb1.

ok
```

CODE EXAMPLE 4-7  OBDiag Menu

```
ok obdiag
stdin: fffe2008
stdout: fffe2010
loading code into: /pci@1f,0/pci@1,1/ebus@1
loading code into: /pci@1f,0/pci@1,1/ebus@1/eeprom@14,0
loading code into: /pci@1f,0/pci@1,1/ebus@1/ecpp@14,3043bc
loading code into: /pci@1f,0/pci@1,1/ebus@1/su@14,3062f8
loading code into: /pci@1f,0/pci@1,1/ebus@1/se@14,400000
loading code into: /pci@1f,0/pci@1,1/network@1,1
loading code into: /pci@1f,0/pci@1,1/network@1,1
loading code into: /pci@1f,0/pci@1,1/ide0@3
loading code into: /pci@1f,0/pci@1,1/ide0@3/disk
loading code into: /pci@1f,0/pci@1,1/ide0@3/cdrom
loading code into: /pci@1f,0/pci@1,1/SUNW,m64B@2
Debugging enabled

OBDiag Menu
```
4.7.2 OB Diagnostics

The OBDiags are described in the following sections:

- Section 4.7.2.1 “PCI/PCIO Diagnostic” on page 4-18
- Section 4.7.2.2 “EBus DMA/TCR Registers Diagnostic” on page 4-19
- Section 4.7.2.3 “Ethernet Diagnostic” on page 4-19
- Section 4.7.2.4 “Keyboard Diagnostic” on page 4-20
- Section 4.7.2.5 “Mouse Diagnostic” on page 4-21
- Section 4.7.2.6 “Diskette Drive (Floppy) Diagnostic” on page 4-21
- Section 4.7.2.7 “Parallel Port Diagnostic” on page 4-22
- Section 4.7.2.8 “Serial Port A Diagnostic” on page 4-22
- Section 4.7.2.9 “Serial Port B Diagnostic” on page 4-24
- Section 4.7.2.10 “NVRAM Diagnostic” on page 4-25
- Section 4.7.2.11 “Audio Diagnostic” on page 4-25
- Section 4.7.2.12 “EIDE Diagnostic” on page 4-26
- Section 4.7.2.13 “Video Diagnostic” on page 4-26
- Section 4.7.2.14 “All Above Diagnostic” on page 4-27

CODE EXAMPLE 4-7  OBDiag Menu (Continued)

<table>
<thead>
<tr>
<th>0</th>
<th>PCI/PCIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EBus DMA/TCR Registers</td>
</tr>
<tr>
<td>2</td>
<td>Ethernet</td>
</tr>
<tr>
<td>3</td>
<td>Keyboard</td>
</tr>
<tr>
<td>4</td>
<td>Mouse</td>
</tr>
<tr>
<td>5</td>
<td>Floppy</td>
</tr>
<tr>
<td>6</td>
<td>Parallel Port</td>
</tr>
<tr>
<td>7</td>
<td>Serial Port A</td>
</tr>
<tr>
<td>8</td>
<td>Serial Port B</td>
</tr>
<tr>
<td>9</td>
<td>NVRAM</td>
</tr>
<tr>
<td>10</td>
<td>Audio</td>
</tr>
<tr>
<td>11</td>
<td>EIDE</td>
</tr>
<tr>
<td>12</td>
<td>Video</td>
</tr>
<tr>
<td>13</td>
<td>All Above</td>
</tr>
<tr>
<td>14</td>
<td>Quit</td>
</tr>
<tr>
<td>15</td>
<td>Display this Menu</td>
</tr>
<tr>
<td>16</td>
<td>Toggle script-debug</td>
</tr>
<tr>
<td>17</td>
<td>Enable External Loopback Tests</td>
</tr>
<tr>
<td>18</td>
<td>Disable External Loopback Tests</td>
</tr>
</tbody>
</table>

Enter (0-13 tests, 14 -Quit, 15 -Menu) ===>

Chapter 4  Troubleshooting Procedures  4-17
4.7.2.1 PCI/PCIO Diagnostic

To start the PCI/PCIO diagnostic, type 0 at the OBDiag menu prompt. The PCI/PCIO diagnostic performs the following:

1. **vendor_ID_test** – Verifies the PCIO ASIC vendor ID is 108e.
2. **device_ID_test** – Verifies the PCIO ASIC device ID is 1000.
3. **mixmode_read** – Verifies the PCI configuration space is accessible as half-word bytes by reading the EBus2 vendor ID address.
4. **e2_class_test** – Verifies the address class code. Address class codes include bridge device (0x B, 0x 6), other bridge device (0x A and 0x 80), and programmable interface (0x 9 and 0x 0).
5. **status_req_walk1** – Performs a walk-one test on the status register with mask 0x 280 (PCIO ASIC is accepting fast back-to-back transactions, DEVSEL timing is 0x 1).
6. **line_size_walk1** – Performs tests 1 through 5.
7. **latency_walk1** – Performs a walk-one test on the latency timer.
8. **line_walk1** – Performs a walk-one test on the interrupt line.
9. **pin_test** – Verifies the interrupt pin is logic-level high (1) after reset.

The following code example shows the PCI/PCIO output message.

**CODE EXAMPLE 4-8 PCI/PCIO Output Message**

```
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===>
0

TEST='all_pci/PCIO_test'
SUBTEST='vendor_id_test'
SUBTEST='device_id_test'
SUBTEST='mixmode_read'
SUBTEST='e2_class_test'
SUBTEST='status_req_walk1'
SUBTEST='line_size_walk1'
SUBTEST='latency_walk1'
SUBTEST='line_walk1'
SUBTEST='pin_test'
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===>
```
4.7.2.2 EBus DMA/TCR Registers Diagnostic

To start the DMA/TCR registers diagnostic, type 1 at the OBDiag menu prompt. The EBus DMA/TCR registers diagnostic performs the following:

1. dma_reg_test – Performs a walking-ones bit test for the control status register, address register, and byte-count register of each channel. Verifies the control status register is set properly.

2. dma_func-test – Validates the DMA capabilities and FIFOs. The test is executed in a DMA diagnostic loopback mode. Initializes the data of transmitting memory with its address, performs a DMA read and write, and verifies that the data received is correct. Repeats for four channels.

The following code example shows the EBus DMA/TCR registers output message.

CODE EXAMPLE 4-9 EBus DMA/TCR Registers Output Message

```
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===> 1
TEST='all_dma/ebus_test'
SUBTEST='dma_reg_test'
SUBTEST='dma_func_test'
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===> 
```

4.7.2.3 Ethernet Diagnostic

To start the Ethernet diagnostic, type 2 at the OBDiag menu prompt. The Ethernet diagnostic performs the following:

1. my_channel_reset – Resets the Ethernet channel.

2. hme_reg_test – Performs a walk-one test on the following registers set: global register 1, global register 2, bmac xif register, bmac tx register, and mif register.

3. MAC_internal_loopback_test – Performs an Ethernet channel engine internal loopback test.

4. 10_mb_xcvr_loopback_test – Enables the 10Base-T data present at the transmit MII data inputs, to be routed back to the receive MII data outputs.

5. 100_mb_phy_loopback_test – Enables MII transmit data to be routed to the MII receive data path.

6. 100_mb_twister_loopback_test – Forces the twisted-pair transceiver into loopback mode.
The following code example shows the Ethernet output message.

**CODE EXAMPLE 4-10 Ethernet Output Message**

```
Enter (0-13 tests, 14 -Quit, 15 -Menu) ===> 2

TEST='ethernet_test'
Using Onboard Transceiver - Link Up.
SUBTEST='my_channel_reset'
SUBTEST='hme_reg_test'
SUBTEST='global_reg1_test'
SUBTEST='global_reg2_test'
SUBTEST='bmac_xif_reg_test'
SUBTEST='bmac_tx_reg_test'
SUBTEST='mif_reg_test'
SUBTEST='mac_internal_loopback_test'
SUBTEST='10mb_xcvr_loopback_test'
SUBTEST='100mb_phy_loopback_test'
SUBTEST='100mb_twister_loopback_test'
Enter (0-13 tests, 14 -Quit, 15 -Menu) ===>
```

**4.7.2.4 Keyboard Diagnostic**

To start the keyboard diagnostic, type 3 at the OBDiag menu prompt. The keyboard diagnostic consists of an external and internal loopback test. The external loopback requires a passive loopback connector. The internal loopback verifies the keyboard port by transmitting and receiving 128 characters.

The following code example shows the keyboard output message.

**CODE EXAMPLE 4-11 Keyboard Output Message**

```
setenv Enter (0-13 tests, 14 -Quit, 15 -Menu) ===> 3

TEST='keyboard_test'
SUBTEST='internal_loopback'
Enter (0-13 tests, 14 -Quit, 15 -Menu) ===>
```
4.7.2.5 Mouse Diagnostic

To start the mouse diagnostic, type 4 at the OBDiag menu prompt. The mouse diagnostic performs a keyboard-to-mouse loopback test.

The following code example shows the mouse output message.

CODE EXAMPLE 4-12 Mouse Output Message

```
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===> 4

TEST='mouse_test'
SUBTEST='mouse_loopback'

###OBDIAG_MFG_START###
TEST='mouse_test'
STATUS='FAILED'
SUBTEST='mouse_loopback'
ERRORS='1'
TTF='1656'
SPEED='295.99 MHz'
PASSES='1'
MESSAGE='Error: Timeout receiving a character'
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===>
```

4.7.2.6 Diskette Drive (Floppy) Diagnostic

To start the diskette drive (floppy) diagnostic, type 5 at the OBDiag menu prompt. The floppy diagnostic verifies the diskette drive controller initialization. It also validates the status of a selected disk drive and reads the diskette drive header.

The following code example shows the floppy test output message.

CODE EXAMPLE 4-13 Floppy Output Message

```
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===> 5

TEST='floppy_test'
SUBTEST='floppy_id0_read_test'
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===>
```
4.7.2.7 Parallel Port Diagnostic

To start the parallel port diagnostic, type 6 at the OBDiag menu prompt. The parallel port diagnostic performs the following:

1. `sio-passive-lb` - Sets up the SuperIO configuration register to enable extended/compatible parallel port select, then does a write 0, walk-one, write 0 x ff to the data register. It verifies the results by reading the status register.

2. `dma_read` - Enables ECP mode, ECP DMA configuration, and FIFO test mode. Transfers 16 bytes of data from memory to the parallel port device and then verifies the data is in TFIFO.

The following code example shows the parallel port output message.

```
CODE EXAMPLE 4-14 Parallel Port Output Message

Enter (0-12 tests, 13 -Quit, 14 -Menu) ===> 6
TEST='parallel_port_test'
SUBTEST='dma_read'
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===> 
```

4.7.2.8 Serial Port A Diagnostic

To start the serial port A diagnostic, type 7 at the OBDiag menu prompt. The serial port A diagnostic invokes the `uart_loopback` test. This test transmits and receives 128 characters and checks serial port A transaction validity.

The following code example shows the serial port A output message.

```
CODE EXAMPLE 4-15 Serial Port A Output Message

Enter (0-12 tests, 13 -Quit, 14 -Menu) ===> 7
TEST='uarta_test'
BAUDRATE='1200'
SUBTEST='internal_loopback'
BAUDRATE='1800'
SUBTEST='internal_loopback'
BAUDRATE='2400'
SUBTEST='internal_loopback'
BAUDRATE='4800'
SUBTEST='internal_loopback'
```
Note – The serial port A diagnostic will stall if the TIP line is installed on serial port A. The following code example shows the serial port A output message when the TIP line is installed on serial port A.

**CODE EXAMPLE 4-15  Serial Port A Output Message (Continued)**

```
BAUDRATE='9600'
SUBTEST='internal_loopback'
BAUDRATE='19200'
SUBTEST='internal_loopback'
BAUDRATE='38400'
SUBTEST='internal_loopback'
BAUDRATE='57600'
SUBTEST='internal_loopback'
BAUDRATE='76800'
SUBTEST='internal_loopback'
BAUDRATE='115200'
SUBTEST='internal_loopback'
BAUDRATE='153600'
SUBTEST='internal_loopback'
BAUDRATE='230400'
SUBTEST='internal_loopback'
BAUDRATE='307200'
SUBTEST='internal_loopback'
BAUDRATE='460800'
SUBTEST='internal_loopback'
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===>
```

**CODE EXAMPLE 4-16  Serial Port A Output Message With TIP Line Installed**

```
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===> 7

TEST='uarta_test'
'UART A in use as console - Test not run.'
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===>
```
4.7.2.9 Serial Port B Diagnostic

To start the serial port B diagnostic, type 8 at the OBDiag menu prompt. The serial port B diagnostic is identical to the serial port A diagnostic.

The following code example shows the serial port B output message.

**Note** – The serial port B diagnostic will stall if the TIP line is installed on serial port B.

**CODE EXAMPLE 4-17** Serial Port B Output Message

```plaintext
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===> 8
TEST='uartb_test' BAUDRATE='1200'
SUBTEST='internal_loopback'
BAUDRATE='1800'
SUBTEST='internal_loopback'
BAUDRATE='2400'
SUBTEST='internal_loopback'
BAUDRATE='4800'
SUBTEST='internal_loopback'
BAUDRATE='9600'
SUBTEST='internal_loopback'
BAUDRATE='19200'
SUBTEST='internal_loopback'
BAUDRATE='38400'
SUBTEST='internal_loopback'
BAUDRATE='57600'
SUBTEST='internal_loopback'
BAUDRATE='76800'
SUBTEST='internal_loopback'
BAUDRATE='115200'
SUBTEST='internal_loopback'
BAUDRATE='153600'
SUBTEST='internal_loopback'
BAUDRATE='230400'
SUBTEST='internal_loopback'
BAUDRATE='307200'
SUBTEST='internal_loopback'
BAUDRATE='460800'
SUBTEST='internal_loopback'
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===>
```
4.7.2.10 NVRAM Diagnostic

To start the NVRAM diagnostic, type 9 at the OBDiag menu prompt. The NVRAM diagnostic verifies the NVRAM operation by performing a write and read to the NVRAM.

The following code example shows the NVRAM output message.

**CODE EXAMPLE 4-18  NVRAM Output Message**

```plaintext
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===> 9
TEST='nvram_test'
SUBTEST='write/read_patterns'
SUBTEST='write/read_inverted_patterns'
Enter (0-12 tests, 13 -Quit, 14 -Menu) ===>
```

4.7.2.11 Audio Diagnostic

To start the audio diagnostic, type 10 at the OBDiag menu prompt. The audio diagnostic performs the following:

1. cs4231_test – Verifies the cs4231 internal registers.
2. Line-in to line-out external loopback test.
3. Microphone to headphone external loopback test.

The following code example shows the audio output message.

**CODE EXAMPLE 4-19  Audio Output Message**

```plaintext
Enter (0-13 tests, 14 -Quit, 15 -Menu) ===> 10
TEST='audio_test'
SUBTEST='cs4231_test'
Codec_ID='8a'
Version_ID='a0'
SUBTEST='external_lpbk'

###OBDIAG_MFG_START###
TEST='audio_test'
STATUS='FAILED'
SUBTEST='external_lpbk'
ERRORS='1 '
```
4.7.2.12 EIDE Diagnostic

To start the EIDE diagnostic, type 11 at the OBDiag menu prompt. The EIDE diagnostic validates both the EIDE chip and the IDE bus subsystem.

The following code example shows the EIDE output message.

**CODE EXAMPLE 4-20 EIDE Output Message**

```
TTF='505'
SPEED='299.80 MHz'
PASSES='1'
MESSAGE='Error: External Audio Test not run: Please set the mfg-mode to sys-ext.'
Enter (0-13 tests, 14 -Quit, 15 -Menu) ===>
```

4.7.2.13 Video Diagnostic

To start the video diagnostic, type 12 at the OBDiag menu prompt. The video diagnostic validates the graphics.

The following code example shows the video output message.

**CODE EXAMPLE 4-21 Video Output Message**

```
Enter (0-13 tests, 14 -Quit, 15 -Menu) ===>

TEST='video_test'
SUBTEST='mach64-chip-id-vendor-id-check'
SUBTEST='video-frame-buffer-test'
Enter (0-13 tests, 14 -Quit, 15 -Menu) ===>
```
4.7.2.14 All Above Diagnostic

To start the all above diagnostic, type 13 at the OB DIAG menu prompt. The all above diagnostic validates the entire system.

The following code example shows the all above output message.

Note – The all above diagnostic will stall if the TIP line is installed on serial port A or serial port B.

**CODE EXAMPLE 4-21** Video Output Message (Continued)

```
Enter (0-13 tests, 14 - Quit, 15 - Menu) ===> 12
SUBTEST='mach64-walk-one-test'
SUBTEST='mach64-walk-zero-test'
Enter (0-13 tests, 14 - Quit, 15 - Menu) ===> 12
```

**CODE EXAMPLE 4-22** All Above Output Message

```
Enter (0-13 tests, 14 - Quit, 15 - Menu) ===> 13

TEST='all_pci/cheerio_test'
SUBTEST='vendor_id_test'
SUBTEST='device_id_test'
SUBTEST='mixmode_read'
SUBTEST='e2_class_test'
SUBTEST='status_reg_walk1'
SUBTEST='line_size_walk1'
SUBTEST='latency_walk1'
SUBTEST='line_walk1'
SUBTEST='pin_test'

TEST='all_dma/ebus_test'
SUBTEST='dma_reg_test'
SUBTEST='dma_func_test'

TEST='ethernet_test'
Using Onboard Transceiver - Link Up.
SUBTEST='my_channel_reset'
SUBTEST='hme_reg_test'
SUBTEST='global_reg1_test'
SUBTEST='global_reg2_test'
SUBTEST='bmac_xif_reg_test'
```
### OBDIAG_MFG_START###

<table>
<thead>
<tr>
<th>Test</th>
<th>Subtest</th>
<th>Status</th>
<th>Errors</th>
<th>TTF</th>
<th>Speed</th>
<th>Passes</th>
<th>Message</th>
</tr>
</thead>
<tbody>
<tr>
<td>keyboard</td>
<td>internal_loopback</td>
<td>FAILED</td>
<td>1</td>
<td>1011</td>
<td>299.80 MHz</td>
<td>1</td>
<td>Error: Timeout receiving a character</td>
</tr>
<tr>
<td>mouse</td>
<td>mouse_loopback</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>floppy</td>
<td>floppy_id0_read_test</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>parallel</td>
<td>dma_read</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>uartA</td>
<td>UART_A in use as console</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Test not run</td>
</tr>
<tr>
<td>uartB</td>
<td>internal_loopback</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### CODE EXAMPLE 4-22  All Above Output Message (Continued) ####

```c
SUBTEST='bmac_tx_reg_test'
SUBTEST='mif_reg_test'
SUBTEST='mac_internal_loopback_test'
SUBTEST='10mb_xcvr_loopback_test'
SUBTEST='100mb_phy_loopback_test'
SUBTEST='100mb_twister_loopback_test'

TEST='keyboard_test'
SUBTEST='internal_loopback'

TEST='mouse_test'
SUBTEST='mouse_loopback'

### OBDIAG_MFG_START###

TEST='mouse_test'
STATUS='FAILED'
SUBTEST='mouse_loopback'
ERRORS='1 '
TTF='1011 '
SPEED='299.80 MHz'
PASSES='1 '
MESSAGE='Error: Timeout receiving a character'

TEST='floppy_test'
SUBTEST='floppy_id0_read_test'

TEST='parallel_port_test'
SUBTEST='dma_read'

TEST='uartA_test'
'UART A in use as console - Test not run.'

TEST='uartB_test'
BAUDRATE='1200'
SUBTEST='internal_loopback'
BAUDRATE='1800'
SUBTEST='internal_loopback'
BAUDRATE='2400'
SUBTEST='internal_loopback'
BAUDRATE='4800'
SUBTEST='internal_loopback'
BAUDRATE='9600'
SUBTEST='internal_loopback'
BAUDRATE='19200'
SUBTEST='internal_loopback'
BAUDRATE='38400'
```
CODE EXAMPLE 4-22  All Above Output Message (Continued)

```c
SUBTEST='internal_loopback'
BAUDRATE='57600'
SUBTEST='internal_loopback'
BAUDRATE='76800'
SUBTEST='internal_loopback'
BAUDRATE='115200'
SUBTEST='internal_loopback'
BAUDRATE='153600'
SUBTEST='internal_loopback'
BAUDRATE='230400'
SUBTEST='internal_loopback'
BAUDRATE='307200'
SUBTEST='internal_loopback'
BAUDRATE='460800'
SUBTEST='internal_loopback'

TEST='nvram_test'
SUBTEST='write/read_patterns'
SUBTEST='write/read_inverted_patterns'

TEST='audio_test'
SUBTEST='cs4231_test'
Codec_ID='8a'
Version_ID='a0'
SUBTEST='external_lpbk'

###OBDIAG_MFG_START###
TEST='audio_test'
STATUS='FAILED'
SUBTEST='external_lpbk'
ERRORS='1 '
TTF='1030 '
SPEED='299.80 MHz'
PASSES='1 '
MESSAGE='Error: External Audio Test not run: Please set the mfg-
mode to sys-ext.‘

TEST='ide_test'
SUBTEST='probe-cmd-device'
SUBTEST='hd-and-cd-check'

TEST='video_test'
Please connect the monitor and use ttya/ttyb when running this test
if you are using the screen it may be become unreadable
SUBTEST='mach64-chip-id-vendor-id-check'
SUBTEST='video-frame-buffer-test'
```

Chapter 4  Troubleshooting Procedures  4-29
4.7.3 Exiting the OBDiag Menu

1. At the `ok` prompt, type:

```
ok% setenv mfg-mode off
mfg-mode = off
```

2. At the `ok` prompt, type:

```
ok% setenv diag-switch? false
diag-switch? = false
```

3. At the `ok` prompt, type:

```
ok% setenv auto-boot? true
auto-boot? = true
```

4. At the `ok` prompt, type:

```
ok% reset-all
```
Preparing for Component Replacement

This chapter describes the activities you must do to prepare for removal and replacement of internal system components.

**Note** – It is very important that you review the safety requirements, safety symbols, and safety precautions in this chapter before you begin to remove or replace system components.

This chapter contains the following topics:

- Section 5.8 “Safety Requirements” on page 5-2
- Section 5.9 “Safety Symbols” on page 5-2
- Section 5.10 “Safety Precautions” on page 5-3
- Section 5.11 “Tools Required” on page 5-5
- Section 5.12 “Powering Off the System” on page 5-5
- Section 5.13 “Removing the System Cover” on page 5-8
- Section 5.14 “Attaching the Wrist Strap” on page 5-10
- Section 5.15 “Removing a Filler Panel” on page 5-11
5.8 Safety Requirements

For protection, observe the following safety precautions when setting up the equipment:

- Follow all cautions, warnings, and instructions marked on the equipment.
- Ensure that the voltages and frequency rating of the power receptacle match the electrical rating label on the equipment.
- Never push objects of any kind through openings in the equipment. They may touch dangerous voltage points or short components, resulting in fire or electric shock.
- Refer servicing of equipment to qualified personnel.

5.9 Safety Symbols

The following symbols mean:

<table>
<thead>
<tr>
<th>Caution – Risk of personal injury and equipment damage. Follow the instructions.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Caution – Hazardous voltages are present. To reduce the risk of electric shock and danger to personal health, follow the instructions.</td>
</tr>
<tr>
<td>Caution – Hot surfaces. Avoid contact. Surfaces are hot and may cause personal injury if touched.</td>
</tr>
</tbody>
</table>
5.10 Safety Precautions

Follow all safety precautions.

5.10.1 Modification to Equipment

**Caution** – Do not make mechanical or electrical modifications to the equipment. Sun Microsystems is not responsible for regulatory compliance of a modified Sun product.

5.10.2 Placement of a Sun Product

**Caution** – To ensure reliable operation of the Sun product and to protect it from overheating, ensure equipment openings are not blocked or covered. Never place a Sun product near a radiator or hot air register.

5.10.3 Power Cord Connection

**Caution** – Not all power cords have the same current ratings. Household extension cords do not have overload protection. Do not use household extension cords with a Sun product.

**Caution** – The power switch on this product functions as a standby type device only. The power cord serves as the primary disconnect device for the system. Be sure to connect the power cord into a grounded electrical receptacle that is nearby the system and is readily accessible. Do not connect the power cord when the power supply has been removed from the system chassis.
**Caution** – The power supply of this product is not an autoranging power supply. You must set the power supply voltage setting to either 115V or 230V on the voltage select switch. Failure to correctly set this switch may result in damage to the equipment.

### 5.10.4 Electrostatic Discharge

**Caution** – The boards and hard drives contain electronic components that are extremely sensitive to static electricity. Ordinary amounts of static electricity from clothing or the work environment can destroy components. Do not touch the components themselves or any metal parts. Wear an antistatic wrist strap when handling the drive assemblies, boards, or cards.

**Caution** – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system components, attach an ESD strap to your wrist, then to a metal area on the chassis. Then disconnect the power cord from the system and the wall receptacle. Following this caution equalizes all electrical potentials with the system.

### 5.10.5 Lithium Battery

**Caution** – On Sun motherboards, a lithium battery is molded into the real-time clock, SDS No. M48T59Y, MK48TXXB-XX, M48T18-XXXPCZ, or M48T59W-XXPCZ. Batteries are *not* customer-replaceable parts. They may explode if mistreated. Do not dispose of a battery in fire. Do not disassemble a battery or attempt to recharge it.
5.11 **Tools Required**

The following tools are required to service the Ultra 10 system.

- No. 2 Phillips screwdriver (magnetized tip suggested)
- Needle-nose pliers
- Grounding wrist strap
- Digital voltage meter (DVM)
- Antistatic mat

Place ESD-sensitive components such as the motherboard, circuit cards, hard drives, and NVRAM/TOD on an antistatic mat. The following items can be used as an antistatic mat:

- Bag used to wrap a Sun replacement part
- Shipping container used to package a Sun replacement part
- Inner side (metal part) of the system cover
- Sun ESD mat, part number 250-1088 (available through your Sun sales representative)
- Disposable ESD mat; shipped with replacement parts or optional system features

5.12 **Powering Off the System**

To power off the system:

1. **Back up system files as necessary.**
   
   See *Solaris Handbook for SMCC Peripherals*, part number 802-7675.

   **Caution** – Exit from the operating system before turning off system power. Failure to do so may result in data loss.

2. **Press the system standby switch** ([FIGURE 5-2](#)) or press the Sun Type-5 keyboard Standby key ([FIGURE 5-3](#)) or the Sun I/O Type-6 keyboard Power key ([FIGURE 5-4](#)).

   **Note** – For the system to gracefully shut down by the standby switch or the Sun Type-5/6 keyboard Standby/Power key, UNIX must be operating. If the system is in POST, the standby switch and the Standby key are inoperative.
Caution – Pressing the standby switch or pressing the Sun Type-5/6 keyboard Standby/Power key does not remove all power from the system; a trickle voltage remains in the power supply. To remove all power from the system, set the power switch to the off position.

FIGURE 5-2  System Standby Switch

FIGURE 5-3  Sun Type-5 Keyboard
3. Set the system power switch to the off position (FIGURE 5-5).

Note – For a typical system shutdown or restart, it is not necessary to set the power switch to the off position.
4. Verify the following:
   a. The front panel power indicator LED is off.
   b. The system fans are not spinning.

Caution – Disconnect the AC power cord prior to servicing system components.

5. Turn off the power to the monitor and any peripheral equipment.

6. Disconnect cables to any peripheral equipment.

5.13 Removing the System Cover

Remove the system cover as follows (FIGURE 5-6):

1. Position the system upside-down on its top.

2. Using a No. 2 Phillips screwdriver, remove the four screws securing the system cover to the chassis.

3. Disengage the system cover from the cover tabs.

4. Lift the system cover straight up. Set it aside in a safe place.
FIGURE 5-6  Removing and Replacing the System Cover
5.14 Attaching the Wrist Strap

**Caution** – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system components, attach an ESD strap to your wrist, then to a metal area on the chassis. Then disconnect the power cord from the system and the wall receptacle. Following this caution equalizes all electrical potentials with the system.

1. Unwrap the first two folds of the wrist strap; wrap the adhesive side firmly against your wrist.

2. Peel the liner from the copper foil at the opposite end of the wrist strap.

3. Attach the copper end of the wrist strap to the chassis (FIGURE 5-7).

4. Disconnect the AC power cord from the system.

**FIGURE 5-7** Attaching the Wrist Strap to the Chassis
5.15 Removing a Filler Panel

1. Remove the system cover.
   See Section 5.13 “Removing the System Cover” on page 5-8.

2. Remove the CD-ROM drive.
   See Section 7.3.1 “Removing a CD-ROM Drive” on page 7-13.

3. Remove a filler panel as follows (FIGURE 5-8 and FIGURE 5-9):
   a. Using a No. 2 Phillips screwdriver, remove the two screws (located at the system base) securing the lower bezel to the chassis.
   b. Remove the lower bezel from the system.
   c. Locate the two tabs securing the upper bezel to the chassis. Remove the upper bezel from the chassis by pressing the tabs outward while lifting the bottom of the bezel upward and out.
   d. Remove the plastic filler panel from the upper bezel.
   e. Using a screwdriver, break the metal filler panel from the chassis.
FIGURE 5-8  Removing a Plastic Filler Panel
4. Replace the CD-ROM drive.
   See Section 7.3.2 “Replacing a CD-ROM Drive” on page 7-14.

5. Replace the system cover.
   See Section 10.1 “Replacing the System Cover” on page 10-1.
6.1 Power Supply

To remove and replace the power supply, proceed as follows.

6.1.1 Removing the Power Supply

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.
2. Remove the power supply as follows (FIGURE 6-1):

   a. Disconnect the power cable connectors from the following (not illustrated):
      ■ CD-ROM drive
      ■ Diskette drive
      ■ Hard drive(s)
      ■ Motherboard (J12 and J13)

   b. Set the system on its side.

   c. Using a No. 2 Phillips screwdriver, remove the four screws securing the power supply to the chassis.

   d. Push the power supply forward to disengage the mounting hooks and lift it from the chassis.

FIGURE 6-1  Removing and Replacing the Power Supply
6.1.2 Replacing the Power Supply

1. Replace the power supply as follows (FIGURE 6-1):

   ![Caution icon]
   **Caution** – Verify the voltage selector switch is set to the correct setting: 115V or 230V. Plugging a 115V power cord into a 230V connector will severely damage the system.

   a. Position the power supply into the chassis.
   b. Push the power supply toward the chassis rear, ensuring that the power supply mounting hooks engage into the chassis mounting slots.
   c. Using a No. 2 Phillips screwdriver, replace the four screws securing the power supply to the chassis.
   d. Connect the power cable connectors to the following (not illustrated):
      - CD-ROM drive
      - Diskette drive
      - Hard drive(s)
      - Motherboard (J12 and J13)

   ![Note icon]
   **Note** – Verify that the cable connectors are oriented properly by aligning the connector keys.

2. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
6.2 Cable Assemblies

To remove and replace the diskette drive cable assembly, the hard drive cable assembly, the serial/parallel cable assembly, and the audio cable assembly, proceed as follows.

**Note** – The Ultra 10 diskette drive cable assembly, hard drive cable assembly, serial/parallel cable assembly, and CD-ROM drive cable assembly are part of service kit 370-3266 and cannot be ordered separately.

6.2.1 Removing the Diskette Drive Cable Assembly

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

**Caution** – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the diskette drive cable assembly connectors from the following (FIGURE 6-2):
   - Diskette drive
   - Motherboard (J16) (not illustrated)

3. Remove the diskette drive cable assembly from the chassis.
FIGURE 6-2  Removing and Replacing the Diskette Drive Cable Assembly
6.2.2 Replacing the Diskette Drive Cable Assembly

Caution – The diskette drive cable assembly connector labeled “A” connects to the diskette drive only.

1. Replace the diskette drive cable assembly as follows (Figure 6-2):
   a. Position the diskette drive cable assembly into the chassis.
   b. Connect the diskette drive cable assembly connectors to the following:
      ■ Motherboard (J16)
      ■ Diskette drive

   Note – Verify that the cable connectors are oriented properly by aligning the connector keys.

2. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.

6.2.3 Removing the Hard Drive Cable Assembly

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

   Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Disconnect the hard drive cable assembly connectors from the following (Figure 6-3):
   ■ Hard drive(s)
   ■ Motherboard (J15, not illustrated)

3. Remove the hard drive cable assembly from the chassis.
6.2.4 Replacing the Hard Drive Cable Assembly

1. Replace the hard drive cable assembly as follows (FIGURE 6-3):
   a. Position the hard drive cable assembly into the chassis.
   b. Connect the hard drive cable assembly connectors to the following:
      - Hard drive(s)
      - Motherboard (J15)

   **Note** – Verify that the cable connectors are oriented properly by aligning the connector keys.

2. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
6.2.5 Removing the Serial/Parallel Cable Assembly

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the serial/parallel cable assembly as follows (FIGURE 6-4):
   a. Disconnect the serial/parallel cable assembly connector from the motherboard (J7/J8).
   b. Using a No. 2 Phillips screwdriver, remove the screw securing the serial/parallel cable connector-assembly to the chassis. Remove the connector assembly from the chassis opening.
   c. Remove the serial/parallel cable assembly from the chassis.

FIGURE 6-4 Removing and Replacing the Serial/Parallel Cable Assembly
6.2.6 Replacing the Serial/Parallel Cable Assembly

1. Replace the serial/parallel cable assembly as follows (FIGURE 6-4):
   a. Position the serial/parallel cable assembly into the chassis.
   b. Position the serial/parallel cable connector-assembly into the chassis opening. Using a No. 2 Phillips screwdriver, replace the screw securing the connector assembly to the chassis.
   c. Connect the serial/parallel cable assembly connector to the motherboard (J7/J8).

   **Note** – Verify that the cable connectors are oriented properly by aligning the connector keys.

2. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.

6.2.7 Removing the Audio Cable Assembly

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

   **Caution** – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the audio cable assembly as follows:
   a. Remove the audio cable assembly connectors from the following (FIGURE 6-5):
      ■ CD-ROM drive
      ■ Motherboard (J5)
   b. Remove the audio cable assembly from the chassis.
6.2.8 Replacing the Audio Cable Assembly

1. Replace the audio cable assembly as follows (FIGURE 6-5):
   a. Position the audio cable assembly into the chassis.
   b. Connect the audio cable assembly connectors to the following:
      - Motherboard (J5)
      - CD-ROM drive

   **Note** — Verify that the cable connectors are oriented properly by aligning the connector keys.

2. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
6.3 Speaker Assembly

To remove and replace the speaker assembly, proceed as follows.

6.3.1 Removing the Speaker Assembly

1. **Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.**

   **Caution** – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. **Remove the speaker assembly as follows (FIGURE 6-6):**
   a. Disconnect the speaker cable from the motherboard (J18).
   b. Grasp the speaker magnet and pull the speaker away from the chassis while moving it downward.
   c. Remove the speaker assembly.
6.3.2 Replacing the Speaker Assembly

1. Replace the speaker assembly as follows (FIGURE 6-6):
   a. Position the speaker assembly.
   b. Grasp the speaker magnet and slide the speaker upwards under the three metal chassis speaker tabs until the lower tab engages the outer rim of the speaker.
   c. Connect the speaker cable to the motherboard (J18).

2. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
6.4 CPU Fan Assembly

To remove and replace the CPU fan assembly, proceed as follows.

6.4.1 Removing the CPU Fan Assembly

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the CPU fan assembly as follows (FIGURE 6-7):
   a. Remove all PCI cards.
      See Section 8.5.1 “Removing a PCI Card” on page 8-12.
   b. Remove the graphics card.
      See Section 8.4.1 “Removing a Graphics Card” on page 8-9.
   c. Disconnect the CPU fan assembly power-cable connector from the motherboard (J19).
   d. Press the fan retaining clip and remove the CPU fan assembly from the chassis.
6.4.2 Replacing the CPU Fan Assembly

1. Replace the CPU fan assembly as follows (FIGURE 6-7):
   a. Position the CPU fan assembly, ensuring that the fan retaining clip is aligned with the chassis retaining-clip hole.
   b. Secure the fan retaining clip to the chassis.
   c. Connect the CPU fan assembly power-cable connector to the motherboard (J19).
   d. Replace the graphics card.
      See Section 8.4.2 “Replacing a Graphics Card” on page 8-10.
   e. Replace all PCI cards.
      See Section 8.5.2 “Replacing a PCI Card” on page 8-13.

2. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
6.5 Front Bezel

To remove and replace the front bezel, proceed as follows.

6.5.1 Removing the Front Bezel

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

   Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the CD-ROM drive.
   See Section 7.3.1 “Removing a CD-ROM Drive” on page 7-13.

3. Remove the front bezel as follows (FIGURE 6-8):
   a. Disconnect the standby switch connector from the motherboard.
   b. Remove the lower front bezel and detach the upper front bezel from the chassis as described in Section 5.15 “Removing a Filler Panel” on page 5-11.
6.5.2 Replacing the Front Bezel

1. Replace the front bezel as follows (FIGURE 6-8):

   a. Position the lower front bezel and upper front bezel to the chassis.

   b. Thread the standby switch connector and wires through the chassis access hole and connect the standby switch connector to the motherboard.

   c. Using a No. 2 Phillips screwdriver, replace the two screws (located at the unit base) securing the lower front bezel to the chassis.

   d. Attach the upper front bezel to the chassis by pressing in the upper bezel tabs while lifting the bottom of the bezel down and in.

2. Replace the CD-ROM drive.

   See Section 7.3.2 “Replacing a CD-ROM Drive” on page 7-14.

3. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
6.6 Rear Hard Drive Bracket

To remove and replace the rear hard drive bracket, proceed as follows.

6.6.1 Removing the Read Hard Drive Bracket

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the rear hard drive.
   See Section 7.2.1 “Removing a Hard Drive” on page 7-4.

3. Using a No. 2 Phillips screwdriver, remove the trapezoidal support bracket.

4. Remove the rear hard drive bracket as follows (FIGURE 6-9):

   a. Using a No. 2 Phillips screwdriver, remove the two screws securing the rear hard drive bracket to the chassis.

   b. While placing your hand under the rear hard drive bracket for support, use a No. 2 Phillips screwdriver to remove the screw securing the rear hard drive bracket to the chassis bracket support.

   c. Remove the rear hard drive bracket.
FIGURE 6-9 Removing and Replacing the Rear Hard Drive Bracket
6.6.2 Replacing the Rear Hard Drive Bracket

**Note** – If you are installing a 9.1-GByte or larger capacity replacement or upgrade hard drive in the rear position, a special bracket is required to ensure cooling. This bracket is already installed in new Ultra 10 systems and can be identified by the manufacturing part number, F370-3721, stamped on the side of the bracket.

1. Replace the rear hard drive bracket as follows (FIGURE 6-9):
   a. Position the rear hard drive bracket.
   b. While placing your hand under the rear hard drive bracket for support, use a No. 2 Phillips screwdriver to replace the screw securing the rear hard drive bracket to the chassis bracket support.
   c. Using a No. 2 Phillips screwdriver, replace the two screws securing the rear hard drive bracket to the chassis.

2. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
Storage Devices

This chapter describes how to remove and replace the Ultra 10 storage devices.

This chapter contains the following topics:

- Section 7.1 “Diskette Drive” on page 7-1
- Section 7.2 “Hard Drives” on page 7-4
- Section 7.3 “CD-ROM Drive” on page 7-13

7.1 Diskette Drive

To remove and replace the diskette drive, proceed as follows.

7.1.1 Removing the Diskette Drive

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the diskette drive as follows (FIGURE 7-1):

   a. Disconnect the following:
      - Diskette drive cable assembly from the diskette drive
      - Power cable from the diskette drive
b. Using a No. 2 Phillips screwdriver, remove the screw securing the diskette drive to the diskette drive bracket.

c. Remove the diskette drive through the chassis rear.

FIGURE 7-1  Removing and Replacing the Diskette Drive

7.1.2  Replacing the Diskette Drive

Note  –  Read the diskette drive product guide for information about jumpers, switch settings, or other installation tasks.

1. Replace the diskette drive as follows (FIGURE 7-1):

   a. Position the diskette drive into the diskette drive bracket.

   b. Using your fingers, push the diskette drive toward the chassis front.
c. Using a No. 2 Phillips screwdriver, replace the screw securing the diskette drive to the diskette drive bracket.

d. Connect the following:
   ■ Diskette drive cable assembly to the diskette drive.
   ■ Power cable to the diskette drive.

   **Note** – Verify that the cable connectors are oriented properly by aligning the connector keys.

2. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
7.2 Hard Drives

To remove and replace a hard drive, proceed as follows.

7.2.1 Removing a Hard Drive

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

   Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the hard drive.
   ■ Chassis rear (primary)—go to Step 3
   ■ Chassis front (secondary)—go to Step 4

3. Remove the primary hard drive from the chassis rear to provide clearance as follows (FIGURE 7-2):
   a. Disconnect the power cable connector and the hard drive cable connector from the hard drive. Move the power and hard drive cables out of the way.
   b. Using a No. 2 Phillips screwdriver, remove the two screws securing the hard drive bracket to the chassis.
   c. Using a No. 2 Phillips screwdriver, remove the four screws securing the hard drive to the hard drive bracket.
   d. Remove the hard drive from the hard drive bracket.
   e. Place the hard drive on an antistatic mat.
4. Remove the secondary hard drive from the chassis front as follows (FIGURE 7-3):
   a. Disconnect the power cable connector and the hard drive cable connector from the hard drive. Move the power and hard drive cables out of the way.
   b. Using a No. 2 Phillips screwdriver, remove the two screws securing the hard drive bracket to the chassis.
   c. Slide the hard drive and the hard drive bracket toward the chassis rear until it clears the chassis.
   d. Remove the hard drive and hard drive bracket.
   e. Using a No. 2 Phillips screwdriver, remove the four screws securing the hard drive to the hard drive bracket.
   f. Remove the hard drive from the hard drive bracket.
   g. Place the hard drive on an antistatic mat.
7.2.2 Replacing a Hard Drive

**Note** – Read the hard drive product guide for information about jumpers, switch settings, or other installation tasks.

**Note** – Prior to replacing a hard drive, verify that the back panel mode-select jumper is set to CS.

1. Replace the hard drive.
   - Chassis rear (primary)—go to Step 2
   - Chassis front (secondary)—go to Step 3
2. Replace the primary hard drive into the chassis rear as follows (FIGURE 7-2):

   Note – If the existing rear hard drive is being replaced with a 9.1-Gbyte or larger capacity hard drive, ensure that the existing rear drive bracket is removed and the replacement drive bracket (part number 370-3721) is installed. See Section 6.6 “Rear Hard Drive Bracket” on page 6-17.

   a. Position the hard drive into the hard drive bracket.

       Note – Ensure the correct hard drive orientation.

   b. Using a No. 2 Phillips screwdriver, replace the four screws securing the hard drive to the hard drive bracket.

   c. Position the power cable and the hard drive cable.

   d. Connect the power cable connector and the hard drive cable connector to the hard drive. Dress cables.

       Note – Verify that the cable connectors are oriented properly by aligning the connector keys.

3. Replace the secondary hard drive into the chassis front as follows (FIGURE 7-3):

   a. Position the hard drive into the hard drive bracket.

   b. Using a No. 2 Phillips screwdriver, replace the four screws securing the hard drive to the hard drive bracket.

   c. Position the hard drive and hard drive bracket into the chassis.

   d. Slide the hard drive and hard drive bracket toward the chassis front.

   e. Using a No. 2 Phillips screwdriver, replace the two screws securing the hard drive bracket to the chassis.

   f. Connect the power and hard drive cable connectors to the hard drive. Dress cables.

       Note – Verify that the cable connectors are oriented properly by aligning the connector keys.

4. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
7.2.3 Hard Drive Mirroring

This section describes the requirements and constraints of a hard drive mirroring solution that utilizes Solstice DiskSuite™ software.

7.2.3.1 Hard Drive Mirroring Configuration

The IDE subsystem of the Ultra 10 system has two independent channels designated “primary” and “secondary”. On the Ultra 10 motherboard there are two separate connectors for each channel, allowing each channel to support two devices. One device may be jumpered as “master” (device 0) and the other as “slave” (device 1).

When mirroring hard drives in an Ultra 10 system, use this hardware configuration:

- Primary channel—One hard drive jumpered as master
- Secondary channel—One hard drive jumpered as master

Two IDE cables are required for this configuration. Each cable is connected to the motherboard at one end and to a hard drive (jumpered as master) at the “MASTER” connector. FIGURE 7-4 shows this hardware configuration (with an optional CD-ROM drive jumpered as a slave device on the secondary channel).

![Diagram of Hard Drive Mirroring Configuration]

FIGURE 7-4 Hard Drive Mirroring Configuration

7.2.3.2 Hardware Considerations

This section describes special considerations and requirements for hardware when mirroring hard drives in an Ultra 10 system.

**Note** — The two hard drives that are mirrored cannot be on the same channel. Both hard drives must be jumpered as the master device on two separate channels.
Note – If a CD-ROM drive is included in an Ultra 10 system with this hard drive mirroring configuration, the CD-ROM drive must be jumpered as a slave device on either the primary or the secondary channel.

Note – If a mirrored Ultra 10 system includes a CD-ROM drive, the alias for the CD-ROM drive must be altered at the OBP level before a user can boot using the boot cdrom command. The procedure for altering the alias immediately follows this note.

Changing a CD-ROM Drive Alias

If a mirrored Ultra 10 system includes a CD-ROM drive, the alias for the CD-ROM drive must be altered at the OBP level before a user can boot using the boot cdrom command. This is because the alias for the CD-ROM drive is hardcoded with the assumption that the CD-ROM drive is connected as the master device on the secondary channel (/pci@1f,0/pci@1,1/ide@3/cdrom@2,0:f). In a mirrored configuration, this is not true because the CD-ROM is jumpered as the slave device on the primary or secondary channel. Therefore, the alias is incorrect and must be altered. Use the nvalias command to alter a CD-ROM drive alias as follows:

■ To change the alias for a CD-ROM drive on the primary channel, type:
  
nvalias cdrom /pci@1f,0/pci@1,1/ide@3/cdrom@1,0:f

■ To change the alias for a CD-ROM drive on the secondary channel, type:
  
nvalias cdrom /pci@1f,0/pci@1,1/ide@3/cdrom@3,0:f

7.2.3.3 Required Software and Patches

The supported software version number is Solstice DiskSuite 4.1.

The IDE drivers have been modified and made more robust for mirroring support on the Ultra 10 system. The appropriate driver patch must be installed on the system before using the mirroring features of Solstice DiskSuite software. These required patch numbers are:

■ For Solaris 7—Patch number 107121
■ For Solaris 2.6—Patch number 106407
■ For Solaris 2.5.1—Patch number 106197

The latest versions of these patches are available for download from SunSolve Online at: http://sunsolve.Corp.Sun.COM
7.2.3.4 Software Constraints

When using Solstice DiskSuite 4.1 software, it is recommended that you have a minimum of three metadevice databases to maintain a “quorum.” It is further recommended that the databases be maintained on different disks, which would require three IDE hard drives in the system. Because the Ultra 10 system can support only two hard drives, only two metadevice databases are possible. This limitation has a known impact.

Solstice DiskSuite software will function with only two disks and two database replicas. However, if one disk fails, there is not a quorum. No problem with the system will be seen until after the system is powered down. After the system is powered down, it will not power on and boot in multiuser mode without system administration intervention.

For example, if the quorum is not seen during boot due to a hard drive failure, the system boots in single-user mode. The problem is reported by the system when the machine is rebooted. The output is similar to the following example:

```
ok boot
Hostname: demo
metainit: demo: stale databases
Use metadb to delete databases which are broken.
Ignore any "Read-only file system" error messages.
Reboot the system when finished to reload the metadevice database. After reboot, repair any broken database replicas which were deleted.
Type Ctrl-d to proceed with normal startup, (or give root password for system maintenance):
```

If you see the message shown above, use the recovery procedure in the next section to replace broken database replicas.
### Recovery Procedure for Broken Database Replicas

The high-level recovery steps are as follows:

- Delete the broken database replica and reboot.
- Repair or replace the problem hard drive.
- Add back the database replica.

Detailed instructions for the broken database recovery are as follows:

1. After you see the error messages described in the previous section, type your root password to enter system maintenance mode at the following prompt:

```
Type Ctrl-d to proceed with normal startup,
(or give root password for system maintenance): <root password>
```

The following message then displays:

Entering System Maintenance Mode

2. Type the `metadb` command as follows to look at the databases to determine which database replica is broken.

```
# /usr/opt/SUNWmd/metadb -i
flags first blk    block count
  a p l 1050 1034 /dev/dsk/c0t3d0s3
 M p unknown unknown /dev/dsk/c1t2d0s3
```

In the example shown above, the system can no longer detect the state database replica on slice `/dev/dsk/c1t2d0s3`, which is part of the failed disk. The `metadb` command flags the replicas on this slice as having a problem with the master blocks.

3. Delete the database replica on the bad disk using the `-d` option of the `metadb` command as follows. Using the example, you would type:

```
# /usr/opt/SUNWmd/metadb -d -f /dev/dsk/c1t2d0s3
metadb: demo:/etc/opt/SUNWmd/mddb.cf.new: Read-only file system
```

At this point, the root (/) file system is read-only. You can ignore any `mddb.cf` error messages that are displayed.
4. Verify that the replica was deleted using the `metadb` command again:

```
# /usr/opt/SUNWmd/metadb -i
flags   first blk  block count
a m p lu 1050     1034     /dev/dsk/c0t3d0s3
```

5. Reboot the system.

6. Halt the system and replace the failed hard drive (refer to Section 7.2 “Hard Drives” on page 7-4).

```
# halt
```

7. After replacing the failed hard drive, power on and reboot the system.

```
ok boot
```

8. Use the `format` or the `fmthard` command to partition the hard drive as it was before the failure. Using the example, you would type:

```
# format /dev/rdsk/c1t2d0s0
```

9. Use the `metadb` command to add back the state database replicas and to determine that the state database replicas are correct. Using the example, you would type:

```
# /usr/opt/SUNWmd/metadb -a /dev/dsk/c1t2d0s3
flags   first blk  block count
a m p luo 16       1034     /dev/dsk/c0t3d0s3
a u       16       1034     /dev/dsk/c1t2d0s3
```
7.3 CD-ROM Drive

To remove and replace a CD-ROM drive, proceed as follows.

7.3.1 Removing a CD-ROM Drive

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the CD-ROM drive as follows (FIGURE 7-5):
   a. Remove the following from the rear of the CD-ROM drive:
      - CD-ROM drive cable connector
      - Power cable connector
      - Audio cable connector
   b. Using a No. 2 Phillips screwdriver, remove the four screws securing the CD-ROM drive to the CD-ROM drive bracket.
   c. Place your fingers on the rear of the CD-ROM drive. Push the CD-ROM drive toward the chassis front and remove.
   d. Place the CD-ROM drive on an antistatic mat.
7.3.2 Replacing a CD-ROM Drive

**Note** – Prior to replacing the CD-ROM drive, verify that the CD-ROM drive back panel mode-select jumper is set to MA.

1. Replace the CD-ROM drive as follows (FIGURE 7-5):
   a. Position the CD-ROM drive into the CD-ROM drive bracket. Push the CD-ROM drive toward the chassis rear.
   b. Using a No. 2 Phillips screwdriver, replace the four screws securing the CD-ROM drive to the bracket.
c. Connect the following to the rear of the CD-ROM drive:

- CD-ROM drive cable connector
- Power cable connector
- Audio cable connector

**Note** – Verify that the cable connectors are oriented properly by aligning the connector keys.

2. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
CHAPTER 8

Motherboard and Component Replacement

This chapter describes how to remove and replace the Ultra 10 motherboard and motherboard components.

This chapter contains the following topics:
- Section 8.1 “CPU Module” on page 8-1
- Section 8.2 “NVRAM/TOD” on page 8-4
- Section 8.3 “DIMM” on page 8-6
- Section 8.4 “Graphics Card” on page 8-9
- Section 8.5 “PCI Card” on page 8-12
- Section 8.6 “PCI Riser Board” on page 8-15
- Section 8.7 “Motherboard” on page 8-17

8.1 CPU Module

To remove and replace the CPU module, proceed as follows.

8.1.1 Removing the CPU Module

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.
Caution – The static random access memory (SRAM) heatsinks are extremely fragile. Do not touch the SRAM heatsinks.

2. If necessary, remove any PCI cards installed to provide clearance.
   See Section 8.5.1 “Removing a PCI Card” on page 8-12.

3. Remove the CPU module as follows (FIGURE 8-1):
   a. Using a No. 2 Phillips screwdriver, remove the screw securing the hold-down brace to the riser. Remove the hold-down brace.
   b. Using a No. 2 Phillips screwdriver, remove the screw securing the CPU module hold-down clip to the motherboard. Remove the CPU module hold-down clip.
   c. Using your fingers, gently and evenly lift the edges of the CPU module to loosen it from the motherboard CPU connectors MJ1 and MJ2.
   d. Lift the CPU module upward from the motherboard CPU connectors until it clears the system chassis.
   e. Place the CPU module on an antistatic mat.
8.1.2 Replacing the CPU Module

1. Replace the CPU module as follows (FIGURE 8-1):
   a. Position the CPU module onto the motherboard CPU connectors MJ1 and MJ2.
   b. Grasping the CPU module, gently and evenly press on the CPU module edges until the CPU module begins to seat.
   c. Using both hands, press the CPU module downward evenly until it is properly seated in the motherboard CPU connectors.
   d. Push the hold-down clip forward over the edge of the CPU module.
e. Replace the hold-down clip. Using a No. 2 Phillips screwdriver, replace the screw securing the CPU module hold-down clip to the motherboard.

f. Replace the hold-down brace. Using a No. 2 Phillips screwdriver, replace the screw securing the hold-down brace to the riser.

2. Replace any PCI card(s) removed.
See Section 8.5.2 “Replacing a PCI Card” on page 8-13.

Note – If you upgrade with a replacement CPU module that is faster than 420 MHz, and the system is using either the Solaris 2.5.1 or 2.6 operating environments, software patches are required for those Solaris releases to run at the faster CPU speed. You can order the software patch CDs using part number 704-6657 (for Solaris 2.5.1) or 704-6658 (for Solaris 2.6). Refer to the instructions included with the CD in the Solaris 2.5.1 and 2.6 for 420+ MHz Systems Installation Guide.

3. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.

8.2 NVRAM/TOD

To remove and replace the NVRAM/TOD, proceed as follows.

8.2.1 Removing the NVRAM/TOD

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the NVRAM/TOD as follows (FIGURE 8-2):

a. Remove any PCI cards installed.
   See Section 8.5.1 “Removing a PCI Card” on page 8-12.

b. Locate the NVRAM/TOD and carrier on the motherboard.

c. Grasp the NVRAM/TOD carrier at each end and pull it straight up, gently wiggling it as necessary.
3. Place the NVRAM/TOD and carrier on an antistatic mat.

8.2.2 Replacing the NVRAM/TOD

1. Replace the NVRAM/TOD as follows (FIGURE 8-2):
   a. Position the NVRAM/TOD carrier on the motherboard.
   b. Carefully insert the NVRAM/TOD carrier into the motherboard socket.
   
   **Note** – The carrier is keyed so the NVRAM/TOD can be installed only one way.
   c. Push the NVRAM/TOD into the carrier until it is properly seated.

2. Replace any PCI card(s) removed.
   See Section 8.5.2 “Replacing a PCI Card” on page 8-13.

3. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
8.3 DIMM

To remove and replace a DIMM, proceed as follows.

**Caution** – DIMMs consist of electronic components that are extremely sensitive to static electricity. Ordinary amounts of static electricity from clothing or work environment can destroy the DIMM.

**Caution** – When removing a DIMM, an identical replacement is required. The replacement DIMM must be inserted into the same socket as the removed DIMM.

**Caution** – Each DIMM bank must contain 2 DIMMs of equal density (for example, two 32-Mbyte DIMMs) to function properly. Do not mix DIMM capacities in any bank. For best system performance, install 4 identical DIMMs in the 2 banks.

The following table identifies DIMM banks and slot pairs.

<table>
<thead>
<tr>
<th>Bank</th>
<th>Slot Pairs</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>DIMM1 and DIMM2</td>
</tr>
<tr>
<td>1</td>
<td>DIMM3 and DIMM4</td>
</tr>
</tbody>
</table>

8.3.1 Removing a DIMM

**Caution** – Handle DIMMs only by the edges. Do not touch the DIMM components or metal parts. Always wear a grounding strap when handling a DIMM.

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.
Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Locate the DIMM to be removed.

3. Push the ejection levers away from the DIMM (FIGURE 8-3).

4. Remove the DIMM from the motherboard connector.

5. Place the DIMM on an antistatic mat.
8.3.2 Replacing a DIMM

**Caution** – Do not remove any DIMM from the antistatic container until you are ready to install it on the motherboard. Handle DIMMs only by their edges. Do not touch DIMM components or metal parts. Always wear a grounding strap when handling DIMMs.

1. **Remove the DIMM from the antistatic container.**

2. **Install the DIMM as follows:** (FIGURE 8-3)

   **Caution** – The system *must* have two identical DIMMs installed in a bank. For best system performance, install four identical DIMMs in the two banks. TABLE 8-1 identifies DIMM banks and slot pairs.

   a. Position the DIMM in the connector, ensuring that the notches on the bottom of the DIMM are aligned with the connector alignment bumps.

   **Note** – Bottom DIMM notches and connector alignment bumps are keyed to ensure proper DIMM orientation.

   **Caution** – If the DIMM is not seated into its slot evenly, it can cause shorts that will damage the system. Ensure that all contacts engage at the same time by pressing evenly on the top corners of the DIMM—do *not* rock the DIMM into place. A clicking sound is heard when the DIMM is properly seated.

   b. Press firmly on the DIMM top until the DIMM is properly seated.

3. **Verify the ejection levers are closed toward the DIMM.**

4. **Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.**
8.4 Graphics Card

To remove and replace a graphics card, and to install graphics card patch software, proceed as follows.

8.4.1 Removing a Graphics Card

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

   **Caution** – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove a graphics card as follows (FIGURE 8-4):

   a. Using a No. 2 Phillips screwdriver, remove the screw securing the graphics card bracket tab to the system chassis.

      **Caution** – To avoid damaging the card’s connectors, apply equal force to both ends of the card.

   b. At the two nearest corners of the graphics card, pull the card straight away from the motherboard connector (UPA1).

3. Place the graphics card on an antistatic mat.
8.4.2 Replacing a Graphics Card

**Note** – If you are using the Solaris 2.5.1 Hardware: 11/97 or the Solaris 2.6 5/98 operating environments, and you are installing an Elite3D UPA graphics card, see Section 8.4.3 “Elite3D m3 and Elite3D m6 UPA Graphics Card Patch Information” on page 8-11.

1. Replace the graphics card as follows (FIGURE 8-4):
   a. Position the graphics card into the chassis.
   b. Guide the graphics card bracket tab into the chassis back panel opening.
c. Position the graphics card connector so that it touches its associated graphics card connector on the motherboard.

| Caution – | To avoid damaging the card’s connectors, apply equal force to both ends of the card. |

| Note – | The graphics card connector is a double-row connector that requires two levels of insertion. When installing the graphics card, ensure that the connector is fully seated into the slot. |

d. At the two nearest corners of the card, push the card straight into the connector until the card is fully seated.

e. Using a No. 2 Phillips screwdriver, replace the screw securing the card bracket tab to the system chassis.

2. Connect the video cable to the graphics card video connector.

3. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.

8.4.3 Elite3D m3 and Elite3D m6 UPA Graphics Card Patch Information

If you are installing or using the Solaris 2.5.1 Hardware: 11/97 or the Solaris 2.6 5/98 operating environments, and you are also installing an Elite3D UPA graphics card, you must install the following software patch(es):

- Solaris 2.5.1 Hardware: 11/97 - Patch 105789-01 is automatically installed when the Elite3D UPA graphics card software is installed. It is recommend that software patch 105791-05 (or a more current version of the patch, if available) also be installed.
- Solaris 2.6 5/98 - After installing the Elite 3D UPA graphics card, software patch 105363-06 (or a more current version of the patch, if available) should be installed.

These latest versions of these patches are available through the SunSolve Online website at http://www.sun.com/service/online/index.html, or by contacting Sun Enterprise Services.
8.5 PCI Card

To remove and replace a PCI card, proceed as follows.

8.5.1 Removing a PCI Card

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the PCI card as follows (FIGURE 8-5):

   a. Using a No. 2 Phillips screwdriver, remove the screw securing the PCI card bracket tab to the system chassis.

Caution – To avoid damaging the card’s connector do not apply force to only one end or one side of the card.

   b. Grasp the two corners of the PCI card and pull the card straight out from the PCI riser board connector.

   c. Place the PCI card on an antistatic mat.
8.5.2 Replacing a PCI Card

Note – Read the PCI card product guide for information about jumper or switch settings, slot requirements, and required tools.

1. Replace the PCI card as follows (FIGURE 8-5):
   a. Position the PCI card into the chassis.
   b. Insert the PCI card connector so that it touches the associated PCI riser board connector.
Caution – Support the PCI riser board with the fingers of one hand to insure full insertion of the PCI card into the board.

c. Guide the PCI card bracket tab into the chassis back panel slot.

d. At the two corners of the card, push the card into the PCI riser board connector until the card is fully seated.

e. Using a No. 2 Phillips screwdriver, replace the screw securing the PCI card bracket tab to the system chassis.

2. Connect all external cables to the PCI card.

3. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.
8.6 PCI Riser Board

To remove and replace a PCI riser board, proceed as follows.

8.6.1 Removing the PCI Riser Board

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

   Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the PCI card(s) from the PCI riser board.
   See Section 8.5.1 “Removing a PCI Card” on page 8-12.

3. Remove the PCI riser board as follows (FIGURE 8-6):
   a. Using a No. 2 Phillips screwdriver, remove the two screws securing the PCI riser board to the system chassis.

      Caution – To avoid damaging the board’s connectors, apply equal force to both ends of the board.

   b. At the two upper corners of the PCI riser board, pull the board straight upward from the connector.

   c. Remove the PCI riser board from the chassis.
8.6.2 Replacing the PCI Riser Board

1. Replace the PCI riser board as follows (FIGURE 8-6):
   a. Position the PCI riser board into the chassis.
   b. Position the PCI riser board connector so that it touches its associated connector on the motherboard.
   c. At the two upper corners of the board, push the board straight downward into the connector until the card is fully seated.
d. Using a No. 2 Phillips screwdriver, replace the two screws securing the PCI riser board to the system chassis.

2. Replace the PCI card(s) to the PCI riser board.
   See Section 8.5.2 “Replacing a PCI Card” on page 8-13.

3. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.

---

8.7 Motherboard

To remove and replace a motherboard, proceed as follows.

Note – Use an antistatic mat when working with the motherboard. An antistatic mat contains the cushioning needed to protect the underside components, to prevent motherboard flexing, and to provide antistatic protection.

8.7.1 Removing the Motherboard

1. Power off the system, remove the system cover, and attach an antistatic wrist strap as described in Chapter 5.

   Note – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

2. Remove the motherboard as follows (FIGURE 8-7):

   a. Place the system on its side.

   b. Disconnect the following from the motherboard:

      ■ Speaker cable connector (J18)
      ■ CPU fan cable connector (J19)
      ■ Power-on LED/software power on cable connector (J17)
      ■ Diskette drive cable assembly (J16)
      ■ CD-ROM drive cable connector (J14)
      ■ Hard drive cable connector (J15)
      ■ Audio cable assembly (J9)
      ■ Serial/parallel cable assembly (J7/J8)
c. Remove the following:

i. CPU module
   See Section 8.1.1 “Removing the CPU Module” on page 8-1.

ii. CPU fan assembly
    See Section 6.4.1 “Removing the CPU Fan Assembly” on page 6-13.

iii. PCI card(s)
    See Section 8.5.1 “Removing a PCI Card” on page 8-12.

iv. PCI riser board
    See Section 8.6.1 “Removing the PCI Riser Board” on page 8-15.

v. UPA graphics card(s)
    See Section 8.4.1 “Removing a Graphics Card” on page 8-9.

vi. NVRAM/TOD with carrier
    See Section 8.2.1 “Removing the NVRAM/TOD” on page 8-4.

---

**Note** – The NVRAM/TOD contains the system host identification (ID) and Ethernet address. If the same ID and Ethernet address are to be used on the replacement motherboard, remove the NVRAM/TOD from the motherboard and install it to the new motherboard after motherboard installation.

---

vii. DIMMs
    See Section 8.3.1 “Removing a DIMM” on page 8-6.

d. Remove the motherboard as follows:

i. Disconnect the external cables.

ii. Using a No. 2 Phillips screwdriver, remove the eight screws securing the motherboard to the chassis standoffs.

---

**Caution** – Handle the motherboard by the back panel or by the edges only.

iii. Lift the motherboard from the chassis.

---

**Note** – It may be necessary to slide the motherboard toward the chassis front before lifting from chassis.

---

iv. Place the motherboard on an antistatic mat.
8.7.2 Replacing the Motherboard

**Note** – Jumpers JP3 and JP4 can be set to either RS-423 or RS-232 serial interface. The jumpers are preset for RS-423. RS-232 is required for digital telecommunication within the European Community.
1. Using long-nose pliers, set the motherboard serial port jumpers JP3 and JP4 (refer to the following table).

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Pins 1 + 2 Select</th>
<th>Pins 2 + 3 Select</th>
<th>Default Shunt on Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP3</td>
<td>RS-232</td>
<td>RS-423</td>
<td>2-3</td>
</tr>
<tr>
<td>JP4</td>
<td>RS-232</td>
<td>RS-423</td>
<td>2-3</td>
</tr>
</tbody>
</table>

Note – Motherboard jumpers are identified as JP. Jumper pins are located immediately adjacent to the part number. Ensure that the serial port jumpers are set correctly.

2. Replace the motherboard as follows (FIGURE 8-7):
   a. Replace the motherboard as follows:

   Caution – Handle the motherboard by the back panel or by the edges only.

      i. Position the motherboard into the chassis.

      ii. Using a No. 2 Phillips screwdriver, replace the eight screws securing the motherboard to the chassis.

      iii. Connect the external cables.

   b. Replace the following:
i. DIMMs
   See Section 8.3.2 “Replacing a DIMM” on page 8-8.

ii. NVRAM/TOD with carrier
   See Section 8.2.2 “Replacing the NVRAM/TOD” on page 8-5.

iii. UPA graphics card(s)
   See Section 8.4.2 “Replacing a Graphics Card” on page 8-10.

iv. PCI riser board
   See Section 8.6.2 “Replacing the PCI Riser Board” on page 8-16.

v. PCI card(s)
   See Section 8.5.2 “Replacing a PCI Card” on page 8-13.

vi. CPU fan assembly
   See Section 6.4.2 “Replacing the CPU Fan Assembly” on page 6-14.

vii. CPU module
   See Section 8.1.2 “Replacing the CPU Module” on page 8-3.

c. Connect the following to the motherboard:
   ■ Speaker cable connector (J18)
   ■ CPU fan cable connector (J19)
   ■ Power-on LED/software power on cable connector (J17)
   ■ Diskette drive cable assembly (J16)
   ■ CD-ROM drive cable connector (J14)
   ■ Hard drive cable connector (J15)
   ■ Audio cable assembly (J9)
   ■ Serial/parallel cable assembly (J7/J8)

Note – Verify that the cable connectors are oriented properly by aligning the connector keys.

3. Detach the wrist strap, replace the system cover, and power on the system as described in Chapter 10.

4. Reset the #power-cycles NVRAM variable to zero as follows:
   a. Press the keyboard Stop and A keys after the system banner appears on the monitor.

   b. At the ok prompt, type:

```
ok% setenv #power-cycles 0
```
c. **Verify that the `#power-cycles` NVRAM variable increments each time the system is power cycled.**

---

**Note** – The Solaris operating environment Power Management software uses the `#power-cycles` NVRAM variable to control the frequency of automatic system shutdown (if automatic shutdown is enabled).
Illustrated Parts List

This chapter lists the authorized replaceable parts for the Ultra 10 system. FIGURE 9-1 illustrates an exploded view of the system and TABLE 9-1 lists the replaceable components. Numerical references illustrated in FIGURE 9-1 correlate to the numerical references listed in TABLE 9-1.

Consult your authorized Sun sales representative or service provider to confirm a part number before ordering a replacement part.
### FIGURE 9-1  Ultra 10 System Exploded View

### TABLE 9-1  Ultra 10 System Replaceable Components

<table>
<thead>
<tr>
<th>Numerical Reference</th>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Manual eject floppy</td>
<td>Manual eject diskette drive</td>
</tr>
<tr>
<td>2</td>
<td>Audio cable assembly</td>
<td>Audio subsystem cables</td>
</tr>
<tr>
<td>3</td>
<td>Diskette drive cable assembly</td>
<td>Diskette drive cable. Part of service kit 370-3267</td>
</tr>
<tr>
<td>4</td>
<td>Hard drive cable assembly</td>
<td>Hard drive cable. Part of service kit 370-3267</td>
</tr>
<tr>
<td>5</td>
<td>CD-ROM drive cable assembly</td>
<td>CD-ROM drive cable. Part of service kit 370-3267</td>
</tr>
<tr>
<td>6</td>
<td>Fan assembly</td>
<td>CPU fan, 92-mm</td>
</tr>
<tr>
<td>7</td>
<td>Speaker assembly</td>
<td>System speaker</td>
</tr>
<tr>
<td>8</td>
<td>16-Mbyte DIMM</td>
<td>60-ns, 16-Mbyte DIMM</td>
</tr>
<tr>
<td>8</td>
<td>32-Mbyte DIMM</td>
<td>60-ns, 32-Mbyte DIMM</td>
</tr>
<tr>
<td>8</td>
<td>64-Mbyte DIMM</td>
<td>60-ns, 64-Mbyte DSIMM</td>
</tr>
<tr>
<td>8</td>
<td>128-Mbyte DIMM</td>
<td>60-ns, 128-Mbyte DSIMM</td>
</tr>
<tr>
<td>8</td>
<td>256-Mbyte DIMM</td>
<td>60-ns, 256-Mbyte DSIMM</td>
</tr>
<tr>
<td>8</td>
<td>32-Mbyte DIMM</td>
<td>50-ns, 32-Mbyte DIMM</td>
</tr>
<tr>
<td>8</td>
<td>64-Mbyte DIMM</td>
<td>50-ns, 64-Mbyte DSIMM</td>
</tr>
<tr>
<td>8</td>
<td>128-Mbyte DIMM</td>
<td>50-ns, 128-Mbyte DSIMM</td>
</tr>
<tr>
<td>8</td>
<td>256-Mbyte DIMM</td>
<td>50-ns, 256-Mbyte DSIMM</td>
</tr>
<tr>
<td>9</td>
<td>CPU module</td>
<td>300-MHz, 512-Kbyte external cache</td>
</tr>
<tr>
<td>9</td>
<td>CPU module</td>
<td>333-MHz, 2-Mbyte external cache</td>
</tr>
<tr>
<td>9</td>
<td>CPU module</td>
<td>360-MHz, 2-Mbyte external cache</td>
</tr>
<tr>
<td>9</td>
<td>CPU module</td>
<td>440-MHz, 2-Mbyte external cache</td>
</tr>
<tr>
<td>9</td>
<td>CPU module</td>
<td>480-MHz, 2-Mbyte external cache</td>
</tr>
<tr>
<td>10</td>
<td>Motherboard</td>
<td>System main logic board</td>
</tr>
<tr>
<td>11</td>
<td>NVRAM/TOD</td>
<td>Time of day, 48T59, with carrier</td>
</tr>
<tr>
<td>12</td>
<td>Serial/parallel cable assembly</td>
<td>Serial/parallel cable. Part of service kit 370-3267</td>
</tr>
<tr>
<td>13</td>
<td>PCI card</td>
<td>Generic</td>
</tr>
</tbody>
</table>
TABLE 9-1   Ultra 10 System Replaceable Components (Continued)

<table>
<thead>
<tr>
<th>Numerical Reference</th>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>PCI riser board</td>
<td>Four-slot riser board</td>
</tr>
<tr>
<td>15</td>
<td>Graphics card</td>
<td>Vertical, double buffer plus Z (DBZ) UPA graphics card</td>
</tr>
<tr>
<td>15</td>
<td>Graphics card</td>
<td>Vertical, single buffer UPA graphics card</td>
</tr>
<tr>
<td>15</td>
<td>Graphics card</td>
<td>Elite3D m3 UPA graphics card</td>
</tr>
<tr>
<td>15</td>
<td>Graphics card</td>
<td>Elite3D m6 UPA graphics card</td>
</tr>
<tr>
<td>16</td>
<td>Hard drive</td>
<td>Disk drive, 9.1-Gbyte, 7200 RPM</td>
</tr>
<tr>
<td>17</td>
<td>Power supply</td>
<td>Power supply, 250 watts</td>
</tr>
<tr>
<td>18</td>
<td>CD-ROM drive</td>
<td>CD-ROM drive</td>
</tr>
<tr>
<td>Not shown</td>
<td>Front bezel</td>
<td>System front bezel</td>
</tr>
<tr>
<td>Not shown</td>
<td>Drive bracket</td>
<td>9.1-Gbyte rear drive bracket (rear position only)</td>
</tr>
</tbody>
</table>
Finishing Replacement Procedures

This chapter describes the activities you must do after you finish removing and replacing internal system components. This chapter also explains how to externally control standby operation.

This chapter contains the following topics:

- Section 10.1 “Replacing the System Cover” on page 10-1
- Section 10.2 “Powering On the System” on page 10-3

10.1 Replacing the System Cover

1. Remove the wrist strap from the system chassis and from your wrist.

2. Replace the system cover as follows: (FIGURE 10-1):

   a. Position the system upside-down on its top.

   b. Position the system cover onto the system chassis. Press the system cover onto the chassis until the cover tabs lock.

   c. Using a No. 2 Phillips screwdriver, replace the four screws securing the system cover to the chassis.

   d. Position the system upright.
FIGURE 10-1 Removing and Replacing the System Cover
10.2 Powering On the System

To power on the system:

Caution – Plugging a 115V power cord into a 230V connector will severely damage the system.

1. Verify the voltage selector switch is set to the correct setting: 115V or 230V.
2. Connect the system power cord to the system and to an AC power outlet.
3. Reconnect and turn on power to any peripherals (so that the system can recognize the peripherals when it is powered on).
4. Set the power switch to the on position (FIGURE 10-2).

5. Press the standby switch (FIGURE 10-3), or press the Sun Type-5 keyboard Standby key (FIGURE 10-4) or the Sun I/O Type-6 keyboard Power key (FIGURE 10-5).
FIGURE 10-3 System Standby Switch

FIGURE 10-4 Sun Type-5 Keyboard
6. Verify the following:
   a. The front panel power-indicator LED is on.
   b. The system fans are spinning.
Product Specifications and Reference Information

This appendix provides product specifications for the Ultra 10 system.

- Section A.1 “Physical Specifications” on page A-1
- Section A.2 “Electrical Specifications” on page A-2
- Section A.3 “Modem Setup Specifications” on page A-2
- Section A.4 “Environmental Requirements” on page A-5
- Section A.5 “Reference Information” on page A-6

A.1 Physical Specifications

The following table lists the Ultra 10 physical specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>U.S.A.</th>
<th>Metric</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height</td>
<td>15.75 in.</td>
<td>40.00 cm</td>
</tr>
<tr>
<td>Width</td>
<td>6.93 in.</td>
<td>16.60 cm</td>
</tr>
<tr>
<td>Depth</td>
<td>16.54 in.</td>
<td>42.00 cm</td>
</tr>
<tr>
<td>Weight (approximate)</td>
<td>44.00 lb.</td>
<td>20.00 kg</td>
</tr>
</tbody>
</table>
A.2 Electrical Specifications

The following table lists the electrical specifications for the Ultra 10 system.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC input</td>
<td>47 to 63 Hz, 90 to 132 VAC or 180 to 264 VAC, switch selectable</td>
</tr>
<tr>
<td>DC output</td>
<td>250W (maximum)</td>
</tr>
<tr>
<td>Output 1</td>
<td>+3.3 VDC, 21A</td>
</tr>
<tr>
<td>Output 2</td>
<td>+5.0 VDC, 22A</td>
</tr>
<tr>
<td>Output 3</td>
<td>+12.0 VDC, 5.0A</td>
</tr>
<tr>
<td>Output 4</td>
<td>-12.0 VDC, 0.3A</td>
</tr>
<tr>
<td>Output 5</td>
<td>-12.0 VDC, 0.3A</td>
</tr>
<tr>
<td>Output 6 (Standby)</td>
<td>+5.0 VDC, 0.2A</td>
</tr>
</tbody>
</table>

A.3 Modem Setup Specifications

- Section A.3.1 “Setting Up the Modem” on page A-2
- Section A.3.2 “Serial Port Speed Change” on page A-3
- Section A.3.3 “Modem Recommendations” on page A-4

A.3.1 Setting Up the Modem

Any modem that is compatible with CCITT V.24 can be connected to the system serial port. Modems can be set up to function in one of three ways:

- Dial out only
- Dial in only
- Bidirectional
To set up a modem:

1. **Become superuser** and type `admintool`.

   ```
   % su
   Password: #
   admintool
   ```

2. In the Admintool window, select Serial Port Manager.

3. Select Port a or Port b for your modem connection.

4. Select Edit.
   
The Serial Port Manager: Modify Service window is displayed.

5. Choose the Expert level of detail.

6. From the Use Template menu, choose one of the following:
   - Modem - Dial-out only
   - Modem - Dial-in only
   - Modem - Bidirectional

7. Select Apply.

8. Set your modem auto-answer switch to one of the following:
   - Off – Dial-out only
   - On – dial-in only
   - On – Bidirectional

---

**A.3.2 Serial Port Speed Change**

To change the speed of a serial port, edit the `/etc/remote` file as follows:

1. **Become superuser, and type** `cd /etc`.

   ```
   % su
   Password: #
   cd /etc
   ```

2. **Type** `vi remote`.  

3. **Type** `tip speed device-name`.
   Typical speeds are 9600, 19200 to 38400 bps.
   The device name is the serial port name—for example, `/dev/tty[a,b]` or `/dev/term/[a,b]`.

4. **Press Esc and type** `wq` **to save your file change(s) and to exit from the vi text editor.**

## A.3.3 Modem Recommendations

### A.3.3.1 Cable

For a modem-to-host (system) connection, use an RS-423/RS-232 straight-through cable with DB-25 male connectors at both ends.

### A.3.3.2 Modem Switch Settings (AT Commands)

- Enable transmit flow control (AT&H1) [suggested setting]
  (Required for sending binary/8-bit data.)
- Set link rate to fixed
  (Will not track modem data rate, AT&Bn; n = menu choice in modem manual.)
- Set display result codes (ATQ0)
- Set verbal result codes (ATV1)
- Set result code subset (ATXn; n = option choice)
- Save settings in NVRAM (AT&W)

**Note** — The above settings are meant as helpful guidelines only. These guidelines may change depending on site requirements and the chosen modem.

For additional information about modem switch settings, see the manual that came with the modem.
A.4 Environmental Requirements

The following table lists environmental requirements for the Ultra 10 systems.

<table>
<thead>
<tr>
<th>Environmental</th>
<th>Operating</th>
<th>Non-operating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>40 to 95 degrees F (5 to 35 degrees C)</td>
<td>-4 to 140 degrees F (-20 to 60 degrees C)</td>
</tr>
<tr>
<td>Humidity</td>
<td>80% (max) noncondensing at 95 degrees F (35 degrees C)</td>
<td>95% noncondensing at 140 degrees F (60 degrees C)</td>
</tr>
<tr>
<td>Altitude</td>
<td>10,000 ft (3 km)</td>
<td>40,000 ft (12 km)</td>
</tr>
</tbody>
</table>
A.5 Reference Information

This section contains the following reference information:

- Section A.5.1 “CD-ROM Drive Cabling Configuration” on page A-6
- Section A.5.2 “Ultra 10 Hard Drive Cabling Configuration” on page A-7
- Section A.5.4 “Jumper Settings” on page A-8
- Section A.5.5 “CD Handling and Use” on page A-8

A.5.1 CD-ROM Drive Cabling Configuration

The following block diagram shows the cabling for the CD-ROM drive.

- CD-ROM data cable: connects to motherboard connector J14
- CD-ROM audio cable: connects to motherboard connector J9

![CD-ROM Drive Cabling Configuration Diagram]

FIGURE A-1 CD-ROM Drive Cabling Configuration
A.5.2 Ultra 10 Hard Drive Cabling Configuration

The Ultra 10 hard drive cabling differs, depending on whether there are one or two hard drives configured:

- Hard drive cable: connects to motherboard connector J15
- If two hard drives are installed, the cable assembly connection is as shown in the following block diagram

![Ultra 10 Hard Drive Cabling Configuration](image)

A.5.3 Hard Drive Cabling Configuration (With Two Mirrored Drives)

The following diagram shows the drive cabling configuration when the system contains two mirrored hard drives:

- Primary channel—One hard drive jumpered as master
- Secondary channel—One hard drive jumpered as master

![Hard Drive Mirroring Configuration](image)

**Note** — The two hard drives that are mirrored cannot be on the same channel. Both hard drives must be jumpered as the master device on two separate channels.
A Note – If a CD-ROM drive is included in an Ultra 10 system with this hard drive mirroring configuration, the CD-ROM drive must be jumpered as a slave device on either the primary or the secondary channel.

For more information on hard drive mirroring, see Section 7.2.3 “Hard Drive Mirroring” on page 7-8.

A.5.4 Jumper Settings

Prior to installing a CD-ROM or hard disk drive in an Ultra 10 system, verify that the drive’s back panel mode-select jumper is set as follows:

- Set the CD-ROM drive jumper to MA
- Set a hard drive jumper to CS

A.5.5 CD Handling and Use

The following topics are discussed in this section.

- Inserting a CD into the CD-ROM drive
- Ejecting a CD from the CD-ROM drive
- Cleaning the CD-ROM drive
- Handling and storing CDs

A.5.5.1 Inserting a CD into the CD-ROM Drive

1. After the system is powered on, push the eject button to open the drive tray.
   
   It may be necessary to unmount the CD before manually ejecting it. The CD can also be ejected by using software commands. Refer to the peripherals handbook that corresponds with your operating environment.

2. Place the CD (label side up) into the tray.
   
   Ensure that the CD is properly set into the recessed area of the tray.

3. If the drive is being installed in a vertical position, slide the two bottom tabs on the tray toward each other to hold the CD.
A.5.5.2  Ejecting a CD From the CD-ROM Drive

To eject a CD, press the eject button on the front of the CD-ROM drive.

If the motorized eject mechanism does not operate, insert a thin, stiff wire (such as a paper clip) into the hole next to the eject button to eject the CD.

A.5.5.3  Cleaning the CD-ROM Drive

If the CD-ROM drive cannot read a CD, the cause may be a dirty CD. Follow these guidelines to clean a CD:

![Caution – Do not use solvents such as benzine, paint thinner, antistatic aerosol spray, or abrasive cleaners to clean CDs.]

- Use a soft, clean, lint-free, dry cloth.
- Clean the non-labeled side of the CD.
- Wipe the CD radially from the center to the outside.
- Use professional cleaning kits.

A.5.5.4  Handling and Storing CDs

Follow these guidelines when handling and storing CDs:

- Handle CDs only by their edges; avoid touching CD surfaces.
- Do not write on CDs with permanent marking pens.
- Do not use CDs in high-dust environments.
- Keep CDs out of direct sunlight, extreme sources of heat or cold, and away from dust and moisture.
- Make sure CDs are at room temperature before using them.
- Store CDs in storage boxes so that they remain clean and free of dust.
Signal Descriptions

This appendix describes the Ultra 10 motherboard connector signals and pin assignments.

■ Section B.1 “Power Supply Connectors” on page B-2
■ Section B.2 “Keyboard/Mouse Connector” on page B-4
■ Section B.3 “Twisted-Pair Ethernet Connector” on page B-5
■ Section B.4 “Serial Port A Connector” on page B-7
■ Section B.5 “Serial Port B Connector” on page B-9
■ Section B.6 “Parallel Port Connector” on page B-10
■ Section B.7 “Audio Connectors” on page B-12
■ Section B.8 “Video Connector” on page B-13
B.1 Power Supply Connectors

There are two power supply connectors on the motherboard. The Ultra 10 motherboard uses a standard ATX style connector (J12).

FIGURE B-1 illustrates the J12 connector configuration and TABLE B-1 lists the pin assignments.

![Power Supply Connector J12 Pin Configuration](image)

**TABLE B-1** Power Supply Connector J12 Pin Assignments

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+3.3V</td>
<td>+3.3 VDC</td>
</tr>
<tr>
<td>2</td>
<td>+3.3V</td>
<td>+3.3 VDC</td>
</tr>
<tr>
<td>3</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>4</td>
<td>+5V</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>5</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>6</td>
<td>+5V</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>7</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>8</td>
<td>PWR_OK</td>
<td>Power okay</td>
</tr>
<tr>
<td>9</td>
<td>5VSB</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>+12V</td>
<td>+12 VDC</td>
</tr>
<tr>
<td>11</td>
<td>+3.3V</td>
<td>+3.3 VDC</td>
</tr>
<tr>
<td>12</td>
<td>-12V</td>
<td>-12 VDC</td>
</tr>
<tr>
<td>13</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>14</td>
<td>PS_ON</td>
<td>Power supply on</td>
</tr>
<tr>
<td>15</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
</tbody>
</table>
### TABLE B-1  Power Supply Connector J12 Pin Assignments (Continued)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>17</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>18</td>
<td>-5V</td>
<td>-5 VDC</td>
</tr>
<tr>
<td>19</td>
<td>+5V</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>20</td>
<td>+5V</td>
<td>+5 VDC</td>
</tr>
</tbody>
</table>
B.2 Keyboard/Mouse Connector

The keyboard/mouse connector is a DIN-8 type connector located on the motherboard back panel. The following figure illustrates the keyboard/mouse connector configuration and the following table lists the pin assignments.

![Keyboard/Mouse Connector Pin Configuration](image)

**TABLE B-2**  Keyboard/Mouse Connector Pin Assignments

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>2</td>
<td>Gnd</td>
<td>Chassis ground</td>
</tr>
<tr>
<td>3</td>
<td>+5V</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>4</td>
<td>Mse-rxd</td>
<td>Mouse receive data</td>
</tr>
<tr>
<td>5</td>
<td>Kbd-txd</td>
<td>Keyboard out</td>
</tr>
<tr>
<td>6</td>
<td>Kbd-rxd</td>
<td>Keyboard in</td>
</tr>
<tr>
<td>7</td>
<td>Kbd-pwk</td>
<td>Keyboard power on</td>
</tr>
<tr>
<td>8</td>
<td>+5V</td>
<td>+5 VDC</td>
</tr>
</tbody>
</table>
B.3 Twisted-Pair Ethernet Connector

The twisted-pair Ethernet (TPE) connector is an RJ-45 type connector located on the motherboard back panel. The following figure illustrates the TPE connector configuration and the following table lists the pin assignments.

Caution – Connect only TPE-type cable into the TPE connector.

![TPE Connector Pin Configuration](image)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>tpe0</td>
<td>Transmit data +</td>
</tr>
<tr>
<td>2</td>
<td>tpe1</td>
<td>Transmit data -</td>
</tr>
<tr>
<td>3</td>
<td>tpe2</td>
<td>Receive data +</td>
</tr>
<tr>
<td>4</td>
<td>Common mode termination</td>
<td>Termination</td>
</tr>
<tr>
<td>5</td>
<td>Common mode termination</td>
<td>Termination</td>
</tr>
<tr>
<td>6</td>
<td>tpe3</td>
<td>Receive data -</td>
</tr>
<tr>
<td>7</td>
<td>Common mode termination</td>
<td>Termination</td>
</tr>
<tr>
<td>8</td>
<td>Common mode termination</td>
<td>Termination</td>
</tr>
</tbody>
</table>
B.3.1 TPE Cable-Type Connectivity

The following types of TPE cables can be connected to the TPE connector.

- For 10BASE-T applications, unshielded twisted-pair (UTP) cable:
  - Category 3 (UTP-3, “voice grade”)
  - Category 4 (UTP-4)
  - Category 5 (UTP-5, “data grade”)
- For 100BASE-T applications, UTP cable, UTP-5, “data grade”

B.3.2 External UTP-5 Cable Lengths

The following table lists TPE UTP-5 types, application, and maximum lengths.

<table>
<thead>
<tr>
<th>Cable Type</th>
<th>Application(s)</th>
<th>Maximum Length (Metric)</th>
<th>Maximum Length (US)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UTP-5, “data grade”</td>
<td>10BASE-T or 100BASE-T</td>
<td>100 meters</td>
<td>109 yards</td>
</tr>
</tbody>
</table>
B.4 Serial Port A Connector

The serial port A connector is a DB-25 type connector located on the motherboard back panel. The serial port A connector provides both synchronous and asynchronous serial communications. The following figure illustrates the serial port A connector configuration and the following table lists the pin assignments.

![Serial Port A Connector Pin Configuration](image)

**TABLE B-5** Serial Port A Connector Pin Assignments

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>2</td>
<td>TXD_A</td>
<td>Transmit data A</td>
</tr>
<tr>
<td>3</td>
<td>RXD_A</td>
<td>Receive data A</td>
</tr>
<tr>
<td>4</td>
<td>RTS_A</td>
<td>Read to send A</td>
</tr>
<tr>
<td>5</td>
<td>CTS_A</td>
<td>Clear to send A</td>
</tr>
<tr>
<td>6</td>
<td>DSR_A</td>
<td>Data set ready A</td>
</tr>
<tr>
<td>7</td>
<td>Gnd</td>
<td>Signal ground</td>
</tr>
<tr>
<td>8</td>
<td>DCD_A</td>
<td>Data carrier detect A</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>11</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>12</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>13</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>14</td>
<td>NC</td>
<td>Not connected</td>
</tr>
</tbody>
</table>
TABLE B-5  Serial Port A Connector Pin Assignments (Continued)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>RTXC_A</td>
<td>Transmit clock A</td>
</tr>
<tr>
<td>16</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>17</td>
<td>RXC_A</td>
<td>Receive clock A</td>
</tr>
<tr>
<td>18</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>19</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>20</td>
<td>DTR_A</td>
<td>Data terminal ready A</td>
</tr>
<tr>
<td>21</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>22</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>23</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>24</td>
<td>TXCA</td>
<td>Data terminal ready A</td>
</tr>
<tr>
<td>25</td>
<td>NC</td>
<td>Not connected</td>
</tr>
</tbody>
</table>
B.5  Serial Port B Connector

The serial port B connector is a DB-9 type connector located on the serial/parallel connector back panel. The serial port B connector provides asynchronous serial communications. The following figure illustrates the serial port B connector configuration and the following table lists the pin assignments.

![FIGURE B-5 Serial Port B Connector Pin Configuration](image)

**TABLE B-6**  Serial Port B Connector Pin Assignments

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CD</td>
<td>Carrier detect</td>
</tr>
<tr>
<td>2</td>
<td>RD</td>
<td>Receive data</td>
</tr>
<tr>
<td>3</td>
<td>TD</td>
<td>Transmit data</td>
</tr>
<tr>
<td>4</td>
<td>DTR</td>
<td>Data terminal ready</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>6</td>
<td>DSR</td>
<td>Data set ready</td>
</tr>
<tr>
<td>7</td>
<td>RTS</td>
<td>Request to send</td>
</tr>
<tr>
<td>8</td>
<td>CTS</td>
<td>Clear to send</td>
</tr>
<tr>
<td>9</td>
<td>RI</td>
<td>Ring indicator</td>
</tr>
</tbody>
</table>
B.6 Parallel Port Connector

The parallel port connector is a DB-25 type connector located on the serial/parallel connector back panel. The following figure illustrates the parallel port connector configuration and the following table lists the connector pin assignments.

![Parallel Port Connector Pin Configuration](image)

**TABLE B-7 Parallel Port Connector Pin Assignments**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Data_Strobe_L</td>
<td>Set low during forward channel transfers to latch data into peripheral device. Set high during reverse channel transfers.</td>
</tr>
<tr>
<td>2 to 9</td>
<td>Data[0..7]</td>
<td>The main data bus for the parallel port. Data0 is the least significant bit (LSB). Are not used during reverse channel transfers.</td>
</tr>
<tr>
<td>10</td>
<td>ACK_L</td>
<td>Driven low by the peripheral device to acknowledge data byte transfer from host during forward channel transfer. Qualifies data being transferred to host in reverse channel transfer.</td>
</tr>
<tr>
<td>11</td>
<td>BUSY</td>
<td>Driven high to indicate the peripheral device is not ready to receive data during forward channel transfer. Used to send Data3 and Data7 during reverse channel transfer.</td>
</tr>
<tr>
<td>12</td>
<td>PERROR</td>
<td>Driven high by peripheral device to indicate an error in the paper path during forward channel transfer. Used to send Data2 and Data6 during reverse channel transfer.</td>
</tr>
<tr>
<td>Pin</td>
<td>Signal</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>13</td>
<td>SELECT_L</td>
<td>Indicates the peripheral device is online during forward channel transfer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Used to send Data1 and Data5 during reverse channel transfer.</td>
</tr>
<tr>
<td>14</td>
<td>AFXN_L</td>
<td>Set low by the host to drive the peripheral into auto-line feed mode during</td>
</tr>
<tr>
<td></td>
<td></td>
<td>forward channel transfer. During reverse channel transfer, set low to</td>
</tr>
<tr>
<td></td>
<td></td>
<td>indicate host can receive peripheral device data and then set high to</td>
</tr>
<tr>
<td></td>
<td></td>
<td>acknowledge receipt of peripheral data.</td>
</tr>
<tr>
<td>15</td>
<td>ERROR_L</td>
<td>Set low by the peripheral device to indicate an error during forward</td>
</tr>
<tr>
<td></td>
<td></td>
<td>channel transfer. In reverse channel transfer, set low to indicate peripheral</td>
</tr>
<tr>
<td></td>
<td></td>
<td>device has data ready to send to the host. Used to send Data0 and Data4.</td>
</tr>
<tr>
<td>16</td>
<td>INIT_L</td>
<td>Driven low by the host to reset peripheral.</td>
</tr>
<tr>
<td>17</td>
<td>PAR_IN_L</td>
<td>Set low by the host to select peripheral device for forward channel transfer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Set high to indicate bus direction is from peripheral to host.</td>
</tr>
<tr>
<td>18</td>
<td>Signal ground</td>
<td>Signal ground</td>
</tr>
<tr>
<td>19</td>
<td>Signal ground</td>
<td>Signal ground</td>
</tr>
<tr>
<td>20</td>
<td>Signal ground</td>
<td>Signal ground</td>
</tr>
<tr>
<td>21</td>
<td>Signal ground</td>
<td>Signal ground</td>
</tr>
<tr>
<td>22</td>
<td>Signal ground</td>
<td>Signal ground</td>
</tr>
<tr>
<td>23</td>
<td>Signal ground</td>
<td>Signal ground</td>
</tr>
<tr>
<td>24</td>
<td>Signal ground</td>
<td>Signal ground</td>
</tr>
<tr>
<td>25</td>
<td>Signal ground</td>
<td>Signal ground</td>
</tr>
</tbody>
</table>
B.7 Audio Connectors

The audio connectors are located on the motherboard backpanel. These connectors use EIA standard 0.125-inch (3.5-mm) jacks. The following figure illustrates each audio connector configuration and the following table lists each connector line assignment.

![Audio Connectors Diagram]

**TABLE B-8 Audio Connector Line Assignment**

<table>
<thead>
<tr>
<th>Component</th>
<th>Headphones</th>
<th>Line-Out</th>
<th>Line-In</th>
<th>Microphone</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tip</td>
<td>Left channel</td>
<td>Left channel</td>
<td>Left channel</td>
<td>Left channel</td>
</tr>
<tr>
<td>Ring (center)</td>
<td>Right channel</td>
<td>Right channel</td>
<td>Right channel</td>
<td>Right channel</td>
</tr>
<tr>
<td>Shield</td>
<td>Ground</td>
<td>Ground</td>
<td>Ground</td>
<td>Ground</td>
</tr>
</tbody>
</table>
## B.8 Video Connector

The video connector is a 15-pin mini D-sub connector located on the motherboard backpanel. The following figure illustrates the video connector configuration and the following table lists the video connector pin assignment.

![Video Connector Pin Configuration](image)

### FIGURE B-8 Video Connector Pin Configuration

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Red</td>
<td>Red video signal</td>
</tr>
<tr>
<td>2</td>
<td>Green</td>
<td>Green video signal</td>
</tr>
<tr>
<td>3</td>
<td>Blue</td>
<td>Blue video signal</td>
</tr>
<tr>
<td>4</td>
<td>Gnd</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>6</td>
<td>Gnd</td>
<td>Ground for red video signal</td>
</tr>
<tr>
<td>7</td>
<td>Gnd</td>
<td>Ground for green video signal</td>
</tr>
<tr>
<td>8</td>
<td>Gnd</td>
<td>Ground for green video signal</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>10</td>
<td>Gnd</td>
<td>Ground</td>
</tr>
<tr>
<td>11</td>
<td>Gnd</td>
<td>Ground</td>
</tr>
<tr>
<td>12</td>
<td>SDA</td>
<td>Bidirectional data</td>
</tr>
</tbody>
</table>
### TABLE B-9  Video Connector Pin Assignments (Continued)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>Horizontal sync</td>
<td>Horizontal synchronizing signal</td>
</tr>
<tr>
<td>14</td>
<td>Vertical sync</td>
<td>V. clock</td>
</tr>
<tr>
<td>15</td>
<td>SCL</td>
<td>Data clock</td>
</tr>
</tbody>
</table>
This appendix provides a functional description of the Ultra 10 system.

- Section C.1 “System” on page C-1
- Section C.2 “Clocking” on page C-27
- Section C.3 “Address Mapping” on page C-29
- Section C.4 “Interrupts” on page C-32
- Section C.5 “Power” on page C-36
- Section C.6 “Motherboard” on page C-37
- Section C.7 “Jumper Descriptions” on page C-38
- Section C.8 “Enclosure” on page C-40

C.1 System

The Ultra 10 system is an UltraSPARC port architecture (UPA)-based uniprocessor machine that uses peripheral component interconnect (PCI) as the I/O bus. The CPU module, APB ASIC (advanced PCI bridge), and UPA graphics communicate with each other using the UPA64S and PCI protocols. The graphics card is a UPA slave-only device. The RISC ASIC routes interrupts to the CPU module.

This section discusses the following topics:
- Section C.1.1 “CPU Module” on page C-3
- Section C.1.2 “UPA” on page C-4
- Section C.1.3 “PCI-IDE Interface” on page C-4
- Section C.1.4 “Memory Architecture” on page C-10
- Section C.1.5 “PCI Riser Board” on page C-14
- Section C.1.6 “ASICs” on page C-19
- Section C.1.7 “EBus2 Devices” on page C-21
- Section C.1.8 “Power and Standby Switching” on page C-26

The following figure shows a functional block diagram of the system.
FIGURE C-1 System Functional Block Diagram
C.1.1 CPU Module

The system CPU module is the UltraSPARC-III processor. The CPU module is a high-performance, highly-integrated superscalar processor implementing the SPARC-V9 64-bit RISC architecture. The CPU module is capable of sustaining the execution of up to four instructions per cycle, even in the presence of conditional branches and cache misses. This sustained performance is supported by a decoupled prefetch and dispatch unit with instruction buffer. The CPU module supports both 2D and 3D graphics, as well as image processing, video compression and decompression, and video effects via the sophisticated visual instruction set (VIS). VIS provides high levels of multimedia performance, including real-time video compression/decompression and two streams of MPEG-2 decompression at full broadcast quality with no additional hardware support. The CPU module characteristics and associated features include:

- SPARC-V9 architecture compliant
- Binary compatible with all SPARC application code
- Snooping or directory-based protocol support
- Four-way superscalar design with nine execution units
  - Four integer execution units
  - Three floating-point execution units
  - Two graphics execution units
- Selectable little-endian or big-endian byte ordering
- 64-bit address pointers
- 16-Kbyte non-blocking data cache
- 16-Kbyte instruction cache with single cycle branch following
- Power management
- Software prefetch instruction support
- Multiple outstanding requests

The Ultra 10 system may contain either a 300-MHz, 333-MHz, 360-MHz, 440-MHz, or a 480-MHz CPU module. The following table identifies the cache and SRAM for each module.

<table>
<thead>
<tr>
<th>Module</th>
<th>Second-Level Cache</th>
<th>Data SRAMs</th>
<th>TAG SRAMs</th>
</tr>
</thead>
<tbody>
<tr>
<td>300-Mhz</td>
<td>500-Kbyte</td>
<td>4 - 64K x 18</td>
<td>1 - 64K x 18</td>
</tr>
<tr>
<td>333-Mhz</td>
<td>2-Mbyte</td>
<td>4 - 256K x 18</td>
<td>1 - 64K x 18</td>
</tr>
<tr>
<td>360-Mhz</td>
<td>2-Mbyte</td>
<td>4 - 256K x 18</td>
<td>1 - 64K x 18</td>
</tr>
<tr>
<td>440-Mhz</td>
<td>2-Mbyte</td>
<td>2 - 256K x 36</td>
<td>1 - 256K x 18</td>
</tr>
<tr>
<td>480-Mhz</td>
<td>2-Mbyte</td>
<td>2 - 256K x 36</td>
<td>1 - 256K x 18</td>
</tr>
</tbody>
</table>
C.1.2 UPA

The system unit supports one slave-only UPA slot for a UPA-based graphics device. The UPA 64-bit data bus provides the connection between the CPU module and the UPA graphics. The 64-bit UPA data shares the data bus with memory through six transceiver chips.

The UPA graphics slot receives a differential signal (\text{UPA_CLK +/-}) from the CPU module, which is in synchronization with the CPU module clock. \text{UPA_CLK +/-} clocks at one-third the frequency of the CPU module frequency. All transfers to and from the graphics connector are fully synchronous. The CPU module transfers UPA data to the graphics connector on leading clock edges that correspond to the UPA clock edges. The maximum interface rate is 120 MHz.

The following figure is a functional block diagram of the UPA graphics.

![UPA Graphics Functional Block Diagram](image)

C.1.3 PCI-IDE Interface

The 32-bit, 66-MHz PCI bus is interfaced through a connector to the motherboard. This interface operates at 66 MHz and interfaces to the APB ASIC. There are three PCI buses: primary PCI bus, secondary PCI bus A, and secondary PCI bus B.

- Section C.1.3.1 “Primary PCI Bus” on page C-5
- Section C.1.3.2 “Secondary PCI Buses” on page C-5
- Section C.1.3.3 “APB ASIC” on page C-5
- Section C.1.3.4 “PCIO ASIC” on page C-5
- Section C.1.3.5 “10-/100-Mbit Ethernet” on page C-5
- Section C.1.3.6 “EBus2 Interface” on page C-6
- Section C.1.3.7 “EIDE Interface” on page C-7
- Section C.1.3.8 “PCI-Based Graphics” on page C-9
C.1.3.1 Primary PCI Bus

The CPU module interfaces to the APB ASIC through the primary PCI bus. The primary PCI bus is a 32-bit, 66-MHz bus. The primary PCI bus is 3.3-VDC bus only, and there cannot be a 5-VDC device residing on this bus. In the Ultra 10 systems, the primary PCI bus is a point-to-point bus between the CPU module and the APB ASIC. There are no other devices or slots on the primary PCI bus.

C.1.3.2 Secondary PCI Buses

The secondary PCI buses are designated as PCI bus A and PCI bus B.

Bus A is a 33-MHz, 32-bit bus that interfaces between the APB ASIC and the PCI slots, with no motherboard device communications. PCI bus A is a 5-VDC-only bus and the only supported boards are 5-VDC type.

PCI bus B is also a 33-MHz, 32-bit bus. Unlike PCI bus A, PCI bus B does not interface to any PCI slots; however, it does communicate with motherboard devices. The motherboard devices residing on PCI bus B include:

- APB ASIC
- PCIO ASIC
- PCI-based graphics controller
- PCI-IDE interface

C.1.3.3 APB ASIC

Refer to Section C.1.6.1 “APB” on page C-19.

C.1.3.4 PCIO ASIC

Refer to Section C.1.6.2 “PCIO” on page C-19.

C.1.3.5 10-/100-Mbit Ethernet

The Ethernet channel engine within the PCIO ASIC provides a buffered full-duplex DMA engine and a media access controller (MAC) function. The descriptor-based DMA engine contains independent transmit and receive channels, each with 2 Kbytes of on-chip buffering. The MAC provides a 10-Mbps or a 100-Mbps CSMA/CD protocol based upon a network interface conforming to IEEE 802.3, proposed IEEE 802.30, and Ethernet specifications. The following figure shows a functional block diagram of the 10-/100-Mbit Ethernet.
**C.1.3.6 EBus2 Interface**

The PCIO ASIC provides the EBus2 interface to connect as many as eight 8-bit devices. The following devices reside on the EBus2:

- Audio CODEC
- SuperIO
- Serial communications controller
- NVRAM/TOD
- Flash PROM

Up to eight single- or multi-function Intel-style 8-bit devices can be accommodated. Four internal DMA engines can be attached to any of the 8-bit devices, buffering data streams in 128-byte FIFOs for each channel.

The EBus2 channel engine provides access to several general purpose AUXIO (auxiliary IO) lines, which are used to control miscellaneous system functions.
C.1.3.7 EIDE Interface

The enhanced integrated drive electronics (EIDE) interface is a hard drive interface that is also called an ATA bus interface. With the advent of faster hard drives, the definition of the EIDE interface has been expanded to include new operating PIO and DMA modes. The five PIO modes, numbered zero through four, offer increasingly faster interface speeds, with the higher-numbered mode being the faster. PIO modes 0, 1, and 2 correspond to the EIDE interface as originally defined. PIO mode 3 defines a maximum transfer rate of 11.1 Mbytes per second and PIO mode 4 defines a maximum transfer rate of 16.67 Mbytes per second. Additional DMA modes have also been defined with Multiword DMA wired 0 corresponding to the original DMA interface and DMA modes 1 and 2 being faster transfer rates. Multiword DMA mode 2 is the same speed as the new PIO mode 4.

The following figure shows the EIDE interface functional block diagram.

![EIDE Interface Functional Block Diagram](image)

**FIGURE C-4** EIDE Interface Functional Block Diagram

**Cable Electrical Requirements**

To allow automatic cable selection of a master and a slave hard drive without the need to change drive jumpers, an ATA cable is used to interface the host with the hard drives. Device 0 must be installed on the connector nearest on the cable to the host and device 1 must be installed on the connector farthest from the host.
Cable Labeling
The ATA cable and/or connectors on the cable are clearly marked to indicate which connector should be connected to the slave device, master device, and motherboard (following figure).

Configuration Support
FIGURE C-6 shows the Ultra 10 ATA cable configurations.
C.1.3.8 PCI-Based Graphics

The system has an on-board PCI-based graphics controller. The graphics controller uses either 2-Mbytes SGRAM or 4-Mbytes SGRAM as the graphics memory. The on-board graphics connector is a standard DB15 VGA connector. The PGX graphics controller provides 8-bit graphics with 2-Mbytes SGRAM. The PGX24 graphics controller provides 24-bit graphics with 4-Mbytes SGRAM.

The following two figures show a functional block diagram of the PGX and the PGX24 PCI-based graphics.

**FIGURE C-7** PCI-Based Graphics Functional Block Diagram (PGX)

**FIGURE C-8** PCI-Based Graphics Functional Block Diagram (PGX24)
C.1.4 Memory Architecture

The memory architecture uses the 168-pin JEDEC standard extended data out (EDO) 3.3-VDC buffered DIMMs. The memory controller unit (MCU) is embedded within the CPU module. All memory addressing and control are driven from the CPU module to the motherboard and then buffered before being gated to the DIMM DRAMs (assuming buffered DIMMs). The data path on the DRAM side is 144 bits (2-bit x 72-bit) wide, and data is multiplexed to 72 bits wide on the processor side by using the transceiver switches.

The interface between the CPU module MCU and the system memory subsystem consists of the following:

- A 12-bit multiplexed row-column address
- Two column address select (CAS) lines
- Eight row address select (RAS) lines
- One write enable (WE) line
- Support for 60-ns EDO DRAMs

Up to four DIMMs can be installed. Having only four DIMM connectors requires a stacked and dual-bank DIMM architecture to achieve the 1-Gbyte capacity.

All memory transfers have error checking code (ECC). The MCU performs ECC generation and checking. The following figure is a functional block diagram of the memory interface.
FIGURE C-9  Memory Interface Functional Block Diagram
C.1.4.1 DIMM Memory Configuration

**Caution** – If the system memory is configured with 16-Mbyte DIMMs, and the system memory is being upgraded with anything other than 16-Mbyte DIMMs, you must remove all 16-Mbyte DIMMs and replace them with the memory upgrade.

An additional mode in the MCU supports 11-bit column addressing. Since the total available address bits in the MCU is constant (1-Gbyte maximum addressable), the maximum number of DIMM pairs in this mode is halved in 11-bit column address mode (4 DIMMs). The MCU can only be programmed in 11-bit column address or 10-bit column address mode (16-Mbyte DIMM memory size), therefore the two types of DIMMs cannot be mixed. If 16-Mbyte DIMMS (10-bit column address) are installed and you wish to upgrade with 11-bit column address DIMMs, then the 10-bit DIMMs must be removed and replaced with 11-bit column address DIMMs. The following table lists memory DIMM configurations.

### TABLE C-2 Memory DIMM Configuration

<table>
<thead>
<tr>
<th>Sun Part Number</th>
<th>DIMM Configuration</th>
<th>Number of DRAMs on Module</th>
<th>DIMM Memory Size</th>
<th>Bank Memory Size (2 DIMMs)</th>
<th>Fully Loaded (2 banks, 4 DIMMs)</th>
<th>Column Address Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>370-3211</td>
<td>2-Mbyte x 72</td>
<td>9</td>
<td>16-Mbyte*</td>
<td>32-Mbyte</td>
<td>64-Mbyte</td>
<td>10*</td>
</tr>
<tr>
<td>370-3198</td>
<td>4-Mbyte x 72</td>
<td>18</td>
<td>32-Mbyte</td>
<td>64-Mbyte</td>
<td>128-Mbyte</td>
<td>11</td>
</tr>
<tr>
<td>370-3199</td>
<td>8-Mbyte x 72</td>
<td>9</td>
<td>64-Mbyte</td>
<td>128-Mbyte</td>
<td>256-Mbyte</td>
<td>11</td>
</tr>
<tr>
<td>370-3200</td>
<td>16-Mbyte x 72</td>
<td>18</td>
<td>128-Mbyte</td>
<td>256-Mbyte</td>
<td>512-Mbyte</td>
<td>11</td>
</tr>
<tr>
<td>370-3201</td>
<td>32-Mbyte x 72</td>
<td>36</td>
<td>256-Mbyte</td>
<td>512-Mbyte</td>
<td>1 Gbyte</td>
<td>11</td>
</tr>
</tbody>
</table>

* Do not mix with other DIMM memory size. Do not mix DIMMs that have 10 column address bits with DIMMs that have 11 column address bits.

C.1.4.2 DIMM Characteristics

The DIMMs used in the system have the following characteristics:

- JEDEC standard in 168-pin DIMM
- Support ECC (x72)
- Single 3.3-VDC +/- 0.3-VDC power supply
- LVTTL-compatible input and outputs
- All inputs are buffered with exception of RAS_L
- CAS_L before RAS_L refresh capability
C.1.4.3 Memory Address Assignment

The system memory spans a 1-Gbyte region, starting at physical address 0x000.0000.0000. The system has four DIMM sockets that accept 16-Mbyte to 256-Mbyte DIMMs. DIMMs must be installed in pairs. If the same size pair of DIMMs are not installed, software configures them to the lower size DIMM. Address mapped to memory must be cacheable. Transfers between any port and memory is done in 64-byte cache line size. Non-cacheable accesses to memory are not supported and are treated as an error. Parameters that effect the address assignment of each DIMM module are DIMM size and in which bank (bank 0 or bank 1) the DIMM is installed.

PA[28:27] are used as the DIMM-pair select. PA[29] is used as an upper stack or a lower stack select; 0 is bottom stack and 1 is the upper stack. DIMMs that contain a single bottom stack must have PA[29] set to 0 (lo) to be accessed. The way that PA[29:27] maps into RASx_L is listed in the following table. TABLE C-4 lists the memory address range based on installed DIMMs.

<table>
<thead>
<tr>
<th>TABLE C-3</th>
<th>PA Map Into RASx_L Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA[29:27]</td>
<td>RASx_L Asserted</td>
</tr>
<tr>
<td>000</td>
<td>RASB_L[0]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TABLE C-4</th>
<th>Memory Address Range Based on Installed DIMMs</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIMM Bank Number</td>
<td>DIMM Size</td>
</tr>
<tr>
<td>0</td>
<td>16 Mbyte</td>
</tr>
<tr>
<td>0</td>
<td>32 Mbyte</td>
</tr>
<tr>
<td>0</td>
<td>64 Mbyte</td>
</tr>
<tr>
<td>0</td>
<td>128 Mbyte</td>
</tr>
<tr>
<td>0</td>
<td>256 Mbyte</td>
</tr>
<tr>
<td>1</td>
<td>16 Mbyte</td>
</tr>
<tr>
<td>1</td>
<td>32 Mbyte</td>
</tr>
</tbody>
</table>
C.1.4.4 Transceivers

The system motherboard transceivers are a hub of all data transfers among memory, CPU module, and the UPA graphics. The transceivers are bit-sliced so that six parts are required to implement the memory subsystem.

C.1.5 PCI Riser Board

Because of the space limitations to the system enclosures, a PCI riser board is present in the systems. The PCI riser board supports a maximum of four PCI cards.

**TABLE C-4 Memory Address Range Based on Installed DIMMs (Continued)**

<table>
<thead>
<tr>
<th>DIMM Bank Number</th>
<th>DIMM Size</th>
<th>DIMM Pair Size</th>
<th>Address Range</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>64 Mbyte</td>
<td>128 Mbyte</td>
<td>0x1000.0000 - 0x17FF.FFFF</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>128 Mbyte</td>
<td>256 Mbyte</td>
<td>0x1000.0000 - 0x1FFF.FFFF</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>256 Mbyte</td>
<td>512 Mbyte</td>
<td>0x3000.0000 - 0x3FFF.FFFF</td>
<td>Stacked or Dual banks</td>
</tr>
</tbody>
</table>

**Note** – If the system memory is configured with 16-Mbyte DIMMs, and the system memory is being upgraded with anything other than 16-Mbyte DIMMs, you must remove all 16-Mbyte DIMMs and replace them with the memory upgrade.
C.1.5.1 Connector Definition

The PCI riser board uses the PCI 64-bit standard connector with revised pinout for additional power needed to support four PCI cards. The following table lists the PCI riser board pin summary.

<table>
<thead>
<tr>
<th>Pin Type</th>
<th>Number of Pins</th>
<th>Current Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gnd</td>
<td>38</td>
<td>N/A</td>
</tr>
<tr>
<td>+5V</td>
<td>18 + 4 + 3 = 25</td>
<td>26 amp (max)</td>
</tr>
<tr>
<td>+12V</td>
<td>1 + 2 = 3</td>
<td>2 amp (max)</td>
</tr>
<tr>
<td>-12V</td>
<td>1</td>
<td>1 amp (max)</td>
</tr>
</tbody>
</table>

- Current rating is 1 ampere at 30°C for each pin.
- Pinout follows the 64-bit 5-VDC PCI specification (with modifications for additional power).
- The IDSEL pin for each PCI slot is reserved.

C.1.5.2 PCI Riser Board Pin Assignment

The following table lists the PCI riser board pin assignments.

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Signal</th>
<th>Pin Number</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>TRST_L</td>
<td>A9</td>
<td>Reserved</td>
</tr>
<tr>
<td>A2</td>
<td>+12V</td>
<td>A10</td>
<td>+5V</td>
</tr>
<tr>
<td>A3</td>
<td>TMS</td>
<td>A11</td>
<td>Reserved</td>
</tr>
<tr>
<td>A4</td>
<td>TDI</td>
<td>A12</td>
<td>Gnd</td>
</tr>
<tr>
<td>A5</td>
<td>+5V</td>
<td>A13</td>
<td>Gnd</td>
</tr>
<tr>
<td>A6</td>
<td>INTA1_L</td>
<td>A14</td>
<td>Reserved</td>
</tr>
<tr>
<td>A7</td>
<td>INTC1_L</td>
<td>A15</td>
<td>RST_L</td>
</tr>
<tr>
<td>A8</td>
<td>+5V</td>
<td>A16</td>
<td>+5V</td>
</tr>
<tr>
<td>A17</td>
<td>GNT1_L</td>
<td>A43</td>
<td>PAR</td>
</tr>
</tbody>
</table>
TABLE C-6  PCI Riser Board Pin Assignment (Continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Signal</th>
<th>Pin Number</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A18</td>
<td>Gnd</td>
<td>A44</td>
<td>AD15</td>
</tr>
<tr>
<td>A19</td>
<td>Reserved</td>
<td>A45</td>
<td>Not connected</td>
</tr>
<tr>
<td>A20</td>
<td>AD30</td>
<td>A46</td>
<td>AD13</td>
</tr>
<tr>
<td>A21</td>
<td>Not connected</td>
<td>A47</td>
<td>AD11</td>
</tr>
<tr>
<td>A22</td>
<td>AD28</td>
<td>A48</td>
<td>Gnd</td>
</tr>
<tr>
<td>A23</td>
<td>AD26</td>
<td>A49</td>
<td>AD9</td>
</tr>
<tr>
<td>A24</td>
<td>Gnd</td>
<td>A50</td>
<td>Key</td>
</tr>
<tr>
<td>A25</td>
<td>AD24</td>
<td>A51</td>
<td>Key</td>
</tr>
<tr>
<td>A26</td>
<td>IDSEL1</td>
<td>A52</td>
<td>C/BE0_L</td>
</tr>
<tr>
<td>A27</td>
<td>Not connected</td>
<td>A53</td>
<td>Not connected</td>
</tr>
<tr>
<td>A28</td>
<td>Gnd</td>
<td>A54</td>
<td>AD6</td>
</tr>
<tr>
<td>A29</td>
<td>AD20</td>
<td>A55</td>
<td>AD4</td>
</tr>
<tr>
<td>A30</td>
<td>Gnd</td>
<td>A56</td>
<td>Gnd</td>
</tr>
<tr>
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<td>A34</td>
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<td>A35</td>
<td>Gnd</td>
<td>A61</td>
<td>+5V</td>
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<tr>
<td>A36</td>
<td>TRDY_L</td>
<td>A62</td>
<td>+5V</td>
</tr>
<tr>
<td>A37</td>
<td>Gnd</td>
<td>A63</td>
<td>Gnd</td>
</tr>
<tr>
<td>A38</td>
<td>STOP_L</td>
<td>A64</td>
<td>+5V</td>
</tr>
<tr>
<td>A39</td>
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<td>A40</td>
<td>SDONE</td>
<td>A66</td>
<td>+5V</td>
</tr>
<tr>
<td>A41</td>
<td>SBO_L</td>
<td>A67</td>
<td>+12V</td>
</tr>
<tr>
<td>A42</td>
<td>Gnd</td>
<td>A68</td>
<td>Not connected</td>
</tr>
<tr>
<td>A69</td>
<td>Gnd</td>
<td>B2</td>
<td>TCK</td>
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<td>Pin Number</td>
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<td>Pin Number</td>
<td>Signal</td>
</tr>
<tr>
<td>------------</td>
<td>----------</td>
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</tr>
<tr>
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<td>INTA2_L</td>
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<td>Gnd</td>
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<tr>
<td>A71</td>
<td>REQ2_L</td>
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<td>TDO</td>
</tr>
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<td>A72</td>
<td>Gnd</td>
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<td>+5V</td>
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<tr>
<td>A73</td>
<td>REQ3_L</td>
<td>B6</td>
<td>+5V</td>
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<td>A74</td>
<td>INTA3_L</td>
<td>B7</td>
<td>INTB1_L</td>
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<tr>
<td>A75</td>
<td>+5V</td>
<td>B8</td>
<td>INTD1_L</td>
</tr>
<tr>
<td>A76</td>
<td>INTA4_L</td>
<td>B9</td>
<td>PRSNT1_L</td>
</tr>
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<td>A77</td>
<td>REQ4_L</td>
<td>B10</td>
<td>Reserved</td>
</tr>
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<td>A78</td>
<td>Gnd</td>
<td>B11</td>
<td>PRSNT2_L</td>
</tr>
<tr>
<td>A79</td>
<td>Not connected</td>
<td>B12</td>
<td>Gnd</td>
</tr>
<tr>
<td>A80</td>
<td>INTC2_L</td>
<td>B13</td>
<td>Gnd</td>
</tr>
<tr>
<td>A81</td>
<td>Gnd</td>
<td>B14</td>
<td>Reserved</td>
</tr>
<tr>
<td>A82</td>
<td>INTC3_L</td>
<td>B15</td>
<td>Gnd</td>
</tr>
<tr>
<td>A83</td>
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<td>CLK1</td>
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<td>A84</td>
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<td>B17</td>
<td>Gnd</td>
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<td>A85</td>
<td>GNT3_L</td>
<td>B18</td>
<td>REQ1_L</td>
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<td>A86</td>
<td>INTC4_L</td>
<td>B19</td>
<td>+5V</td>
</tr>
<tr>
<td>A87</td>
<td>Gnd</td>
<td>B20</td>
<td>AD31</td>
</tr>
<tr>
<td>A88</td>
<td>+5V</td>
<td>B21</td>
<td>AD29</td>
</tr>
<tr>
<td>A89</td>
<td>GNT4_L</td>
<td>B22</td>
<td>Gnd</td>
</tr>
<tr>
<td>A90</td>
<td>Gnd</td>
<td>B23</td>
<td>AD27</td>
</tr>
<tr>
<td>A91</td>
<td>+5V</td>
<td>B24</td>
<td>AD25</td>
</tr>
<tr>
<td>A92</td>
<td>Reserved</td>
<td>B25</td>
<td>Not connected</td>
</tr>
<tr>
<td>A93</td>
<td>Gnd</td>
<td>B26</td>
<td>C/BE3_L</td>
</tr>
<tr>
<td>A94</td>
<td>Reserved</td>
<td>B27</td>
<td>AD23</td>
</tr>
<tr>
<td>B1</td>
<td>-12V</td>
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<td>Gnd</td>
</tr>
<tr>
<td>B29</td>
<td>AD21</td>
<td>B52</td>
<td>AD8</td>
</tr>
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</table>
### TABLE C-6  PCI Riser Board Pin Assignment (Continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Signal</th>
<th>Pin Number</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>B30</td>
<td>AD19</td>
<td>B53</td>
<td>AD7</td>
</tr>
<tr>
<td>B31</td>
<td>Not connected</td>
<td>B54</td>
<td>Not connected</td>
</tr>
<tr>
<td>B32</td>
<td>AD17</td>
<td>B55</td>
<td>AD5</td>
</tr>
<tr>
<td>B33</td>
<td>C/BE2_L</td>
<td>B56</td>
<td>AD3</td>
</tr>
<tr>
<td>B34</td>
<td>Gnd</td>
<td>B57</td>
<td>Gnd</td>
</tr>
<tr>
<td>B35</td>
<td>IRDY_L</td>
<td>B58</td>
<td>AD1</td>
</tr>
<tr>
<td>B36</td>
<td>Not connected</td>
<td>B59</td>
<td>+5V</td>
</tr>
<tr>
<td>B37</td>
<td>DEVSEL_L</td>
<td>B60</td>
<td>ACK64_L</td>
</tr>
<tr>
<td>B38</td>
<td>Gnd</td>
<td>B61</td>
<td>+5V</td>
</tr>
<tr>
<td>B39</td>
<td>LOCK_L</td>
<td>B62</td>
<td>+5V</td>
</tr>
<tr>
<td>B40</td>
<td>PERR_L</td>
<td>B63</td>
<td>Reserved</td>
</tr>
<tr>
<td>B41</td>
<td>Not connected</td>
<td>B64</td>
<td>Gnd</td>
</tr>
<tr>
<td>B42</td>
<td>SERR_L</td>
<td>B65</td>
<td>IDSEL4</td>
</tr>
<tr>
<td>B43</td>
<td>Not connected</td>
<td>B66</td>
<td>IDSEL2</td>
</tr>
<tr>
<td>B44</td>
<td>C/BE1_L</td>
<td>B67</td>
<td>Gnd</td>
</tr>
<tr>
<td>B45</td>
<td>AD14</td>
<td>B68</td>
<td>IDSEL3</td>
</tr>
<tr>
<td>B46</td>
<td>Gnd</td>
<td>B69</td>
<td>+5V</td>
</tr>
<tr>
<td>B47</td>
<td>AD12</td>
<td>B70</td>
<td>+5V</td>
</tr>
<tr>
<td>B48</td>
<td>AD10</td>
<td>B71</td>
<td>INTD2_L</td>
</tr>
<tr>
<td>B49</td>
<td>Gnd</td>
<td>B72</td>
<td>Not connected</td>
</tr>
<tr>
<td>B50</td>
<td>Key</td>
<td>B73</td>
<td>INTD3_L</td>
</tr>
<tr>
<td>B51</td>
<td>Key</td>
<td>B74</td>
<td>Gnd</td>
</tr>
<tr>
<td>B75</td>
<td>INTD4_L</td>
<td>B85</td>
<td>Gnd</td>
</tr>
</tbody>
</table>
C.1.6 ASICs

System ASICs include APB, PCIO, and RISC.

C.1.6.1 APB

The advanced PCI bridge (APB) ASIC provides a connection path between the primary PCI bus and the two secondary PCI buses. APB features include:

- 32-bit memory addressing for PIO, 64-bit memory addressing (DACs) for DMA
- 16-bit I/O addressing
- Full concurrences for primary and secondary PCI interfaces
- 72-byte FIFO data buffering on each of the DMA and PIO paths
- Arbitration/prioritization
- PIO reads and writes are in non-cacheable memory space

C.1.6.2 PCIO

The PCI-to-EBus/Ethernet controller (PCIO) ASIC interfaces to the PCI bus and implements three major functions:

- 10-/100-Mbit Ethernet media access controller (MAC)
- Asynchronous 8-bit EBus2 interface

---

**TABLE C-6** PCI Riser Board Pin Assignment (Continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Signal</th>
<th>Pin Number</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>B76</td>
<td>CLK2</td>
<td>B86</td>
<td>Gnd</td>
</tr>
<tr>
<td>B77</td>
<td>INTB2_L</td>
<td>B87</td>
<td>+5V</td>
</tr>
<tr>
<td>B78</td>
<td>Gnd</td>
<td>B88</td>
<td>+5V</td>
</tr>
<tr>
<td>B79</td>
<td>+5V</td>
<td>B89</td>
<td>+5V</td>
</tr>
<tr>
<td>B80</td>
<td>CLK3</td>
<td>B90</td>
<td>+5V</td>
</tr>
<tr>
<td>B81</td>
<td>INTB3_L</td>
<td>B91</td>
<td>Gnd</td>
</tr>
<tr>
<td>B82</td>
<td>Gnd</td>
<td>B92</td>
<td>Reserved</td>
</tr>
<tr>
<td>B83</td>
<td>INTB4_L</td>
<td>B93</td>
<td>Reserved</td>
</tr>
<tr>
<td>B84</td>
<td>CLK4</td>
<td>B94</td>
<td>Gnd</td>
</tr>
</tbody>
</table>
Four dedicated DMA channels:
  ■ Parallel port
  ■ Audio capture/record
  ■ Audio playback
  ■ Diskette

A PCIO ASIC interrupt router directs the channel engine interrupts to the appropriate device. EBus2 interrupts (only those associated with a DMA channel) are assigned to INTA# and Ethernet interrupts are assigned to INTB#. In PC card mode, this is in add-in mode. The PCIO ASIC has separate interrupt lines for each internal device. INTA# becomes ent_irq_1, INTB# is unused, INTC# becomes pport_irq_1, and INTD# becomes fpy_irq_1. Interrupts from the audio capture are routed to audio_cap_irq_1 while interrupts from audio playback are routed to audio_pb_irq_1.

In the motherboard mode, interrupts from external EBus2 devices not associated with DMA channels (for example, keyboard and mouse) are connected directly to the system interrupt controller (RISC) ASIC.

C.1.6.3 RISC

The reset, interrupt, scan, and clock (RISC) ASIC combine the five reset conditions into three signals to the CPU module. Based on these signals, the CPU module sets the proper control register bit to enable the software to identify the source of the reset. The following figure shows the system reset functional block diagram. The five reset conditions include:
  ■ POWER_GOOD from power supply
  ■ Scan control
  ■ Button POR
  ■ Button XIR
  ■ Scan XIR
C.1.7 EBus2 Devices

The devices described in the sections below interface to the EBus2 within PCIO ASIC. The EBus2 is a slave interface that provides slave cycles on the EBus2. The EBus2 slave interface provides eight chip selects. The slave cycle timing(s) on the EBus2 is programmable. Timing control is provided for 7 address ranges that correspond to the EB_CS1 through EB_CS7 address ranges. This section discusses the following topics.

- Section C.1.7.1 “SuperIO” on page C-22
- Section C.1.7.2 “Serial Communications Controller” on page C-23
- Section C.1.7.3 “Flash PROM” on page C-23
- Section C.1.7.4 “NVRAM/TOD” on page C-24
- Section C.1.7.5 “Audio” on page C-24
C.1.7.1 SuperIO

The SuperIO is a chip device that provides the following functions:
- On-chip diskette controller
- Two standard 16550 UARTs used for the serial mouse and keyboard
- Parallel port
- Mixed voltage support
- 100-pin PQFP

Serial Ports/Keyboard and Mouse

The on-chip serial ports are used as the mouse and keyboard devices because the system does not have fast and synchronous serial ports. The following figure is a functional block diagram of the serial port.

Parallel Port

- IEEE 1284-compatible parallel port

All five modes supported:
- Compatible mode
- Nibble mode
- Byte mode
- ECP
- EPP

One legacy DMA channel supported
C.1.7.2 Serial Communications Controller

The Siemens serial communications controller enables a two-channel increased throughput because of 32-byte first-in-first-out (FIFO) architecture. Serial port A (DB25 connector) is fully synchronous/asynchronous, while serial port B (DB9 connector) is asynchronous only. The serial communications controller has 64-byte buffering on both input and output. Therefore, the serial ports take less CPU bandwidth. Interrupts are driven when the buffer is half full. The controller has a dedicated crystal that enables using integer dividers to achieve exact baud rates in most cases. The serial communications controller supports rates up to 921.6 Kbaud. The limitation is the line drivers, which support up to 460.8 Kbaud.

The serial communications controller operates up to 430 Kbaud in asynchronous mode. Synchronous mode operation is up to 460 Kbaud with external clocks.

The line drivers used are compatible with RS232 and RS423 protocols and are set with a jumper on the motherboard. The slew rate of the line drivers is programmable. The system slew rates are set at 10 VDC per microsecond for baud rates greater than 100 Kbaud, and at 5 VDC per microsecond for baud rates less than 100 Kbaud. The following figure is a functional block diagram of the communications controller serial ports.

![Communications Controller Serial Ports Functional Block Diagram](image)

C.1.7.3 Flash PROM

The flash PROM is an 8-Mbit, 5.0 VDC, 1-Mbyte by 8-bit flash memory. The 1 Mbyte of data is divided into 16 sectors of 64 Kbytes of flexible erase capability. This device is designed to be programmed in-system with the standard system 5.0 VDC VCC supply. 12.0 VDC Vpp is not required for program or erase operations. The flash PROM is also programmed in a standard EPROM programmer. The flash PROM has an access time of approximately 120 nanoseconds.
The flash PROM is divided into two halves, the open boot PROM (OBP) half, and the power-on self-test (POST)/open boot diagnostic (OBDiag) half. There are two physical jumpers on the motherboard. One jumper is used to enable either ROMBO or the on-board flash. The second jumper protects the flash prom from accidental writes to the flash PROM.

C.1.7.4 NVRAM/TOD

The non-volatile RAM/time of day (NVRAM/TOD), is an 8K x 8 nonvolatile static RAM and real-time clock. The programmable alarm output is used for turning the system on when Energy Star is enabled and the system has turned itself off. The following figure shows the NVRAM/TOD functional block diagram.

![NVRAM/TOD Functional Block Diagram](image)

C.1.7.5 Audio

The system audio consists of a single-chip CODEC, integrated amplifier, and supporting analog circuitry.

The CODEC is a single-chip stereo, analog-to-digital and digital-to-analog converter based on delta-sigma conversion technique. The microphone input specifications are designed for the SunMicrophone II or equivalent. The following figure shows a functional block diagram of the system audio circuit. TABLE C-7 lists the audio input electrical specifications and TABLE C-8 lists the audio output electrical specifications.
**TABLE C-7**  Audio Input Electrical Specification

<table>
<thead>
<tr>
<th>Parameter (Rec=50, Mon, Play=100)</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage at microphone jack input that results in full scale digital output</td>
<td>66.9</td>
<td>70.4</td>
<td>77.4</td>
<td>mV (p-p)</td>
</tr>
<tr>
<td>Input voltage at line-in jack that results in full scale digital output</td>
<td>6.00</td>
<td>6.54</td>
<td>6.99</td>
<td>V (p-p)</td>
</tr>
<tr>
<td>Microphone input impedance</td>
<td>1.5</td>
<td>2.21</td>
<td>2.5</td>
<td>Kohm</td>
</tr>
<tr>
<td>Microphone input capacitance</td>
<td>200</td>
<td>220</td>
<td>240</td>
<td>pF</td>
</tr>
<tr>
<td>Line-in input impedance</td>
<td>8.7</td>
<td>9.16</td>
<td>9.62</td>
<td>Kohm</td>
</tr>
<tr>
<td>Line-in input capacitance</td>
<td>200</td>
<td>220</td>
<td>240</td>
<td>pF</td>
</tr>
</tbody>
</table>

**TABLE C-8**  Audio Output Electrical Specification

<table>
<thead>
<tr>
<th>Parameter OLB= 1 (Rec=50, Mon, Play=100)</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage at line out that results from a full scale digital signal (ATTN= 0dB)</td>
<td>2.60</td>
<td>2.8</td>
<td>3.20</td>
<td>V (p-p)</td>
</tr>
</tbody>
</table>
C.1.8 Power and Standby Switching

The system has one power switch and two standby switches. These switches include the power switch, the Sun Type-5 keyboard Standby key (or the Sun I/O Type-6 Power key), and the front panel standby switch.

C.1.8.1 Power Switch

The power switch is located on the system back, on the power supply. When set to off, the system is completely off with no power.

C.1.8.2 Keyboard Standby or Power Key

The Sun Type-5 keyboard Standby key (or the Sun I/O Type-6 Power key) turns on the system if the power switch is set to on and the system has been previously placed in the standby mode.

The keyboard Standby/Power key can also be used to suspend the operating system and place the system in the standby mode if the Energy Star power management software (dtpower) has been installed.

C.1.8.3 Front Panel Standby Switch

The front panel standby switch turns on the system if the power switch is set to on and the system has been previously placed in the standby mode.

The front panel standby switch can also be used to halt the operating system and place the system in standby mode.

### TABLE C-8 Audio Output Electrical Specification (Continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>OLB= 1 (Rec=50, Mon, Play=100)</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage at headphone out that results from a full scale digital signal (ATTN= 10.5 dB)</td>
<td>1.55</td>
<td>1.67</td>
<td>1.91</td>
<td>V (p-p)</td>
<td></td>
</tr>
<tr>
<td>Headphone output impedance</td>
<td>15</td>
<td>16</td>
<td>1.0K</td>
<td>ohm</td>
<td></td>
</tr>
<tr>
<td>Line-out output impedance</td>
<td>207</td>
<td>220</td>
<td>233</td>
<td>ohm</td>
<td></td>
</tr>
</tbody>
</table>
C.2 Clocking

There are five system clock domains: CPU, second level cache SRAMs, UPA, PCI, and miscellaneous clocks for the various IO devices.

C.2.1 CPU and UPA Clocking

The CPU and UPA clocks are generated using a frequency synthesizer on the CPU module. The synthesizer output frequency is divided by four, before being driven to the CPU and SRAMs. In addition, one synthesizer output frequency is divided by six and is gated to the CPU module and to the UPA graphics slot as the UPA clock.

C.2.2 PCI Clock Generation

All PCI clocks are generated on the motherboard. Additionally, two 66-MHz PCI clocks are gated to the CPU module through the module connector. TABLE C-9 lists the generated PCI clocks.

The motherboard supports two different PCI clock generators; the ICW48C60-422G clock generator or the CY2254A-2 clock generator. TABLE C-10 and TABLE C-11 list the PCI clock generator frequency select bits for the ICW48C60-422G and the CY2254A-2 PCI clock generators, respectively.

<table>
<thead>
<tr>
<th>TABLE C-9 PCI Clocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component</td>
</tr>
<tr>
<td>CPU module</td>
</tr>
<tr>
<td>APB</td>
</tr>
<tr>
<td>PCI expansion slots</td>
</tr>
<tr>
<td>RISC</td>
</tr>
<tr>
<td>PCIO</td>
</tr>
</tbody>
</table>
### TABLE C-9  PCI Clocks (Continued)

<table>
<thead>
<tr>
<th>Component</th>
<th>66 MHz</th>
<th>33 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDE</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>ATI PCI based VGA</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Total number of PCI clocks</td>
<td>3</td>
<td>7</td>
</tr>
</tbody>
</table>

### TABLE C-10  PCI Clock Generator Frequency Select (ICW48C60-422G)

<table>
<thead>
<tr>
<th>SEL0</th>
<th>SEL1</th>
<th>SEL2</th>
<th>R%EF1:2</th>
<th>CPUx (50/66 MHz)</th>
<th>PCIx (30/33)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>14.318 MHz</td>
<td>50 MHz</td>
<td>25 MHz</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>14.318 MHz</td>
<td>60 MHz</td>
<td>30 MHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>14.318 MHz</td>
<td>66 MHz</td>
<td>33 MHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>14.318 MHz</td>
<td>66 MHz</td>
<td>33 MHz</td>
</tr>
</tbody>
</table>

### TABLE C-11  PCI Clock Generator Frequency Select (CY2254A-2)

<table>
<thead>
<tr>
<th>SEL0</th>
<th>SEL1</th>
<th>OE</th>
<th>R%EF1:2</th>
<th>CPUx (50/66 MHz)</th>
<th>PCIx (30/33)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>14.318 MHz</td>
<td>50 MHz</td>
<td>25 MHz</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>14.318 MHz</td>
<td>60 MHz</td>
<td>30 MHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>14.318 MHz</td>
<td>66 MHz</td>
<td>33 MHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>14.318 MHz</td>
<td>55 MHz</td>
<td>27.5 MHz</td>
</tr>
</tbody>
</table>
C.3 Address Mapping

This section provides the overview of address partitioning and software-visible registers and their respective functionality. The physical address associated with each of these registers is listed, along with a brief description of the register. For further details on the description of the registers and chips functionality refer to the respective chip specification.

- Section C.3.1 “Port Allocations” on page C-29
- Section C.3.2 “UPA Graphics Address Assignments” on page C-30
- Section C.3.3 “PCI Address Assignments” on page C-31

C.3.1 Port Allocations

The following table lists the system port allocations. The CPU module divides the physical address space among:

- Main memory (DRAM)
- UPA graphics
- PCI (which is further subdivided into the primary PCI bus (PCI-A) and the secondary PCI bus (PCI-B bus) when the APB ASIC is used)

<table>
<thead>
<tr>
<th>Address Range in PA&lt;40:0&gt;</th>
<th>Size</th>
<th>Port Access</th>
<th>Access Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000.0000.0000 - 0x000.3FFF.FFFF</td>
<td>1 Gbyte</td>
<td>Main memory</td>
<td>Cacheable</td>
</tr>
<tr>
<td>0x000.4000.0000 - 0x1FF.FFFF.FFFF</td>
<td>Do not use</td>
<td>Undefined</td>
<td>Cacheable</td>
</tr>
<tr>
<td>0x1FC.0000.0000 - 0x1FD.FFFF.FFFF</td>
<td>8 Gbytes</td>
<td>UPA graphics</td>
<td>Non-cacheable</td>
</tr>
<tr>
<td>0x1FE.0000.0000 - 0x1FF.FFFF.FFFF</td>
<td>8 Gbytes</td>
<td>CPU IO</td>
<td>Non-cacheable</td>
</tr>
</tbody>
</table>
C.3.2 UPA Graphics Address Assignments

The following table lists the UPA graphics address assignments. TABLE C-14 lists additional CPU module internal CSR space (non-cacheable).

**TABLE C-13** UPA Address Space

<table>
<thead>
<tr>
<th>UPA Address Space</th>
<th>PA[40:0]</th>
<th>Size</th>
<th>CPU Commands Supported</th>
<th>PCI Commands Generated</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Config. Space</td>
<td>0x1FE.0100.0000 - 0x1FE.01FF.FFFF</td>
<td>16 Mbytes</td>
<td>NC read (max 4 bytes) NC write (max 4 bytes)</td>
<td>Configuration read, configuration write (may also be Special cycle)</td>
</tr>
<tr>
<td>PCI bus IO space</td>
<td>0x1FE.0200.0000 - 0x1FE.02FF.FFFF</td>
<td>16 Mbytes</td>
<td>NC Read (any), NC Write (any)</td>
<td>IO read IO write</td>
</tr>
<tr>
<td>Don’t use</td>
<td>0x1FE.0300.0000 - 0x1FE.FFFF.FFFF</td>
<td></td>
<td>May wrap to configuration or IO Space behavior</td>
<td></td>
</tr>
<tr>
<td>PCI bus memory space</td>
<td>0x1FE.0000.0000 - 0x1FE.FFFF.FFFF</td>
<td>4 Gbytes</td>
<td>NC read (4 byte) NC read (8 byte) NC block read NC write NC block write NC Instruction fetch</td>
<td>Memory read Memory read multiple Memory read line Memory write Memory write memory Read</td>
</tr>
</tbody>
</table>

**TABLE C-14** CPU Module Internal CSR Space

<table>
<thead>
<tr>
<th>PA[40:0]</th>
<th>Owner</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1FE.0000.0000 - 0x1FE.0000.01FF</td>
<td>MCU</td>
</tr>
<tr>
<td>0x1FE.0000.0200 - 0x1FE.0000.03FF</td>
<td>IOM</td>
</tr>
<tr>
<td>0x1FE.0000.0400 - 0x1FE.0000.1FFF</td>
<td>PIE</td>
</tr>
<tr>
<td>0x1FE.0000.2000 - 0x1FE.0000.5FFF</td>
<td>PBM</td>
</tr>
<tr>
<td>0x1FE.0000.6000 - 0x1FE.0000.9FFF</td>
<td>PIE</td>
</tr>
<tr>
<td>0x1FE.0000.A000 - 0x1FE.0000.A7FF</td>
<td>IOM</td>
</tr>
<tr>
<td>0x1FE.0000.A800 - 0x1FE.0000.EFFF</td>
<td>PIE</td>
</tr>
<tr>
<td>0x1FE.0000.F000 - 0x1FE.00FF.FFFF</td>
<td>MCU</td>
</tr>
</tbody>
</table>
C.3.3 PCI Address Assignments

The following table lists the PCI address assignments.

### TABLE C-15 PCI Address Assignments

<table>
<thead>
<tr>
<th>Address Range in PCI Address</th>
<th>Size</th>
<th>PCI Space Addressed</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x8000.0000 - 0xBFFF.FFFF</td>
<td>1 Gbyte</td>
<td>Primary PCI DVMA space</td>
<td>CPU module DVMA register (equals 0x30)</td>
</tr>
<tr>
<td>0x4000.0000 - 0x7FFF.FFFF</td>
<td>1 Gbyte</td>
<td>PCI bus A memory space</td>
<td>PCI slots APB ASIC register (equals 0xc)</td>
</tr>
<tr>
<td>0x40.0000 - 0x7f.ffff</td>
<td>4 Mbytes</td>
<td>PCI bus A I/O space</td>
<td>PCI slots</td>
</tr>
<tr>
<td>0x0000.0000 - 0x3FFF.FFFF</td>
<td>2 Gbytes</td>
<td>PCI bus B memory space</td>
<td>Onboard PCI bus APB ASIC B register (equals 0xc3)</td>
</tr>
<tr>
<td>0xC000.0000 - 0xFFFF.FFFF</td>
<td>8 Mbytes</td>
<td>PCI bus B I/O space</td>
<td></td>
</tr>
</tbody>
</table>

C.3.3.1 PCI Bus A Address Assignments

PCI bus A has all the PCI slots and the address is programmable by the OpenBoot Prom (OBP).

C.3.3.2 PCI Bus B Address Assignments

The PCI bus B address assignments are as follows:

- PCIO ASIC registers
- Boot PROM

**PCIO ASIC Registers**

The PCIO ASIC is a PCI client and the address can be reprogrammed by software during boot only. Therefore, instead of providing absolute addresses for each of the registers, only offset addresses, relative to a base address, are given.

The PCIO ASIC is a multifunction PCI device and its configuration space has three base address pointers:

- Boot PROM
- EBus2 (function 0)
- Ethernet (function 1)
**Boot PROM**

The PCIO ASIC is strapped so that the red mode trap address is:

- UPA: 0xFF.F000.0000
- PCI: 0xF000.0000
- EBus2: 0x00.0000

The following table lists the boot and flash PROM address assignments.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register Description</th>
<th>Type</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00.0000 - 0xFF.FFFF</td>
<td>Flash Prom/EPROM</td>
<td>R</td>
<td>1 or 4 bytes</td>
</tr>
</tbody>
</table>

**C.4 Interrupts**

Interrupts utilize a UPA-provided interrupt vector mechanism. All interrupts are delivered to the CPU module through a packet-write scheme that provides 24 bytes of data to the CPU module. Level sensitive software-acknowledge interrupts, which would typically be communicated through dedicated interrupt lines, are converted into interrupt packets and delivered to the CPU module.

The output of INT_NUM is registered externally and synchronized to the PCI clock before being transferred to the CPU module. The following figure shows the interrupt scheme block diagram and the following table summarizes the interrupt routing.
**TABLE C-17**  Interrupt Routing

<table>
<thead>
<tr>
<th>RISC Pin</th>
<th>Interrupt</th>
<th>Int/Ext</th>
<th>Source</th>
<th>INT_NUM (from RISC)</th>
<th>Type</th>
<th>Offset</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB0_INTREQ7</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x07</td>
<td>Level</td>
<td>0x00</td>
<td>7</td>
</tr>
<tr>
<td>SB0_INTREQ5</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x05</td>
<td>Level</td>
<td>0x01</td>
<td>5</td>
</tr>
<tr>
<td>SB2_INTREQ5</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x05</td>
<td>Level</td>
<td>0x02</td>
<td>5</td>
</tr>
<tr>
<td>SB0_INTREQ2</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x02</td>
<td>Level</td>
<td>0x03</td>
<td>2</td>
</tr>
<tr>
<td>SB1_INTREQ7</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x0F</td>
<td>Level</td>
<td>0x04</td>
<td>7</td>
</tr>
<tr>
<td>SB1_INTREQ5</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x0D</td>
<td>Level</td>
<td>0x05</td>
<td>5</td>
</tr>
<tr>
<td>SB3_INTREQ5</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x1D</td>
<td>Level</td>
<td>0x06</td>
<td>5</td>
</tr>
<tr>
<td>SB1_INTREQ2</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x0A</td>
<td>Level</td>
<td>0x07</td>
<td>2</td>
</tr>
<tr>
<td>SB2_INTREQ7</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x17</td>
<td>Level</td>
<td>0x08</td>
<td>6</td>
</tr>
<tr>
<td>NO RISC PIN</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x38</td>
<td>Level</td>
<td>0x09</td>
<td>5</td>
</tr>
<tr>
<td>NO RISC PIN</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x10</td>
<td>Level</td>
<td>0x0A</td>
<td>2</td>
</tr>
<tr>
<td>SB1_INTREQ2</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x12</td>
<td>Level</td>
<td>0x0B</td>
<td>1</td>
</tr>
<tr>
<td>NO RISC PIN</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x18</td>
<td>Level</td>
<td>0x0C</td>
<td>6</td>
</tr>
<tr>
<td>NO RISC PIN</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x39</td>
<td>Level</td>
<td>0x0D</td>
<td>5</td>
</tr>
</tbody>
</table>

**FIGURE C-15**  Interrupt Scheme Block Diagram
### TABLE C-17 Interrupt Routing (Continued)

<table>
<thead>
<tr>
<th>RISC Pin</th>
<th>Interrupt</th>
<th>Int/Ext</th>
<th>Source</th>
<th>INT_NUM (from RISC)</th>
<th>Type</th>
<th>Offset</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO RISC PIN</td>
<td>Not used</td>
<td>Ext</td>
<td>PCI</td>
<td>0x00</td>
<td>Level</td>
<td>0x0E</td>
<td>2</td>
</tr>
<tr>
<td>SB3_INTREQ2</td>
<td>On Board PCI GFX</td>
<td>Ext</td>
<td>PCI</td>
<td>0x1A</td>
<td>Level</td>
<td>0x0F</td>
<td>1</td>
</tr>
<tr>
<td>SB0_INTREQ6</td>
<td>PCI A slot 0, INTA#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x06</td>
<td>Level</td>
<td>0x10</td>
<td>6</td>
</tr>
<tr>
<td>SB0_INTREQ4</td>
<td>PCI A slot 0, INTB#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x04</td>
<td>Level</td>
<td>0x11</td>
<td>4</td>
</tr>
<tr>
<td>SB0_INTREQ3</td>
<td>PCI A slot 0, INTC#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x03</td>
<td>Level</td>
<td>0x12</td>
<td>3</td>
</tr>
<tr>
<td>SB0_INTREQ1</td>
<td>PCI A slot 0, INTD#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x01</td>
<td>Level</td>
<td>0x13</td>
<td>1</td>
</tr>
<tr>
<td>SB1_INTREQ6</td>
<td>PCI A slot 1, INTA#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x0E</td>
<td>Level</td>
<td>0x14</td>
<td>6</td>
</tr>
<tr>
<td>SB1_INTREQ4</td>
<td>PCI A slot 1, INTB#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x0C</td>
<td>Level</td>
<td>0x15</td>
<td>4</td>
</tr>
<tr>
<td>SB1_INTREQ3</td>
<td>PCI A slot 1, INTC#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x0B</td>
<td>Level</td>
<td>0x16</td>
<td>3</td>
</tr>
<tr>
<td>SB1_INTREQ1</td>
<td>PCI A slot 1, INTD#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x09</td>
<td>Level</td>
<td>0x17</td>
<td>1</td>
</tr>
<tr>
<td>SB2_INTREQ6</td>
<td>PCI A slot 2, INTA#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x16</td>
<td>Level</td>
<td>0x18</td>
<td>6</td>
</tr>
<tr>
<td>SB2_INTREQ4</td>
<td>PCI A slot 2, INTB#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x14</td>
<td>Level</td>
<td>0x19</td>
<td>4</td>
</tr>
<tr>
<td>SB2_INTREQ3</td>
<td>PCI A slot 2, INTC#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x13</td>
<td>Level</td>
<td>0x1A</td>
<td>3</td>
</tr>
<tr>
<td>SB2_INTREQ1</td>
<td>PCI A slot 2, INTD#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x11</td>
<td>Level</td>
<td>0x1B</td>
<td>1</td>
</tr>
<tr>
<td>SB3_INTREQ6</td>
<td>PCI A slot 3, INTA#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x1E</td>
<td>Level</td>
<td>0x1C</td>
<td>6</td>
</tr>
<tr>
<td>SB3_INTREQ4</td>
<td>PCI A slot 3, INTB#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x1C</td>
<td>Level</td>
<td>0x1D</td>
<td>4</td>
</tr>
<tr>
<td>SB3_INTREQ3</td>
<td>PCI A slot 3, INTC#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x1B</td>
<td>Level</td>
<td>0x1E</td>
<td>3</td>
</tr>
<tr>
<td>SB3_INTREQ1</td>
<td>PCI A slot 3, INTD#</td>
<td>Ext</td>
<td>PCI</td>
<td>0x19</td>
<td>Level</td>
<td>0x1F</td>
<td>1</td>
</tr>
<tr>
<td>SCSI_INT</td>
<td>IDE</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x20</td>
<td>Level</td>
<td>0x20</td>
<td>3</td>
</tr>
<tr>
<td>ETHERNET_INT</td>
<td>Ethernet</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x21</td>
<td>Level</td>
<td>0x21</td>
<td>3</td>
</tr>
<tr>
<td>PARALLEL_INT</td>
<td>Parallel Port</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x22</td>
<td>Level</td>
<td>0x22</td>
<td>2</td>
</tr>
<tr>
<td>AUDIO_INT</td>
<td>Audio Capture/Rec</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x24</td>
<td>Level</td>
<td>0x23</td>
<td>8</td>
</tr>
<tr>
<td>SB3_INTREQ7</td>
<td>Audio Playback</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x1F</td>
<td>Level</td>
<td>0x24</td>
<td>7</td>
</tr>
<tr>
<td>RISC Pin</td>
<td>Interrupt</td>
<td>Int/Ext</td>
<td>Source</td>
<td>INT_NUM (from RISC)</td>
<td>Type</td>
<td>Offset</td>
<td>Priority</td>
</tr>
<tr>
<td>------------------</td>
<td>----------------------------</td>
<td>---------</td>
<td>--------</td>
<td>---------------------</td>
<td>------</td>
<td>--------</td>
<td>----------</td>
</tr>
<tr>
<td>Power_FAIL_INT</td>
<td>Power Fail</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x25</td>
<td>Level</td>
<td>0x25</td>
<td>8</td>
</tr>
<tr>
<td>KEYBOARD_INT</td>
<td>IDE Channel 2 (Not used)</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x28</td>
<td>Level</td>
<td>0x26</td>
<td>7</td>
</tr>
<tr>
<td>FLOPPY_INT</td>
<td>Diskette</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x29</td>
<td>Level</td>
<td>0x27</td>
<td>8</td>
</tr>
<tr>
<td>SPARE_INT</td>
<td>Spare hardware</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x2A</td>
<td>Level</td>
<td>0x28</td>
<td>2</td>
</tr>
<tr>
<td>SKEY_INT</td>
<td>Keyboard</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x2B</td>
<td>Level</td>
<td>0x29</td>
<td>4</td>
</tr>
<tr>
<td>SMOU_INT</td>
<td>Mouse</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x2C</td>
<td>Level</td>
<td>0x2A</td>
<td>4</td>
</tr>
<tr>
<td>SSER_INT</td>
<td>Serial Ports</td>
<td>Ext</td>
<td>OBIO</td>
<td>0x2D</td>
<td>Level</td>
<td>0x2B</td>
<td>7</td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>Ext</td>
<td>OBIO</td>
<td>0x2C - 0x2D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Uncorrectable ECC</td>
<td>Int ECC</td>
<td>Int</td>
<td>ECC</td>
<td>0x2E</td>
<td>Level</td>
<td>0x2E</td>
<td>8</td>
</tr>
<tr>
<td>Correctable ECC</td>
<td>Int ECC</td>
<td>Int</td>
<td>ECC</td>
<td>0x2F</td>
<td>Level</td>
<td>0x2F</td>
<td>8</td>
</tr>
<tr>
<td>PCI Bus Error</td>
<td>Int PBM</td>
<td>Int</td>
<td>PBM</td>
<td>0x30</td>
<td>Level</td>
<td>0x30</td>
<td>8</td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>Int</td>
<td></td>
<td>0x31 - 0x32</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Graphics1_INT</td>
<td>Graphics</td>
<td>Ext</td>
<td>UPA64</td>
<td>0x23</td>
<td>Pulse</td>
<td>FROM INR</td>
<td>5</td>
</tr>
<tr>
<td>Graphics1_INT</td>
<td>Graphics (Not used)</td>
<td>Ext</td>
<td>UPA64</td>
<td>0x26</td>
<td>Pulse</td>
<td>FROM INR</td>
<td>5</td>
</tr>
<tr>
<td>No Interrupt</td>
<td>Ext NONE</td>
<td>Ext</td>
<td>NONE</td>
<td>0x3F</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>
C.5  Power

This section discusses the following topics.

- Section C.5.1 “Onboard Voltage Regulator” on page C-36
- Section C.5.2 “Power Supply Memory” on page C-36

C.5.1  Onboard Voltage Regulator

The onboard voltage regulator meets VRM8.1 specifications. The output of the voltage regulator is programmed by the module. The module drives VID[3:0], which asks the regulator to generate the correct core voltage for the CPU module core voltage and SRAM IO.

C.5.2  Power Supply Memory

The system remembers the state that it was in before a power failure or accidental power cord removal. This circuit is implemented on the motherboard. A latching relay circuit on the motherboard performs this function.

C.5.3  Power Management

To meet EPA Energy Star requirements, the system power consumption is lower than 30 watts.

In-system software monitors system activity, and based on the system control settings, system software saves the machine state (including the memory) onto the hard drive and halts the operating system. The system software then turns off the power supply.

Based on the setting of the NVRAM/TOD, which has an alarm clock, the system is turned on automatically if the alarm is set. This is done by having the interrupt out of the NVRAM/TOD directly connected to the power supply. The power supply requires a power_off signal for the system software to be able to write to a bit within a register and have the power supply shut down.
C.6 Motherboard

The following figure illustrates a block diagram of the system motherboard.

FIGURE C-16 Motherboard Block Diagram
C.7 Jumper Descriptions

Jumper configurations can be changed by setting jumper switches on the motherboard. The motherboard’s jumpers are preset at the factory.

A jumper switch is closed (sometimes referred to as shorted) with the plastic cap inserted over two pins of the jumper. A jumper is open with the plastic cap inserted over one or no pin(s) of the jumper. The following figure shows the different jumper settings that are used on the motherboard.

![Figure C-17 Selected Jumper Settings](image)

Jumper descriptions include brief overviews of serial port jumpers, flash PROM jumpers, and additional system board jumper and connector blocks.

Jumpers are identified on the system board by J designations. Jumper pins are located immediately adjacent to the J designator. Ensure that the serial port jumpers are set correctly.

![Figure C-18 Identifying Jumper Pins](image)
C.7.1 Serial Port Jumpers

Serial port jumpers JP3 and JP4 can be set to either RS-423 or RS-232 serial interface. The jumpers are preset for RS-423. RS-232 is required for digital telecommunication within the European Community. The following table identifies serial port jumper settings. If the system is being connected to a public X.25 network, the serial-port-mode jumper setting may need to change from RS-423 to RS-232 mode. The following figure illustrates the JP3/JP4 jumper settings for RS-423 (default) interface.

![JP3/JP4 Jumper Settings](image)

**FIGURE C-19** JP3/JP4 Jumper Settings for RS-423 Interface

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Pins 1-2 Select</th>
<th>Pins 2-3 Select</th>
<th>Default Jumper on Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP3</td>
<td>RS-232</td>
<td>RS-423</td>
<td>2-3</td>
</tr>
<tr>
<td>JP4</td>
<td>RS-232</td>
<td>RS-423</td>
<td>2-3</td>
</tr>
</tbody>
</table>

To change the serial port jumper setting from RS-423 (default) to RS-232, refer to Section 8.7.2, “Replacing the Motherboard.”

C.7.2 Flash PROM Jumpers

Flash PROM jumpers JP1 and JP2 are used for reprogramming specific code blocks and remote programming of the flash PROM. The following figure illustrates the JP1/JP2 jumper settings (default) for the flash PROM and the following table identifies the flash PROM jumper settings. The default shunt settings of jumpers JP1 and JP2 are 1-2. Placing the shunt on pins 2 and 3 enables reprogramming of the flash PROM.
C.8 Enclosure

The system uses an enclosure that reflects style, ergonomics, serviceability, functionality, versatility, and quality. Physical orientation allows for a rack-mount, desktop, or under-desk installation. The enclosure design complies with all necessary environmental and regulatory specifications.

The Ultra 10 enclosure houses:
- One 3.5-inch (8.89-cm) diskette drive
- One 1.6-inch (4.064-cm) CD-ROM drive
- One 3.5-inch (8.89-cm) hard drive bay
- One plug-in UltraSPARC module
- Four DIMMs
- Four PCI slots
- One UPA64S module

### TABLE C-19 Flash PROM Jumper Settings

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Pins 1-2 Select</th>
<th>Pins 2-3 Select</th>
<th>Default Jumper on Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP1</td>
<td>To onboard PROM</td>
<td>To ROMBO</td>
<td>1-2</td>
</tr>
<tr>
<td>JP2</td>
<td>Disable (default)</td>
<td>Enable</td>
<td>1-2</td>
</tr>
</tbody>
</table>
Software Notes

Note – Systems with PGX24 graphics have "PGX24" or “Series 3” printed on the serial number label that is affixed to the system front bezel.

D.1 PGX24 8- or 24-Bit Graphics

The PGX24 offers PCI-based onboard 8-bit or 24-bit graphics. Selected features of the PCI-based onboard 8-bit or 24-bit graphics are described in the following paragraphs. (Also included is an m64 driver installation procedure that is required for systems running either the Solaris 2.5.1 Hardware: 11/97 or Solaris 2.6 5/98 operating environments.) Software support for PGX24 is included with Solaris 7.

Software support for version 2.5.1 Hardware: 11/97 or version 2.6 5/98 requires an update, which is included on the Sun Ultra 10 Software Supplement CD (704-6624). For patch installation instructions, refer to this appendix or the instructions in the CD-insert document included with that CD.

D.1.1 What Does 8-Bit or 24-Bit Frame Buffer Refer To?

The 8-bit or 24-bit graphics describes the number of graphics bits available to store the information for each pixel on the screen. The Ultra 5 onboard PGX24 graphics supports 8-bit or 24-bit colormapping. In contrast, the earlier Ultra 5 onboard PGX graphics only support 8-bit colormapping.
D.1.2 The Difference Between 8-Bit Mode and 24-Bit Mode on Ultra 5 Onboard Graphics

When in 8-bit mode, an 8-bit colormap is available. A main drawback of the 8-bit mode is colormap flashing. Because of the low number of colors, each application typically uses all the colors in the map. If two applications assigned different colors to the map, when one application is pulled into the foreground, the color map is changed and the colors of all the other open application windows change (i.e., flash) to use those in the map of the application just pulled into the foreground. The visual classes available for the 8-bit mode are: PseudoColor, StaticGray, StaticColor, GrayScale, TrueColor, and DirectColor. The 8-bit mode provides 256-different-colors availability at one time. All of the applications that run on previous Ultra 5 on-board frame buffers (PGX) are available.

When in 24-bit mode, a 24-bit colormap is available. The visual class available is TrueColor. The 24-bit mode provides up to 16.7 million different colors available at one time. The large number of colors available eliminate the colormap flashing. However, some of the applications that assume an 8-bit colormap do not initialize in 24-bit mode.

D.1.3 How to Install PGX24 Graphics Software on Solaris 2.5.1 HW:11/97

To load the Solaris 2.5.1 HW:11/97 PGX24 graphics software patch, patch 103792-15, proceed as follows:

1. Become super-user on the system.
2. Go to the directory that contains the patch by typing

   ```
   # ./cdrom/sun.Ultra_5_10_series_hw_ab/Patches/103792-15
   ```

3. Install the patch by typing

   ```
   # ./installpatch
   ```

4. Reboot the system.
5. Become super-user on the system.
6. Set the PGX24.graphics mode to 24-bit by typing

```
# m64config -depth 24 -res 1152x900x66
```

7. Either log out or exit the windowing system, then restart the windowing system.

When the windowing system starts up, the display will be in 24-bit mode.

**Note** – Software patches may be updated after the release of this product. You may contact Sun Enterprise Services, or go to the Sun Online Support Tools webpage, http://www.sun.com/service/online/, to obtain the latest software patch.

---

**D.1.4 How to Install PGX24 Graphics Software on Solaris 2.6 5/98**

To load the Solaris 2.6 5/98 PGX24 graphics software patch, patch 105362-13, proceed as follows:

1. Become super-user on the system.

2. Go to the directory that contains the patch by typing

```
# ./cdrom/sun_ultra_5_10_series_hw_ab/Patches/105362-13
```

3. Install the patch by typing

```
# ./installpatch .
```

4. Reboot the system.

5. Become super-user on the system.

6. Set the PGX24.graphics mode to 24-bit by typing

```
# m64config -depth 24 -res 1152x900x66
```
7. Either log out or exit the windowing system, then restart the windowing system. When the windowing system starts up, the display will be in 24-bit mode.

Note – Software patches may be updated after the release of this product. You may contact Sun Enterprise Services, or go to the Sun Online Support Tools webpage, http://www.sun.com/service/online/, to obtain the latest software patch.

D.1.5 Which Mode is Running

The output of the command:

```
% /usr/sbin/m64config -propt
```

tells you this information. depth 8 means that 8-bit mode is initialized. Likewise, depth 24 means that the 24-bit mode is active. The default setting is 8-bit mode.

D.1.6 Changing From One Mode to the Other

1. Exit the window system.

2. Enter the command:

```
% /usr/sbin/m64config -res <current resolution> -depth <8/24>
```

3. Check the current resolution by entering:

```
% /usr/sbin/m64config -prconf
```

4. Example 1 - To change from 8-bit to 24-bit mode:

```
% /usr/sbin/m64config -res 1152x900x66 -depth 24
```
5. Example 2 - To change from 24-bit to 8-bit mode:

```
% /usr/sbin/m64config -res 1152x900x66 -depth 8
```

**Note** – The `-res` option needs to be specified although the resolution is not changing.

**Note** – The maximum resolution supported by the 24-bit mode is 1152x900x76.

6. Restart the window system or reboot the machine.

---

**D.2 Solaris 2.5.1 and 2.6 Software Upgrades for Systems Faster Than 420 MHz**

If your system CPU speed is faster than 420 MHz, or if you upgrade with a replacement CPU module that is faster than 420 MHz, and your system is using either the Solaris 2.5.1 or 2.6 operating environments, software patches are required for those Solaris releases to run at the faster CPU speeds.

Systems with CPU speed faster than 420 MHz have the patch CDs shipped with them from the factory.

If you upgrade to a CPU faster than 420 MHz, you can order the software patch CDs using part number 704-6657 (for Solaris 2.5.1) or 704-6658 (for Solaris 2.6).

Refer to the installation instructions included with the CDs in the *Solaris 2.5.1 and 2.6 for 420+ MHz Systems Installation Guide*. 

---
# Glossary

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>address</td>
<td>A unique location within computer or peripheral memory. Reference made to an address is usually for retrieving or storing data.</td>
</tr>
<tr>
<td>APB</td>
<td>Advanced PCI bridge. A PCI-to-PCI bridge ASIC that features a connection path between a 32-bit bus operating at speeds up to 66 MHz on the primary interface and two 32-bit, 5 Vdc or 3.3 Vdc, PCI buses (each operating at 33 MHz), on the secondary interface.</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application-specific integrated circuit.</td>
</tr>
<tr>
<td>ASP</td>
<td>Authorized service provider.</td>
</tr>
<tr>
<td>AUXIO</td>
<td>Auxiliary IO. General purpose lines used to control miscellaneous system functions.</td>
</tr>
<tr>
<td>boot</td>
<td>A term used to identify the process of reading initial software into the computer.</td>
</tr>
<tr>
<td>boot PROM</td>
<td>In Sun workstations, contains the PROM monitor program, a command interpreter used for booting, resetting, low-level configuration, and simple test procedures.</td>
</tr>
<tr>
<td>CAS</td>
<td>Column address select.</td>
</tr>
<tr>
<td>CDE</td>
<td>Common Desktop Environment.</td>
</tr>
<tr>
<td>CD-ROM</td>
<td>Compact disc read-only memory.</td>
</tr>
<tr>
<td>DBZ</td>
<td>Double buffer with Z.</td>
</tr>
<tr>
<td>DCE</td>
<td>Data communication equipment. An external modem.</td>
</tr>
<tr>
<td>default</td>
<td>A preset value that is assumed to be correct unless changed by the user.</td>
</tr>
<tr>
<td>DIMM</td>
<td>Dual in-line memory module. A small printed circuit card that contains dynamic random access memory chips.</td>
</tr>
<tr>
<td>DMA</td>
<td>Direct memory address.</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>DOC</td>
<td>Department of communications.</td>
</tr>
<tr>
<td>dpi</td>
<td>Dots per inch.</td>
</tr>
<tr>
<td>DRAM</td>
<td>Dynamic random-access memory. A read/write dynamic memory in which the data can be read or written in approximately the same amount of time for any memory location.</td>
</tr>
<tr>
<td>DTAG</td>
<td>Dual tag or data tag.</td>
</tr>
<tr>
<td>DTE</td>
<td>Data terminal equipment.</td>
</tr>
<tr>
<td>EBus</td>
<td>Extension bus.</td>
</tr>
<tr>
<td>ECC</td>
<td>Error checking code.</td>
</tr>
<tr>
<td>EDO</td>
<td>Extended data out.</td>
</tr>
<tr>
<td>EIDE</td>
<td>Enhanced IDE.</td>
</tr>
<tr>
<td>EMI</td>
<td>Electrostatic magnetic interference. Electrical phenomena that directly or indirectly contributes to a degradation in performance of an electronic system.</td>
</tr>
<tr>
<td>Ethernet</td>
<td>A type of network hardware that provides communication between systems connected directly together by transceiver taps, transceiver cables, and various cable types such as coaxial, twisted-pair, and fiber-optic.</td>
</tr>
<tr>
<td>FBC</td>
<td>Frame buffer controller. An ASIC responsible for the interface between the UPA and the 3DRAM. Also controls graphic draw acceleration.</td>
</tr>
<tr>
<td>FCC</td>
<td>Federal communications commission.</td>
</tr>
<tr>
<td>FIFO</td>
<td>First-in-first-out.</td>
</tr>
<tr>
<td>flash PROM</td>
<td>Flash programmable read-only memory.</td>
</tr>
<tr>
<td>Gbyte</td>
<td>Gigabyte.</td>
</tr>
<tr>
<td>GUI</td>
<td>Graphical user interface.</td>
</tr>
<tr>
<td>IDC</td>
<td>Insulation displacement connector.</td>
</tr>
<tr>
<td>IDE</td>
<td>Intergrated drive electronics.</td>
</tr>
<tr>
<td>I/O</td>
<td>Input/output.</td>
</tr>
<tr>
<td>JTAG</td>
<td>IEEE standard 1149.1.</td>
</tr>
<tr>
<td>Kbyte</td>
<td>Kilobyte.</td>
</tr>
<tr>
<td>LAN</td>
<td>Local area network.</td>
</tr>
<tr>
<td>LED</td>
<td>Light-emitting diode.</td>
</tr>
<tr>
<td>MAC</td>
<td>Media access controller.</td>
</tr>
</tbody>
</table>
**Mbyte**  Megabyte.

**MBps**  Megabyte per second.

**Mbps**  Megabit per second.

**MCU**  Memory controller unit.

**MHz**  Megahertz.

**MII**  Media independent interface.

**ns**  Nanosecond.

**NVRAM**  Non-volatile random access memory. Stores system variables used by the boot PROM. Contains the system hostID number and Ethernet address.

**OBP**  OpenBoot PROM. A routine that tests the network controller, diskette drive system, memory, cache, system clock, network monitoring, and control registers.

**PCI**  Peripheral component interconnect. A high-performance 32- or 64-bit-wide bus with multiplexed address and data lines.

**PCIO**  PCI-to-EBus/Ethernet controller. An ASIC that bridges the PCI bus to the EBus, enabling communication between the PCI bus and all miscellaneous I/O functions, as well as the connection to slower on-board functions.

**PCMCIA**  Personal Computer Memory Card International Association.

**PID**  Process ID.

**POR**  Power-on reset.

**POST**  Power-on self-test. A series of tests that verify motherboard components are operating properly. Initialized at system power-on or when the system is rebooted.

**RAMDAC**  RAM digital-to-analog converter. An ASIC responsible for direct interface to 3DRAM. Also provides onboard phase-lock loop (PLL) and clock generator circuitry for the pixel clock.

**RAS**  Row address select.

**RC**  Resistive-capacitive.

**RISC**  Reset, interrupt, scan, and clock. An ASIC responsible for reset, interrupt, scan, and clock.

**SB**  Single buffer.

**SDRAM**  Synchronous DRAM.

**SGRAM**  Synchronous graphics RAM.
<table>
<thead>
<tr>
<th><strong>SRAM</strong></th>
<th>Static random access memory.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Standby switch</strong></td>
<td>Controls the standby state of the system.</td>
</tr>
<tr>
<td><strong>STP</strong></td>
<td>Shielded twisted-pair.</td>
</tr>
<tr>
<td><strong>SunVTS</strong></td>
<td>A diagnostic application designed to test hardware.</td>
</tr>
<tr>
<td><strong>TIP connection</strong></td>
<td>A connection that enables a remote shell window to be used as a terminal to display test data from a system.</td>
</tr>
<tr>
<td><strong>TPE</strong></td>
<td>Twisted-pair Ethernet.</td>
</tr>
<tr>
<td><strong>TOD</strong></td>
<td>Time of day. A timekeeping integrated circuit.</td>
</tr>
<tr>
<td><strong>TTL</strong></td>
<td>Transistor-transistor logic.</td>
</tr>
<tr>
<td><strong>UPA</strong></td>
<td>UltraSPARC port architecture. Provides processor-to-memory interconnection.</td>
</tr>
<tr>
<td><strong>UTP</strong></td>
<td>Unshielded twisted-pair.</td>
</tr>
<tr>
<td><strong>VCCI</strong></td>
<td>Voluntary control council for interference.</td>
</tr>
<tr>
<td><strong>VIS</strong></td>
<td>Visual instruction set.</td>
</tr>
<tr>
<td><strong>Vrms</strong></td>
<td>Volts root-mean-square.</td>
</tr>
</tbody>
</table>
Index

NUMERICS
10-/100-Mbit Ethernet, C-5
  functional block diagram, C-6

A
all above output message, 4-27
APB ASIC, C-5, C-19
ASIC
  APB, C-5, C-19
  PCIO, C-5, C-19
  RISC, C-20
attaching wrist strap
to chassis (Ultra 10), 5-10
audio, 4-25, C-24
  cable assembly
    removing, 6-9
    replacing, 6-10
  circuit functional block diagram, C-25
  connector
    line assignments, B-12
    pin configuration, B-12
  input electrical specification, C-25
  output electrical specification, C-25
  audio output message, 4-25

B
baud rate, verifying, 3-4
  block diagram
    motherboard, C-37
  bypassing POST, 3-22

C
cabling configuration
  CD-ROM drive, A-6
  cabling configuration, Ultra 10 hard drive, A-7
  CD-ROM drive
    failure, 4-4
    removing, 7-13
    replacing, 7-14
  CD-ROM drive cabling configuration, A-6
  commands, keyboard control, 3-22
  common features, 1-2
  communications controller serial ports functional
    block diagram, C-23
  compliance
    German acoustic, xxvii
  components, system unit, 1-6
cover, top
  removing, 5-8
  replacing, 10-1
CPU
  fan assembly
removing, 6-13
replacing, 6-14
module, C-3
removing, 8-1
replacing, 8-3

D
description
functional, C-1
product, 1-1
signal, B-1
SunVTS, 2-1
diag-level
variable
set to max, 3-7
set to min, 3-15
diagnostics, OBP on-board, 4-8
DIMM
bank location, 8-6
characteristics, C-12
failure, 4-7
physical memory address, 4-7
removing, 8-6
replacing, 8-8
slot pair location, 8-6
diskette drive
cable assembly
removing, 6-4
replacing, 6-6
removing, 7-1
replacing, 7-2
drive bracket
removing, 6-17
interface, C-6
EIDE
cable
configuration support, C-8
electrical requirements, C-7
labeling, C-8
interface, C-7
functional block diagram, C-7
electrical specification
audio input, C-25
audio output, C-25
electrical specifications, A-2
Ultra 10, A-2
electrostatic discharge, 5-4
Elite3D m3 Lite
patch information, 8-11
enclosure, C-40
environmental
requirements, A-5
error reporting, POST, 3-19
Ethernet, 4-19
output message, 4-20
external UTP-5 cable lengths, B-6

F
failure
CD-ROM drive, 4-4
DIMM, 4-7
hard drive, 4-4
power-on, 4-2
video output, 4-3
features
common, 1-2
flash PROM, C-23
jumper settings, C-40
jumpers, C-39
floppy, 4-21
output message, 4-21
front
panel on/off switch, C-26

Index-2  Sun Ultra 10 Service Manual • February 2000
initializing POST, 3-5
internal drives identification, 4-4

J
J12 connector
   pin assignments, B-2
   pin configuration, B-2
J17 connector
   pin assignments, 4-6
   pin configuration, 4-6
jumper
descriptions, C-38
   pins
      identifying, C-38
      settings
         flash PROM, C-40
         RS-423 interface, C-39
         serial port, 8-20, C-39
jumpers
   flash PROM, C-39
   serial port, C-39

K
keyboard, 4-20
   LED patterns, 3-19
   output message, 4-20
   Sun Type-5, 5-6, 10-4
keyboard standby key, C-26
keyboard/mouse connector
   pin assignments, B-4
   pin configuration, B-4

L
LEDs, 3-5, 3-6, 5-7, 10-5
   patterns, keyboard, 3-19
line assignments, audio connector, B-12
lithium battery, 5-4
M
major subassemblies, 6-1
maximum level of POST, 3-7
memory
  address assignments, C-13
  architecture, C-10
  DIMM configuration, C-12
  interface
    functional block diagram, C-11
minimum level of POST, 3-7
minitower workstation, Ultra 10, 1-2
mirroring hard drives, 7-8
modem
  setting up, A-2
  setup specifications, A-2
modification to equipment, 5-3
motherboard
  block diagram, C-37
  component replacement, 8-1
  initializing POST, 3-23
  removing, 8-17
  replacement, 8-1
  replacing, 8-19
mouse
  output message, 4-21

N
NVRAM, 4-25
  output message, 4-25
NVRAM/TOD, C-24
  functional block diagram, C-24
  removing, 8-4
  replacing, 8-5

O
OBDiags, 4-13
  all above, 4-27
  audio, 4-25
  EBus
    DMA registers, 4-19
    TCR registers, 4-19
  Ethernet, 4-19
  floppy, 4-21
  IDE, 4-26
  keyboard, 4-20
  mouse, 4-21
  NVRAM, 4-25
  parallel port, 4-22
  PCI/PCIO, 4-18
  serial port A, 4-22
  serial port B, 4-24
  OBP on-board diagnostics, 4-8
    probe-ide, 4-10
    selected tests, 4-11
    watch-clock, 4-8
    watch-net, 4-8
    watch-net-all, 4-8
  on/off switch
    front panel, C-26
    power supply, C-26
  on-board voltage regulator, C-36
  OpenBoot diagnostics, 4-13
  operation
    SunVTS, 2-2
  output message
    all above, 4-27
    audio, 4-25
    Ethernet, 4-20
    floppy, 4-21
    ide, 4-26
    keyboard, 4-20
    mouse, 4-21
    NVRAM, 4-25
    parallel port, 4-22
    PCI/PCIO, 4-18
    probe-ide, 4-10
    serial port A, 4-22
Index-5

serial port A with TIP line, 4-23
serial port B, 4-24
test, 4-11
watch-clock, 4-8
watch-net, 4-9
watch-net-all, 4-9
overview
POST, 3-1
SunVTS, 2-1

P
parallel port, 4-22, C-22
  connector
    pin assignments, B-10
    pin configuration, B-10
  output message, 4-22
parts list, illustrated, 9-1
patch information, Elite3D m3 Lite, 8-11
PCI
  bus
    primary, C-5
    secondary, C-5
  card
    removing, 8-12
    replacing, 8-13
PCI/PCIO, 4-18
PCI/PCIO output message, 4-18
PCI-based graphics, C-9
PCI-based graphics (PGX)
  functional block diagram, C-9
PCI-based graphics (PGX24)
  functional block diagram, C-9
PCI-IDE
  interface, C-4
PCIO ASIC, C-5, C-19
physical dimensions
  Ultra 10, 1-4
  Ultra 5, 1-4
physical specifications, A-1
  Ultra 10, A-1
pin assignments
  connector J12, B-2
  J17 connector, 4-6
  keyboard/mouse connector, B-4
  parallel port connector, B-10
  riser board, C-15
  serial port B connector, B-9
  TPE connector, B-5
  video connector, B-13
pin configuration
  audio connector, B-12
  connector J12, B-2
  J17 connector, 4-6
  keyboard/mouse connector, B-4
  parallel port connector, B-10
  serial port A connector, B-7
  serial port B connector, B-9
  TPE connector, B-5
  video connector, B-13
placement of Sun product, 5-3
POST
  bypassing, 3-22
  error reporting, 3-19
  initializing, 3-5
  maximum level, 3-7
  minimum level, 3-7
  motherboard, initializing, 3-23
  overview, 3-1
  progress reporting, 3-19
power, C-36
  cord connection, 5-3
  management, C-36
  on/off switch, system unit, 5-7, 10-3
  supply on/off switch, C-26
  supply, test, 4-5
  switching, C-26
power supply
  removing, 6-1
  replacing, 6-3, 6-19
power supply (Ultra 10)
removing and replacing, 6-2
powering
  off the system unit, 5-5
  on the system unit, 10-3
power-on
  failure, 4-2
  self-test, 3-1
preface, xix
pre-POST preparation, 3-2
primary PCI bus, C-5
probe-ide diagnostic output message, 4-10
procedures, troubleshooting, 4-1
product
  description, 1-1
  specifications, A-1
progress reporting, POST, 3-19

R
rear view
  Ultra 10 system unit, 1-5
reference information, A-6
related documents, xxiii
removing
  audio cable assembly, 6-9
  CD-ROM drive, 7-13
  CPU fan assembly, 6-13
  CPU module, 8-1
  DIMM, 8-6
  diskette drive, 7-1
    cable assembly, 6-4
    drive bracket, 6-17
  front bezel (Ultra 10), 6-16
  hard drive, 7-4
    cable assembly, 6-6
    motherboard, 8-17
  NVRAM/TOD, 8-4
  PCI card, 8-12
  power supply, 6-1
  rear drive bracket (Ultra 10), 6-18
  riser board, 8-15
  serial/parallel cable assembly, 6-8
  speaker assembly, 6-11
  top cover, 5-8
  UPA graphics card, 8-9
removing and replacing
  audio cable (Ultra 10), 6-10
  CD-ROM drive (Ultra 10), 7-14
  CPU fan assembly (Ultra 10), 6-14
  CPU module (Ultra 10), 8-3
  DIMM (Ultra 10), 8-7
  diskette drive (Ultra 10), 7-2
  diskette drive cable (Ultra 10), 6-5
  hard drive (Ultra 10 chassis front), 7-6
  hard drive (Ultra 10 chassis rear), 7-5
  hard drive cable (Ultra 10), 6-7
  motherboard (Ultra 10), 8-19
  NVRAM/TOD (Ultra 10), 8-5
  PCI card (Ultra 10), 8-13
  power supply (Ultra 10), 6-2
  riser board (Ultra 10), 8-16
  serial/parallel cable (Ultra 10), 6-8
  speaker assembly (Ultra 10), 6-12
  UPA graphics card (Ultra 10), 8-10
  upper and lower bezels (Ultra 10), 5-12
replaceable components
  Ultra 10, 1-6
  Ultra 5, 1-6
replacing
  audio cable assembly, 6-10
  CD-ROM drive, 7-14
  CPU fan assembly, 6-14
  CPU module, 8-3
  DIMM, 8-8
  diskette drive, 7-2
    cable assembly, 6-6
  front bezel (Ultra 10), 6-16
  hard drive, 7-6
    cable assembly, 6-7
motherboard, 8-19
NVRAM/TOD, 8-5
PCI card, 8-13
power supply, 6-3, 6-19
rear drive bracket (Ultra 10), 6-18
riser board, 8-16
serial/parallel cable assembly, 6-9
speaker assembly, 6-12
top cover, 10-1
UPA graphics card, 8-10
requirements, environmental, A-5
RISC ASIC, C-20
riser board
connector definition, C-15
pin assignment, C-15
pin summary, C-15
removing, 8-15
replacing, 8-16

S
safety
precautions
electrostatic discharge, 5-4
lithium battery, 5-4
modification to equipment, 5-3
placement of Sun product, 5-3
power cord connection, 5-3
requirements, 5-2
secondary PCI bus, C-5
selected jumper settings, C-38
serial
communications controller, C-23
port
A connector, B-7
B connector, B-9
jumper settings, 8-20, C-39
jumpers, C-39
speed change, A-3
port A, 4-22
connector
pin assignments, B-7
pin configuration, B-7
output message, 4-22
output message with TIP line, 4-23
port B, 4-24
connector
pin assignments, B-9
pin configuration, B-9
output message, 4-24
serial ports/keyboard and mouse, C-22
serial/parallel
cable assembly
removing, 6-8
replacing, 6-9
setting up
modem, A-2
tip connection, 3-2
shell prompts, xxii
signal descriptions, B-1
speaker assembly
removing, 6-11
replacing, 6-12
specifications
electrical, A-2
physical, A-1
product, A-1
standard serial port functional block diagram, C-22
standby
switch, system unit, 5-6, 10-4
standby switching, C-26
storage devices, 7-1
Sun
Type-5 keyboard, 5-6, 10-4
type-5 keyboard, 3-5
type-5 keyboard LEDs, 3-5
Type-6 keyboard, 3-6, 5-7, 10-5
Type-6 keyboard LEDs, 3-6, 5-7, 10-5
SunVTS
description, 2-1
operation, 2-2
overview, 2-1
SuperIO, C-22
supported
  Ultra 10 configuration, C-8
symbols, 5-2
system
  reset functional block diagram, C-21
  unit, C-1
  components, 1-6
  features, 1-4
  functional block diagram, C-2
  power on/off switch, 5-7, 10-3
  standby switch, 5-6, 10-4
system unit
  replaceable components, 9-3

T
  test
    power supply, 4-5
  test diagnostic output message, 4-11
  tip connection, setting up, 3-2
  tools required, 5-5
TPE
  cable-type connectivity, B-6
  connector
    pin assignments, B-5
    pin configuration, B-5
  transceivers, C-14
  troubleshooting procedures, 4-1
  typical error code failure message, 3-20
  typographic conventions, xxii

U
  Ultra 10
    electrical specifications, A-2
    minitower workstation, 1-2
    physical dimensions, 1-4
    physical specifications, A-1
    replaceable components, 1-6
    system unit
      front view, 1-5
  rear view, 1-5
  Ultra 10 hard drive cabling configuration, A-7
  Ultra 5
    physical dimensions, 1-4
    replaceable components, 1-6
  UPA, C-4
    graphics card
      removing, 8-9
      replacing, 8-10
    graphics card (Ultra 10 only), 4-12
    graphics card (Ultra 10), 8-9
  UPA graphics
    functional block diagram, C-4
  V
    verifying baud rate, 3-4
    video connector
      pin assignments, B-13
      pin configuration, B-13
    video output failure, 4-3
  W
    watch-clock diagnostic, 4-8
    watch-clock diagnostic output message, 4-8
    watch-net diagnostic, 4-8
    watch-net diagnostic output message, 4-9
    watch-net-all diagnostic, 4-8
    watch-net-all diagnostic output message, 4-9
    wrist strap, attaching
      to chassis (Ultra 10), 5-10