Netra™ CP3010 Board User's Guide

Sun Microsystems, Inc.
www.sun.com

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Preface

The *Netra CP3010 Board User's Guide* describes the hardware specifications, function, and physical properties of the Netra™ CP3010 board. The *Netra CP3010 Board User's Guide* is written for system integration engineers, field applications and service engineers, and others involved in the integration of these boards into systems.

How This Document Is Organized

Chapter 1 provides an overview of the Netra CP3010 board.

Chapter 2 provides instructions on hardware installation.

Chapter 3 provides instructions on the software configuration.

Chapter 4 provides information about the Netra CP3010 firmware.

Chapter 5 provides hardware and functional descriptions of the Netra CP3010 board.

Appendix A provides information about the physical characteristics of the Netra CP3010 board.

Appendix B describes the Sun-specific OEM-defined Intelligent Platform Management Interface (IPMI) commands.

Using UNIX Commands

This document might not contain information on basic UNIX® commands and procedures such as shutting down the system, booting the system, and configuring devices. Refer to the following for this information:

- Software documentation that you received with your system
- Solaris™ Operating System documentation, which is at:

  `http://docs.sun.com`

Shell Prompts

Shell	Prompt
C shell	*machine-name*%
C shell superuser	*machine-name*#
Bourne shell and Korn shell	$
Bourne shell and Korn shell superuser	#

Typographic Conventions

Typeface*	Meaning	Examples
`AaBbCc123`	The names of commands, files, and directories; on-screen computer output	Edit your `.login` file. Use `ls -a` to list all files. `% You have mail.`
`AaBbCc123`	What you type, when contrasted with on-screen computer output	`% su` `Password:`
AaBbCc123	Book titles, new words or terms, words to be emphasized. Replace command-line variables with real names or values.	Read Chapter 6 in the *User's Guide*. These are called *class* options. You *must* be superuser to do this. To delete a file, type `rm` *filename*.

* The settings on your browser might differ from these settings.

Related Documentation

For additional information about the Netra CP3010 board and the Netra CP30x0 rear transition card, refer to the following documents.

Title	Part Number
Netra CP3010 Board Product Notes	819-1181-xx
Netra CP3010 Board Getting Started Guide	819-1182-xx
Netra CP3010 Board Programming Guide	819-1185-xx
Netra CP30x0 Rear Transition Card Getting Started Guide	819-1186-xx
Netra CP30x0 Rear Transition Card User's Guide	819-1187-xx
OpenBoot PROM Enhancements for Diagnostic Operation	817-6957-xx
Important Safety Information for Sun Hardware Systems (printed version only)	816-7190-10

Except for the *Important Safety Information for Sun Hardware Systems*, all the documents listed are available online at:

`http://www.sun.com/documentation`

Documentation, Support, and Training

Sun Function	URL
Documentation	http://www.sun.com/documentation/
Support	http://www.sun.com/support/
Training	http://www.sun.com/training/

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Netra CP3010 Board User's Guide, part number 819-1183-10

CHAPTER 1

Introduction to the Netra CP3010 Board

This chapter contains the following sections:

1.1 Overview of the Netra CP3010 Board

The Netra™ CP3010 board is a high-performance single-board computer based on two UltraSPARC® IIIi processors and designed for high availability in a switched network computing environment. This board is compliant with Advanced Telecom Computing Architecture® (ATCA) specifications (PICMG® 3.0 and PICMG 3.1) and can achieve greater performance levels than compactPCI (cPCI) standards-based products targeted for telco markets.

The PICMG (PCI Industrial Computer Manufacturers Group) standards committee has developed the new standard ATCA (or PICMG 3.x) to address the issues posed by previous standards based on cPCI and cPSB (PICMG 2.x). The PICMG 3.x specification brought the following changes to the existing PICMG 2.x family of products:

- Larger board space (8U high compared to 6U for cPCI), which allows more features and processing power
- On-board power supplies deriving local power from redundant –48V power from the midplane (rather than separate power supplies)
- 6 HP slot width, allowing greater component height and new PCI Mezzanine card (PMC) options

- Elimination of PCI connectivity between the boards in the system and reallocation of connectivity to serial interconnects, eliminating single points of failure in the system
- Mandatory use of Intelligent Platform Management Interface (IPMI) management interfaces
- Flexible user I/O
- Power and thermal management guidelines enforced by the management infrastructure
- Separation of control and data traffic by supporting Base Fabric (PICMG 3.0) and Extended Fabric (PICMG 3.1) interfaces

The ATCA standard consists of the PICMG 3.0, PICMG 3.1, PICMG 3.2, and PICMG 3.3 specifications. The Netra CP3010 board complies with:

- PICMG 3.0, the base specification that defines the mechanical, power distribution, system management, data transport, and regulatory guidelines
- PICMG 3.1, which builds upon the PICMG 3.0 base specification and the IEEE 802.3-2003 standard

1.2 Features of the Netra CP3010 Board

The Netra CP3010 board provides two 10/100BASE-T Ethernet interfaces for the Base Fabric interface (a requirement of PICMG 3.0) and two serializer, deserializer (SERDES) gigabit Ethernet interfaces (PICMG 3.1) for the Extended Fabric interface. The Base Fabric interface is used as the control interface and the Extended Fabric interface can be used for data traffic. Both Base Fabric and Extended Fabric interfaces are configured as Dual Star configurations.

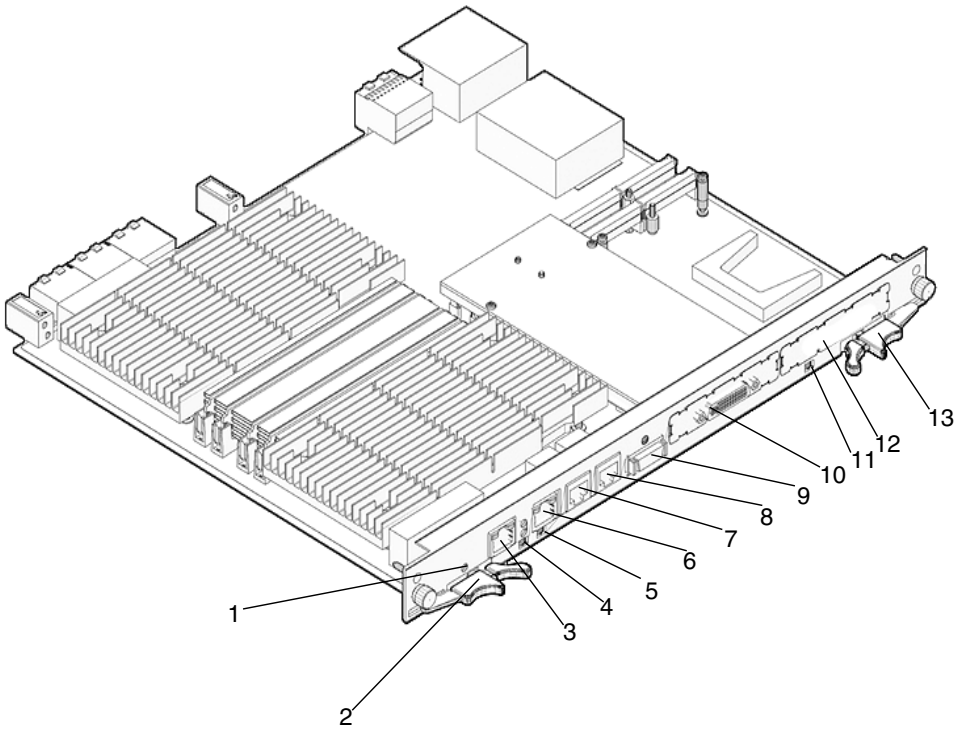
Netra CP3010 board features include:

- Single or dual UltraSPARC IIIi+ processors
- DDR-1 memory, up to 8 Gbytes (Very Low Profile DIMMs)
- JBus-PCI ASICs (application-specific integrated circuits) to bridge processors and the PCI I/O subsystem
- Two PCI Mezzanine card (PMC) expansion slots that support PCI I/O expansion and storage PMC modules
- Two-channel Serial Attached SCSI (SAS) port for external storage access (2X front and rear)
- Two 10/100BASE-T Ethernet interfaces as maintenance ports
- Two asynchronous serial ports

- Compact Flash socket to support a 1-Gbyte or 2-Gbyte user flash type I memory card
- Management support using Pigeon Point Systems Intelligent Platform Management (IPM) controller, providing a redundant IPMI channel to communicate with the ATCA shelf manager
- Rear I/O access using a compatible rear transition card (RTC)

FIGURE 1-1 and FIGURE 1-2 show the Netra CP3010 board.

FIGURE 1-1 Dual Processor Netra CP3010 Board (Front View)



1 - Reset button
2 - Top latch
3 - Serial port A (RJ-45, ttya)
4 - Out of Service LED (yellow)
5 - OK LED (green)
6 - Serial port B (RJ-45, ttyb)
7 - Ethernet port A (RJ-45, net2)
8 - Ethernet port B (RJ-45, net3)
9 - SAS 2x port
10 - PMC A (with PMC installed)
11 - Hot-Swap LED (blue)
12 - PMC B (with filler panel)
13 - Hot-Swap switch and bottom latch

FIGURE 1-2 Netra CP3010 Board (Top View)

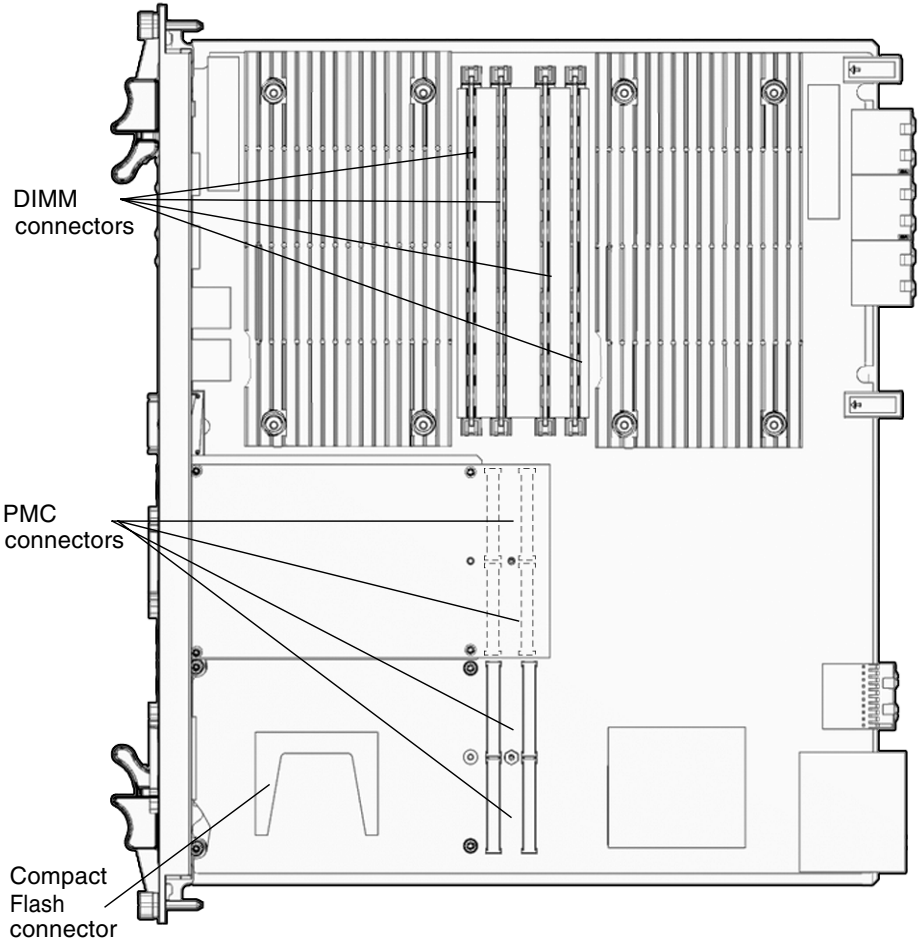


TABLE 1-1 lists features of the board.

TABLE 1-1 Feature Summary for the Netra CP3010 Board

Feature	Description
CPU	• Two UltraSPARC IIIi processors • CPU core speed: 1.0 GHz • Both processors operate at the same speed
Memory	• Four DDR-1 184-pin Very Low Profile (VLP) DIMMs, buffered, registered • 1-Gbyte or 2-Gbyte DIMMs, for a total memory of 4 or 8 Gbytes for two CPU configurations • ECC supported
Power requirement	ATCA 3.0 standard of 200 watts maximum
PICMG and PMC compliance	• PICMG 3.0 R1.0 • PICMG 3.1 R1.0 • PCI Mezzanine Card (PMC) IEEE P1386.1/Draft 2.3 • PICMG 2.15 R1.0 (PCI Telecom Mezzanine/Carrier Card [PTMC] standard)
Node board support	The board functions as a CPU node board with the Solaris software package
Operating system	Solaris 10 OS Solaris 9 9/05 OS and subsequent compatible versions with supported Netra patches
Internal I/O (connections to ATCA midplane)	• Dual gigabit Ethernet for Base Fabric interface • Dual SERDES interface as Extended Fabric interface • Dual IPMI channel connects to the midplane for communicating with the Shelf Management card
External I/O	• Two 10/100 Mbps Ethernet ports for maintenance (front or rear) • Two asynchronous serial ports (front and rear) • Dual 2X SAS ports (one front and one rear), speed: 300 Mbps per channel • Rear access support using Netra CP30x0 rear transition card: –CP3010 front I/O is redirected to rear when RTC is present. –Serial port access is available in front and rear when RTC is present. It is available only in front when no RTC is present. –2X SAS port is available in front and rear (RTC required) at all times. • PMC I/O rear access requires corresponding PIMs: –Majority of PMC I/O is routed to RTC as single-ended signals. –Others are routed as differential pairs to support certain Fibre Channel PMC cards.

TABLE 1-1 Feature Summary for the Netra CP3010 Board

Feature	Description
IPMI system management	Uses IPMI communications with baseboard management controller (BMC); performs advanced system monitoring (ASM) on local board interface (for example, temperature sense, FRU ID, and control)
Hot-swap support	Basic, full, and high-availability (HA) hot-swap support
Front panel access	• Two serial ports (SubDB-9) • Two 10/100BASE-T Ethernet ports (RJ-45) • Two PMC I/O access panels • One 2X SAS port (via 4X external SAS connector) • Recessed reset push button
PMC I/O	Provision for adding up to two independent hardware vendor (IHV) supplied PMC expansion ports on front panel
NVRAM	8-Kbyte nonvolatile inter-integrated circuit (I^2C) serial EEPROM to save OpenBoot™ PROM configuration.
System flash	2 Mbytes on board
User flash	14 Mbytes on board
Building compliance	Network Equipment Building Systems (NEBS) Level 3
Flash update	Supported from downloaded file

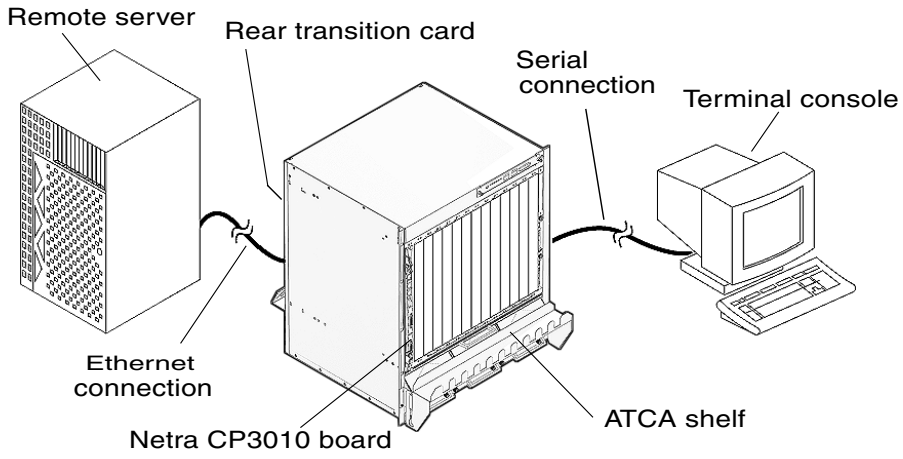
Note – For EMI compliance of front access ports, use shielded cables on all I/O ports. The shields for all shielded cables must be terminated on both ends.

1.3 Netra CP3010 Board System Configurations

Netra CP3010 boards can be installed in an ATCA shelf (or chassis), shown in FIGURE 1-3. The boards can be deployed in various electrical configurations to suit each end-user requirement. For example, the board can be configured to boot from a network as a diskless client with either a front panel or rear transition card network connection, or from an optional Compact Flash card. Alternatively, industry-standard PCI Mezzanine card (PMC) and PCI Interface Module (PIM)

hardware from IHVs can be installed to provide local disk I/O, which can be used optionally as a boot path. The Netra CP3010 board has fixed on-board memory and connectors for additional memory.

FIGURE 1-3 Netra CP3010 Board in an ATCA Shelf Enclosure



Diskless client that boots through network from a remote server

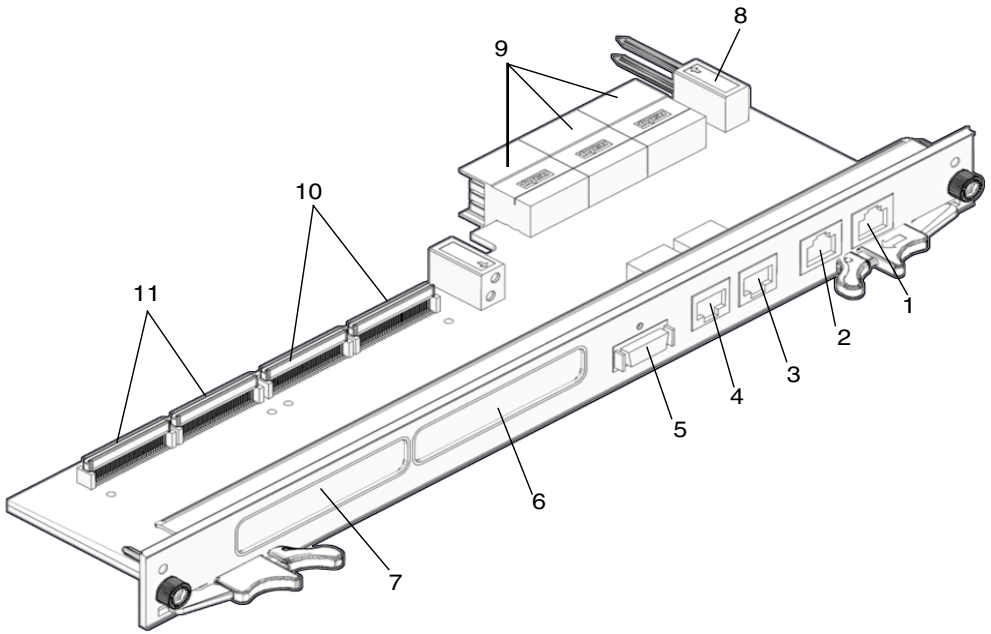
1.3.1 PMC and PIM Modules

The Netra CP3010 board has two PMC slots to provide additional I/O to the front panels or to the rear of the enclosure when used with a rear transition card. PMC modules decode their custom I/O from the Netra CP3010 board's on-board PCI bus A signals. A rear transition card can also be fitted with PIMs to bring I/O channels to the rear of the unit. See Section A.6.2, "PMC Connectors " on page A-9 for more information.

1.3.2 Rear Transition Card

The optional Netra CP30x0 rear transition card installs into the rear of the ATCA enclosure, opposite the Netra CP3010 board (see FIGURE 1-5). The card connects with the host Zone 3 rear I/O connectors and carries two serial ports, two Dual gigabit Ethernet (GbE) ports with RJ-45 connectors, and a two-channel SAS port to its rear-panel flange (see FIGURE 1-4).

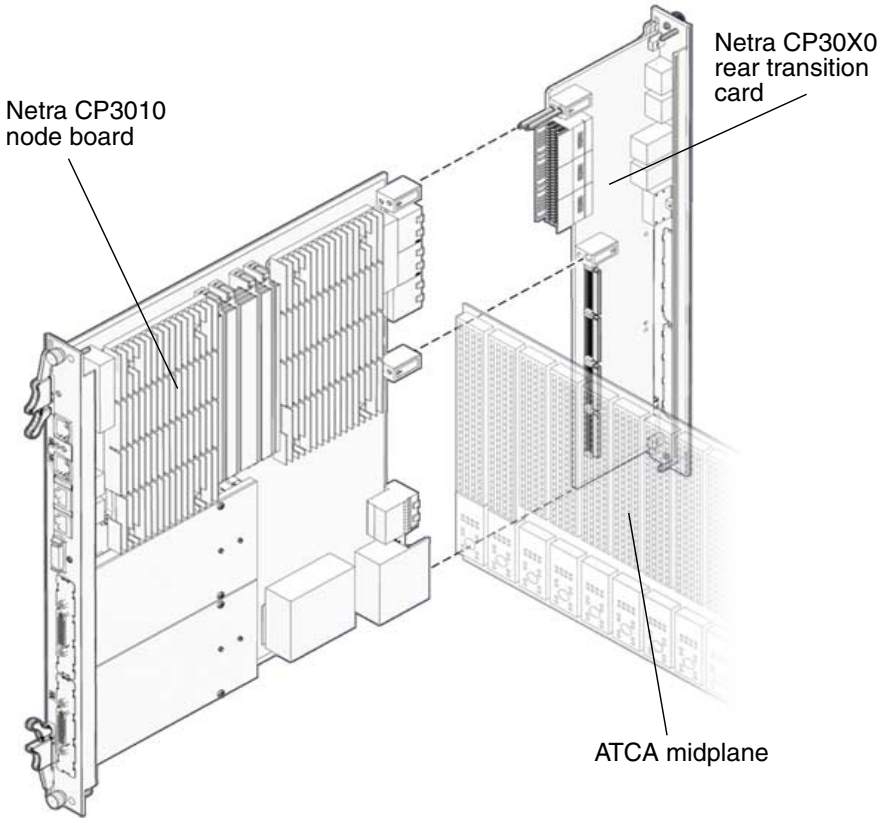
FIGURE 1-4 Netra CP30x0 Rear Transition Card



1 - Serial port A (RJ-45)
2 - Serial port B (RJ-45)
3 - Ethernet port A (RJ-45)
4 - Ethernet port B (RJ-45)
5 - SAS port (2x)
6 - PIM B cutout
7 - PIM A cutout
8 - Alignment pin
9 - Zone 3 connectors
10 - PIM B connectors
11 - PIM A connectors

FIGURE 1-5 shows the physical relationship between the board, rear transition card, and the midplane in a typical ATCA system.

FIGURE 1-5 Relationship of the Netra CP3010 Board, Midplane, and Rear Transition Card



Note – When the rear transition card is used with the Netra CP3010 board, shielded cables are required for serial I/O ports. Unshielded cables can be used on Ethernet ports to satisfy EMI compliance standards. The shields for all shielded cables must be terminated on both ends.

The rear transition card can also be fitted with PIM modules that are configured to bring I/O channels to the unit's rear panel. A PIM hardware kit includes a card for the PMC slot and a card for the PIM slot on the rear transition card. A PIM is a rear-panel extension added to a PMC module. When the PIM I/O is configured, the front PMC I/O output is not accessible.

The customer can order the Netra CP30x0 rear transition card, build a custom card, or buy from an IHV. A minimal set of I/O must provide a boot path for the host board and a path for console I/O to deliver commands and to read board and system status.

Possible boot and console configurations are described in TABLE 1-2. Sun Microsystems provides the Netra CP3010 board and a compatible Netra CP30x0 rear transition card. This card provides two 10/100BASE-T Ethernet RJ-45 ports from the host to the rear of the system, which can optionally be used to accomplish a network boot as a diskless client. The other configurations require IHV hardware.

TABLE 1-2 I/O Configurations

I/O	Hardware Required	Description
Ethernet	Netra CP30x0 rear transition card—supplied as an option for rear access	Default boot path uses the Ethernet port; the board runs in diskless client configuration.
SCSI	Netra CP30x0 rear transition card; PMC SCSI I/O	SCSI devices can be used for local booting; requires optional rear transition card with PMC SCSI I/O.
Serial data	Netra CP3010 board	Serial ports on front panel provide a path for a console I/O. Both serial ports can be used on either the CP3010 board or CP30X0 transition card, but the same port should not be used on both. If serial port A is used on the CP3010 board, serial port A on the CP30X0 rear transition card should not be used.
	Netra CP30x0 rear transition card	
Compact Flash	Sun Compact Flash card	The Compact Flash connector can be used to add an optional 1-or 2-Gbyte user flash type I memory card.

1.4 Hot-Swap Support

This section briefly discusses the hot-swap support on the Netra CP3010 board.

See the PICMG *CompactPCI Hot Swap Specification,* which provides a detailed description of this subject. In general, the hot-swap process includes the orderly connection of the hardware and software.

This process uses hardware connection control to connect the hardware in an orderly sequence. The process includes the use of backplane pins of different lengths to accomplish signal sequencing, protect the hardware, and avoid corrupting the backplane bus.

There are three hot-swap models described in the PICMG *CompactPCI Hot Swap Specification*: basic hot-swap, full hot-swap, and high-availability (HA) hot-swap.

1.5 System Requirements

This section contains the system-level hardware and software requirements for the Netra CP3010 board.

1.5.1 Hardware Requirements

Sun provides the following items for customer order:

- Netra CP3010 node board
- Netra CP30x0 rear transition card (optional)

  The rear transition card enables rear system I/O access to the network, to a boot device, and to a console terminal (shown in FIGURE 1-4). Refer to the *Netra CP30x0 Rear Transition Card User's Guide* (819-1187) for more information.

  This rear transition card is optional and must be ordered separately from the Netra CP3010 board.
- Compact Flash card (optional)

  An IDE Compact Flash card is optional and must be ordered separately.

Acquire the following components, if needed:

- Serial terminal or terminal emulation for console output.
- Cables for terminal and network connections.

- Rear transition cards and PMCs are optional. If a PMC is used, PIM and PMC hardware is needed.
- TOD battery is optional. If used, the battery must be type CR 1632, with a minimum of 4ma abnormal charging current rating (for example; a Panasonic CR 1632).

TABLE 1-3 lists ATCA and other minimum requirements met by the Netra CP3010 board.

TABLE 1-3 ATCA and Other Minimum Requirements Met By the Netra CP3010 Board

Requirements	Netra CP3010 as Node Board
ATCA system enclosure for 8U boards (includes chassis, backplane, power supply)	Yes
Console output device or serial terminal	Yes
Boot device (such as hard drive, network, or Compact Flash card)	Yes
Peripheral device for network access	Yes
Intelligent Platform Management Controller (IPMC)	Yes

1.5.2 Software Requirements

The Netra CP3010 board supports the following versions of the Solaris OS:

- Solaris 10 OS and subsequent compatible versions
- Solaris 9 9/05 OS and subsequent compatible versions with supported Netra patches

Refer to the *Netra CP3010 Board Product Notes* (819-1181) for more Solaris OS information, including a list of the required Netra software patches. You can view and download the latest version of this manual at the following web site:

`http://www.sun.com/documentation`

1.6 Technical Support and Warranty

Should you have any technical questions or support issues that are not addressed in the Netra CP3010 board documentation set or on the web site, contact your local Sun Services representative. This hardware carries a 1-year return-to-depot warranty. For

customers in the US or Canada, please call 1-800-USA-4SUN (1-800-872-4786). For customers in the rest of the world, find the World Wide Solution Center nearest you by visiting our web site:

http://www.sun.com/service/contacting/solution.html

When you call Sun Services, be sure to indicate that the Netra CP3010 board was purchased separately and is not associated with a system. Please have the board identification information ready. For proper identification of the board be prepared to give the representative the board part number, serial number, and date code (see FIGURE 1-6).

1.6.1 Board Part Number, Serial Number, and Revision Number Identification

The Netra CP3010 board part number, serial number, and version can be found on stickers located on the card (see FIGURE 1-6).

The Sun barcode label provides the following information:

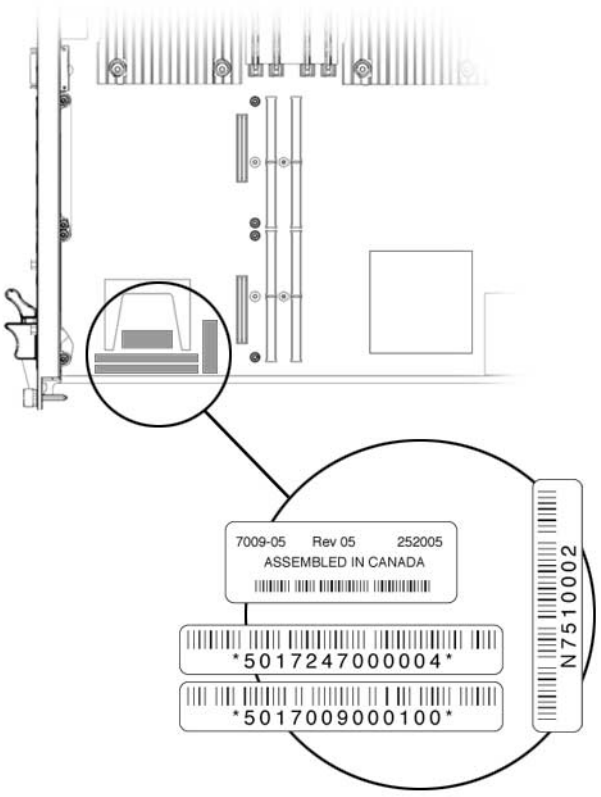
- Board part number (for example, 5017247), which is the first seven digits on the barcode label
- Board serial number (for example, 000004), which is the next six digits on the barcode label

The dash/revision/date code label provides the following information:

- Product dash number (for example, -05)
- Revision number (for example, REV: 05)
- Board date code (for example, 252005, which represents the twenty-fifth week of the year 2005)

The MAC address label contains the MAC address for the board in printed and barcode form. See Section 2.4.6, “Replacing the EEPROM” on page 2-16 for information on installation and removal of the MAC address label.

FIGURE 1-6 Netra CP3010 Board Barcode Labeling



Note – You might find the labels shown in FIGURE 1-6 on other locations on your board. Also, your particular board configuration might appear different from the preceding illustration.

CHAPTER 2

Hardware Installation

This chapter describes the hardware installation procedures for the Netra CP3010 board, and contains the following sections:

2.1 Equipment and Operator Safety

Refer to *Important Safety Information for Sun Hardware Systems* (816-7190) for general safety information.

Read the safety statements specific to the Netra CP3010 board carefully before you install or remove any part of the system.

Caution – Depending on the particular chassis design, operations with open equipment enclosures can expose the installer to hazardous voltages with a consequent danger of electric shock. Ensure that line power to the equipment is disconnected during operations that make high voltage conductors accessible.

The installer must be familiar with commonly accepted procedures for integrating electronic systems and with the general practice of Sun systems integration and administration. Although parts of these systems are designed for hot-swap

operation, other components must not be subjected to such stresses. Work with power connected to a chassis only when necessary, and follow these installation procedures to avoid equipment damage.

This equipment is sensitive to damage from electrostatic discharge (ESD) from clothing and other materials. Use the following antistatic measures during an installation:

- If possible, disconnect line power from the equipment chassis when servicing a system or installing a hardware upgrade. If the chassis cannot be placed upon a grounded antistatic mat, connect a grounding strap between the facility electrical input ground (usually connected to the equipment chassis) and facility electrical service ground.
- Use an antistatic wrist strap when:
  - Removing a board from its antistatic bag
  - Connecting or disconnecting boards or peripherals

  The other end of the strap lead should be connected to one of the following:
  - A ground mat
  - Grounded chassis metalwork
  - A facility electrical service ground
- Keep boards in the antistatic bags until they are needed.
- Place circuit boards that are out of their antistatic bags on an antistatic mat if one is available. The mat must be grounded to a facility electrical service ground. Do not place boards on top of an antistatic bag unless the outside of the bag also has antistatic protective properties.
- Remove a board from its antistatic bag only when wearing a properly connected ground strap.

2.2 Materials and Tools Required

This section provides information on the materials and tools required to perform installation. The minimum tools required to perform installation are:

- Phillips screwdrivers, No. 1, No. 2 (optional)
- Antistatic wrist strap
- Terminal console

Refer to Section 1.5.1, "Hardware Requirements" on page 1-12 for information on hardware requirements.

2.3 Preparing for the Installation

Read the following subsections before starting to install these boards. In addition, do the following:

1. Become familiar with the contents of the referenced documentation.
2. Verify that all listed hardware and software is available (see Section 1.5, "System Requirements" on page 1-12).
3. Check power, thermal, environmental, and space requirements (see Section 2.3.1, "Checking Power, Thermal, Environmental, and Space Requirements" on page 2-4).
4. Verify that local area networking (LAN) preparations are completed (see Section 2.3.2, "Determining Local Network IP Addresses and Host Names" on page 2-4).
5. Ensure that the host names and their network IP addresses are allocated and registered at the site.

2.3.1 Checking Power, Thermal, Environmental, and Space Requirements

Observe the following requirements:

- Your enclosure specifications support the sum of the specified maximum board power loads. See Section 5.5, "Power Requirements" on page 5-46 for board power specifications.
- Facility power loading specifications can support the rack or enclosure requirements.
- Your enclosure specifications support the cooling airflow requirements. The Netra CP3010 board fits a standard ATCA shelf or chassis. If your installation requirements are different, contact your field application engineer.

2.3.2 Determining Local Network IP Addresses and Host Names

Collect the following information to connect hosts to the local area network (LAN). Ask your network administrator for help, if necessary. This information is not needed for a standalone installation. You can use TABLE 2-1 to record this information.

TABLE 2-1 Your Local Network Information

Information Needed	Your Information
IP addresses* and host name for each Netra CP3010 client	
Domain name	
Type of name service and corresponding name server names and IP addresses—for example, DNS and NIS (or NIS+)	
Subnet mask	
Gateway router IP address	
NFS server names and IP addresses	
Web server URL	

* Local IP addresses are not needed if they are assigned by a network DHCP server.

You might need the MAC (Ethernet) addresses of the local hosts to make nameserver database entries. The MAC address can be seen in the console output while booting to the `ok` prompt. It can also be derived from the host ID seen on the barcode label of the I^2C EEPROM (see Section 1.6.1, "Board Part Number, Serial Number, and Revision Number Identification" on page 1-14).

2.3.3 Installation Procedure Summary

The steps in this section summarize the Netra CP3010 board installation at a high level. Be sure to read the details in Section 2.4, "Configuring the Board Hardware" on page 2-6 before installing the board.

The procedure to set up and configure a Netra CP3010 board in a system includes the following steps:

1. Configure the board's physical hardware. For example, install memory and PMC cards, replace the serial EEPROM, and set switches if necessary.
2. Configure the rear transition card with PIMs, switch settings, or connector attachments, as necessary.
3. Physically install the rear transition card (as necessary), host, and any peripheral boards into the chassis.
4. Connect the nodes to a local network. Alternatively, the board can be run as a standalone system without a network connection.
5. Install the operating system.

2.4 Configuring the Board Hardware

This section lists hardware installation and settings that might apply to your board configuration. Read and perform the procedures, as necessary, before installing the Netra CP3010 board into the chassis.

2.4.1 Installation of DDR-1 DIMM Memory Modules

The Netra CP3010 board supports a total of 4 DIMMs and a maximum memory capacity of 8 Gbytes (using four 2-Gbyte DIMMs). In addition to the on-board memory, the Netra CP3010 board accommodates the following:

- Four standard DDR-1 DIMMs, buffered, registered
- Two matching DIMMs per CPU
- Supports 1-Gbyte and 2-Gbyte DDR-1 modules
- All four DIMMs are installed

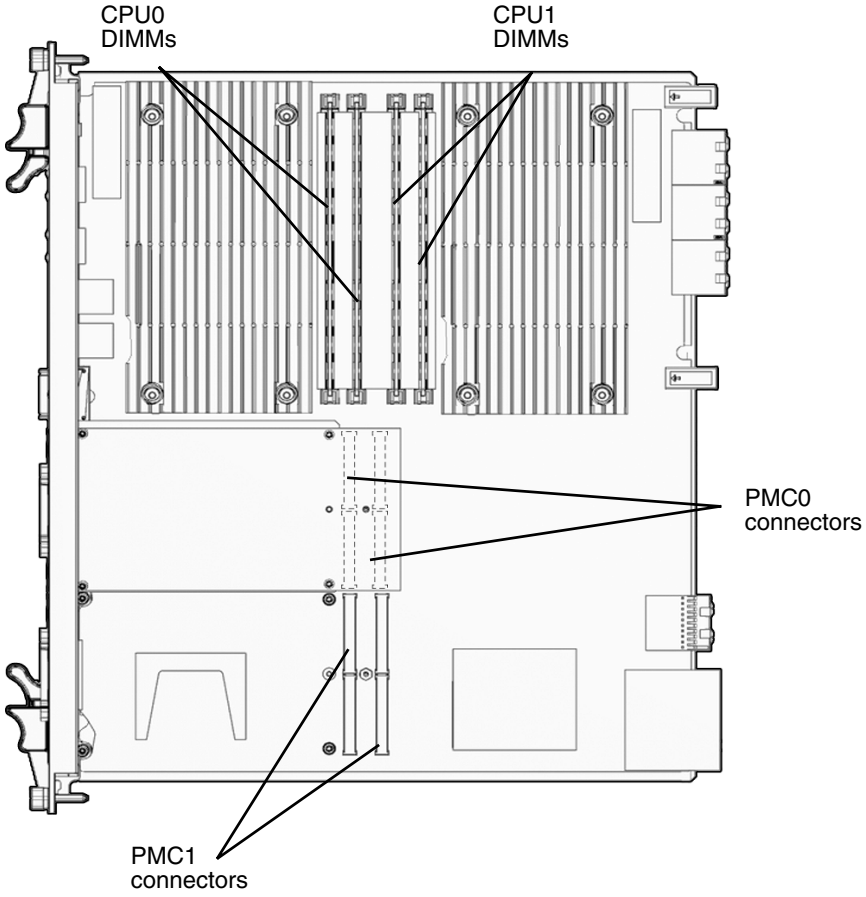
Two DIMMs must be installed for each CPU, and they must be matching pairs. You cannot mix 1-Gbyte and 2-Gbyte DIMMs for a CPU, but you can have two 1-Gbyte DIMMs for one CPU and two 2-Gbyte DIMMs for the other CPU.

The Netra CP3010 board supports DDR-1 DIMM memory modules that have the following characteristics:

- Each DIMM has a 72-bit wide data bus (64+8 ECC) and up to 14 address bits.
- The DIMMs run at 2.5 volts and take a 1.25 reference voltage (Vtt).
- Maximum height of the DIMM module is 0.72 inches, Very Low Profile (VLP).
- Four 184-pin JEDEC Standard DDR DIMM slots that support PC-2100 registered/buffered DIMMs.
- Maximum SDRAM clock frequency of 133 MHz.
- Supports single-bank or dual-bank SDRAM DIMMs.
- Supports 4-Rank DIMMs.
- Memory controller supports 128-bit data plus 9-bits error correcting code (ECC).
- Supports four internal SDRAM device banks.
- Maximum of 8 Gbytes:
  - Peak memory bandwidth of 4.2 Gbit/sec at 133 MHz
  - SSTL_2 inputs and output

For additional information, see Section 5.1.2, "DDR Memory Subsystem" on page 5-5. FIGURE 2-1 shows the location of the DIMMs and PMC connectors.

FIGURE 2-1 DDR-1 DIMM Memory and PMC Connector Locations



2.4.1.1 Installing a DDR-1 DIMM Memory Module

The following procedure provides a general guide for installing additional memory. However, for directions on the installation process of the memory DDR-1 DIMMs on the Netra CP3010 board, refer to the documentation that shipped with the memory module.

Caution – Do not remove the DDR-1 DIMM from its antistatic container until you are ready to install it on the card. Handle the module only by its edges. Do not touch module components or metal parts. Always wear a grounded antistatic wrist strap when handling modules.

1. **Locate the DDR-1 DIMM connectors on the Netra CP3010 board.**

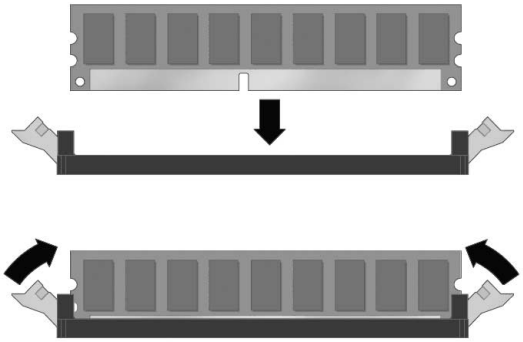
   Select the connectors where you will install the memory module (see FIGURE 2-1). If you need to replace an existing memory module with a new module, see Section 2.4.1.2, "Removing a DDR-1 DIMM Memory Module" on page 2-10 for instructions on removing the DDR-1 DIMM module.

2. **Remove the DDR-1 DIMM from its protective packaging, holding the module only by the edges.**

3. **Holding the DDR-1 DIMM at approximately a 20-degree angle to the board, insert the bottom edge of the DDR-1 DIMM into the bottom of the slot's hinge-style connector (see FIGURE 2-2).**

   The socket and module are both keyed, which means the module can be installed one way only. With even pressure, push simultaneously on both upper corners of the DDR-1 DIMM until its bottom edge (the edge with the gold fingers) is firmly seated in the connector.

FIGURE 2-2 Installing a DDR-1 DIMM Memory Module



Caution – Evenly engage the DDR-1 DIMM in its hinge-style slot at the 20-degree angle; uneven contact can cause shorts that damage the Netra CP3010 board. Do not rock the DDR-1 DIMM into place. Ensure that all contacts engage at the same time. You feel or hear a click when the DDR-1 DIMM properly seats in the connector.

4. **Press the top edge of the DDR-1 DIMM toward the board until the retainer clips click into place (see** FIGURE 2-2**).**

   The small metal retainer clips on each side of the DDR-1 DIMM slot are spring-loaded, and click into place in the notches on the sides of the DDR-1 DIMM.

5. **Install heat sinks on DIMMs if heat sinks are provided.**

2.4.1.2 Removing a DDR-1 DIMM Memory Module

You might need to remove a DDR-1 DIMM module from the Netra CP3010 board if you are returning the DDR-1 DIMM module or the board for service, or if you are replacing a module with another DDR-1 DIMM module. To remove a DDR-1 DIMM from the Netra CP3010 board, perform the following steps:

Note – Safely store the original factory-shipped DDR-1 DIMM and related DDR-1 DIMM packaging. You might wish to store any removed DDR-1 DIMM in the new DDR-1 DIMM packaging, or use the packaging for service.

---

1. **Take antistatic precautions: attach and electrically ground the wrist strap.**

Caution – Always wear a grounded antistatic wrist strap when handling modules.

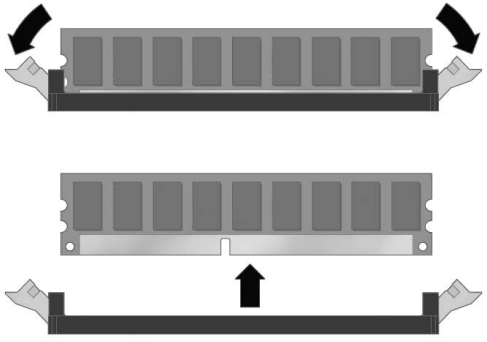
---

2. **Place the Netra CP3010 board on an antistatic mat, or on the board's antistatic bag if you do not have a mat available.**
3. **For the DDR-1 DIMM you wish to remove, simultaneously pull both DDR-1 DIMM spring retainer clips outward from the slot.**

   The DDR-1 DIMM releases outward at an angle of about 20 degrees (see FIGURE 2-3).
4. **Grasp the DDR-1 DIMM by the edges, and carefully pull it out of its connector. Place it in an antistatic bag.**

   Ensure that you pull the DDR-1 DIMM out at an angle of about 20 degrees, or you might damage the DDR-1 DIMM.

FIGURE 2-3 Removing a DDR-1 DIMM Memory Module



5. **If you are replacing the module you removed with a new DDR-1 DIMM, install it as described in** Section 2.4.1.1, “Installing a DDR-1 DIMM Memory Module” on page 2-7**.**

2.4.2 Installation of Optional TOD Battery

Because the Netra CP3010 board is shipped without a battery, the date and time stored in the TOD chip are not backed up when the system is powered off. The customer has the option of installing a TOD battery on the board.

The TOD battery **must** be type CR 1632, with a minimum of 4ma abnormal charging current rating (for example; a Panasonic CR 1632).

Caution – Risk of explosion if battery is replaced by an incorrect type. Dispose of batteries properly in accordance with manufacturer’s instructions and local regulations.

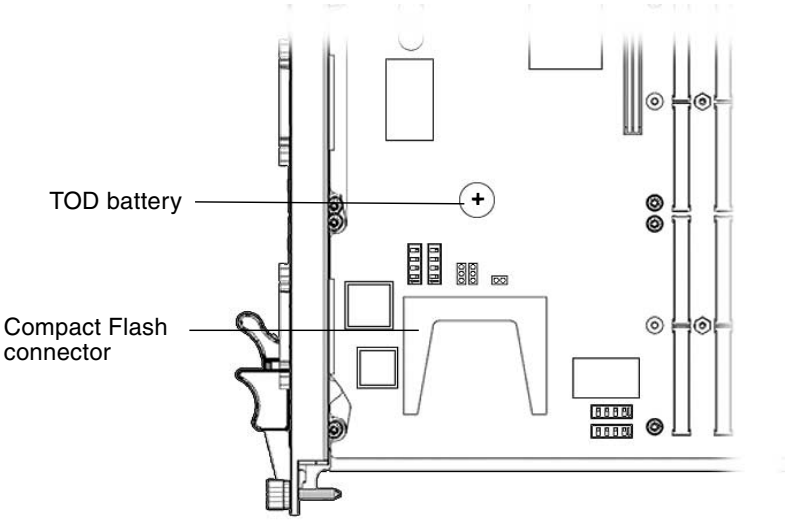
To install the battery, slide the battery into the holder (see FIGURE 2-4) with the side labeled "+" facing up.

2.4.3 Installation of Optional Compact Flash Card

An optional IDE Compact Flash card can be installed on the Netra CP3010 board. The Compact Flash card is not hot-swappable and there is no access to the card once the board is installed in an ATCA chassis.

To install the Compact Flash card, use the arrow on the card’s label as a guide and insert the card into the Compact Flash connector (see FIGURE 2-4).

FIGURE 2-4 TOD Battery and Compact Flash Card Locations



2.4.4 Installation of Optional PMC Devices

A PCI Mezzanine card (PMC) is a slim, modular card that provides additional functionality to the Netra CP3010 board. The board contains two PMC slots in which you can install optional PMC devices (see FIGURE 2-1 for the location of these slots). You must install PMC devices on the Netra CP3010 board before you install the board into the chassis.

To provide rear I/O access to the PMC device, the PMC device's kit might contain a PIM card that must be installed on the Netra CP30x0 rear transition card. Refer to the PIM card documentation and the *Netra CP30x0 Rear Transition Card User's Guide* (819-1187) for installation instructions.

2.4.4.1 Installing an Optional PMC Device

Note – The following procedure provides a general set of instructions for installing PMC devices on the Netra CP3010 board. Refer to the PMC card manufacturer's documentation for specific instructions on installing these devices.

---

1. Retrieve the wrist strap from the adapter's ship kit.

2. **Attach the adhesive copper strip of the antistatic wrist strap to the metal chassis. Wrap the other end twice around your wrist, with the adhesive side against your skin.**

3. **Remove the Netra CP3010 board from its antistatic envelope and place it on an ESD mat (if one is available) near the chassis.**

   If an ESD mat is not available, you can place the card on the antistatic envelope it was packaged in.

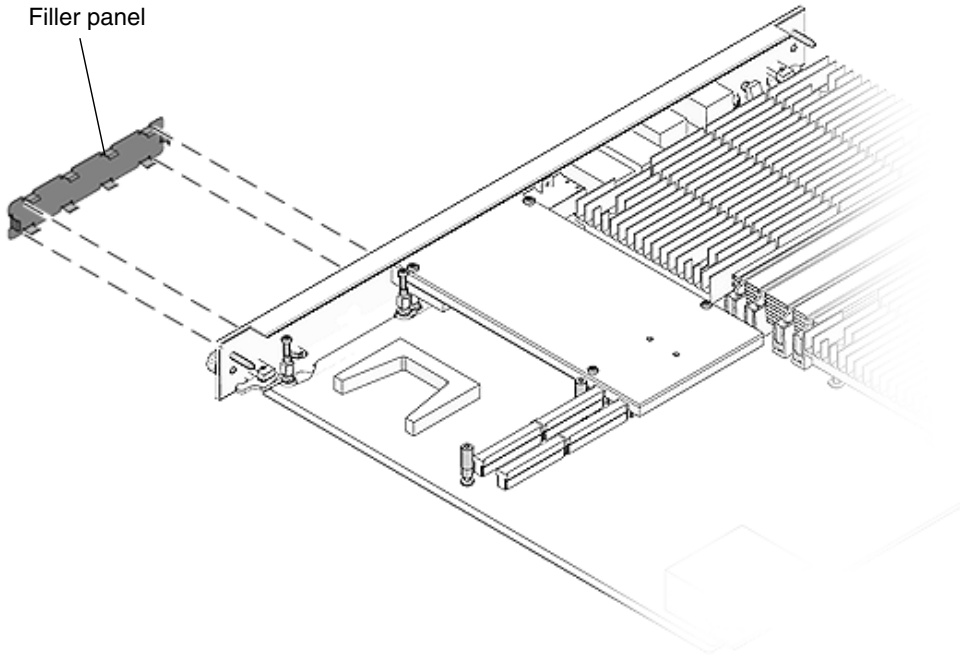
Note – If EMI compliance is required, do not remove the PMC filler panel unless you are going to install a PMC to the adapter.

---

4. **If the PMC has a connector for cabling, remove the Netra CP3010 board's filler panel (**FIGURE 2-5**).**

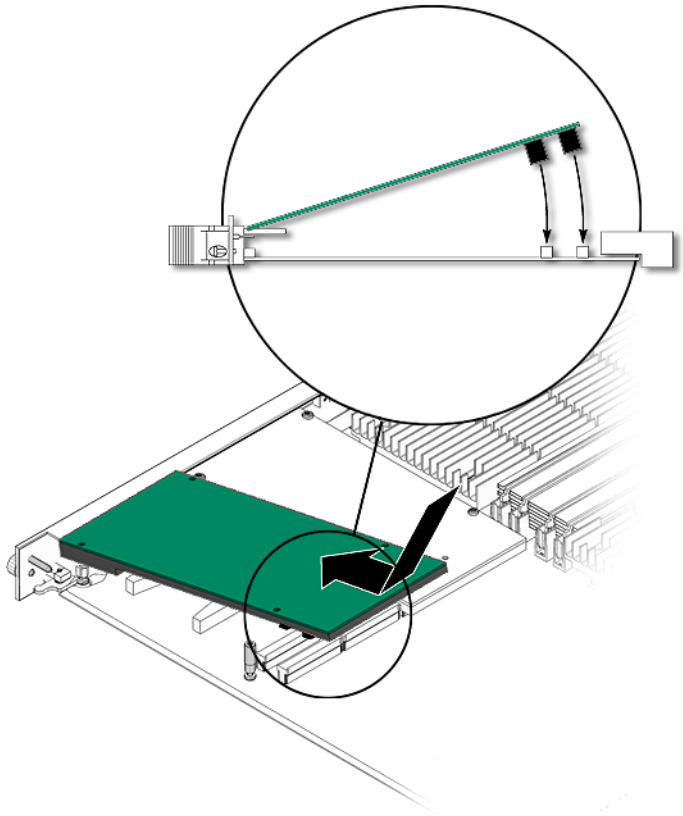
   Depending on its application, a PMC might contain a connector where you need to attach a PMC-specific cable, or it might have LEDs that must be viewed while operating. If the PMC has a connector or LEDs, remove the board's filler panel so that you can connect the appropriate cable after installing the board.

FIGURE 2-5 Removing the PMC Filler Panel



5. **Retrieve the PMC from its ship kit and place it on an antistatic surface.**
6. **Insert the PMC at an angle into the appropriate PMC slot (**FIGURE 2-6**).**
   Make sure that the PMC's connector goes through the board's PMC slot.

FIGURE 2-6 Inserting the PMC Into the PMC Slot



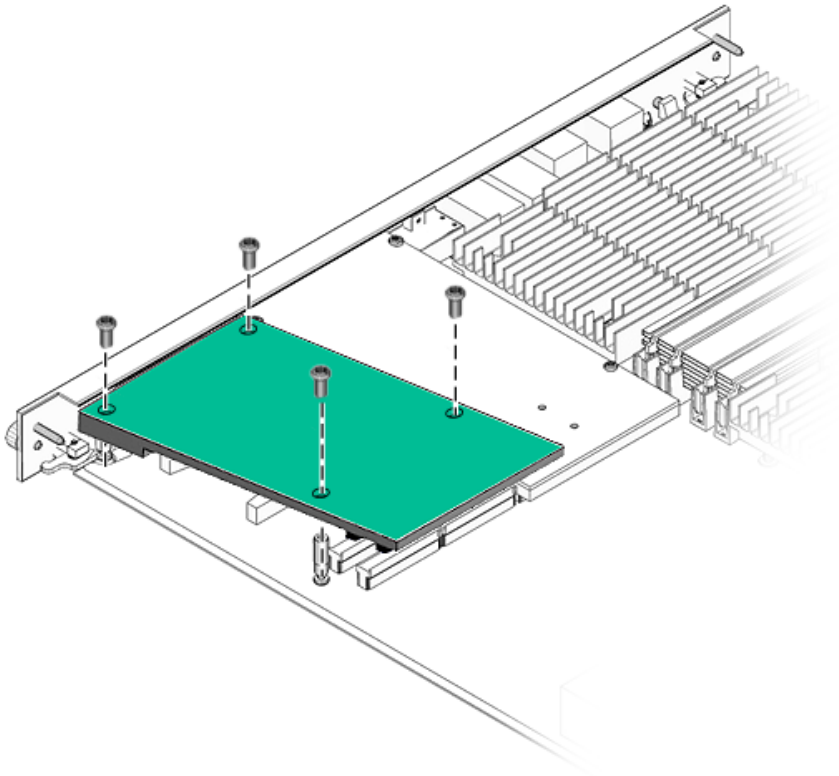
7. **Align the PMC over the PMC connectors.**

8. **Carefully press the PMC into the board's PMC connectors (**FIGURE 2-6**).**

Caution – Do not use excessive force when installing the PMC into the slot. You might damage the PMC's connectors or the connectors on the Netra CP3010 board, causing permanent damage to the PMC or the board. If the PMC does not seat properly when you apply even pressure, remove the PMC and carefully reinstall it.

9. **Use a screwdriver to secure the four screws that attach the PMC to the Netra CP3010 board (**FIGURE 2-7**).**

FIGURE 2-7 Securing the PMC Screws



Refer to the PMC device's documentation for PMC software and cabling installation instructions.

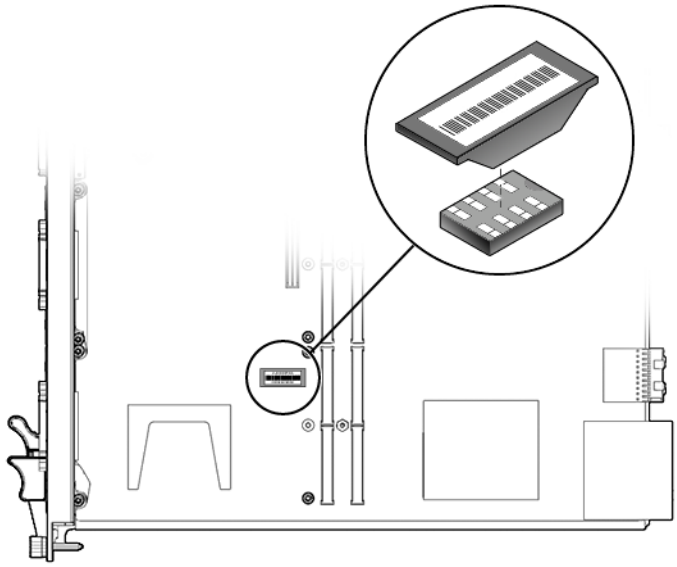
2.4.5 Setting Switches

Normally you do not need to set or reset the switches or jumpers. See Section A.5, "Switches and Jumpers" on page A-4 for details about the Netra CP3010 board switch settings.

2.4.6 Replacing the EEPROM

The I^{2}C serial EEPROM stores the board's MAC address and host ID information. You do not need to replace the EEPROM unless you are installing a replacement board that does not have the host ID information.

FIGURE 2-8 Replacing the I^{2}C EEPROM



If you need to replace the Netra CP3010 board, remove the I^{2}C EEPROM from the original board and install it on the replacement Netra CP3010 board. FIGURE 2-8 shows the position of the I^{2}C EEPROM on the Netra CP3010 board. The MAC address label is positioned on top of the I^{2}C EEPROM.

2.4.7 Configuring Rear Transition Card Hardware

If you are using the Netra CP30x0 rear transition card, refer to the *Netra CP30x0 Rear Transition Card User's Guide* (819-1187). You can also refer to the Netra CP30x0 manual for detailed connector pin assignments.

2.4.7.1 Installing PIM Assemblies

Follow the PMC card manufacturer's procedure to install PIM cards. Refer to the *Netra CP30x0 Rear Transition Card User's Guide* (819-1187) for more PIM connector pin assignments and additional installation information.

Caution – When installing a PIM card onto the rear transition card, ensure that the PIM card power signals match the corresponding power signals of the PIM connectors that are to be installed on the Netra CP30x0 rear transition card.

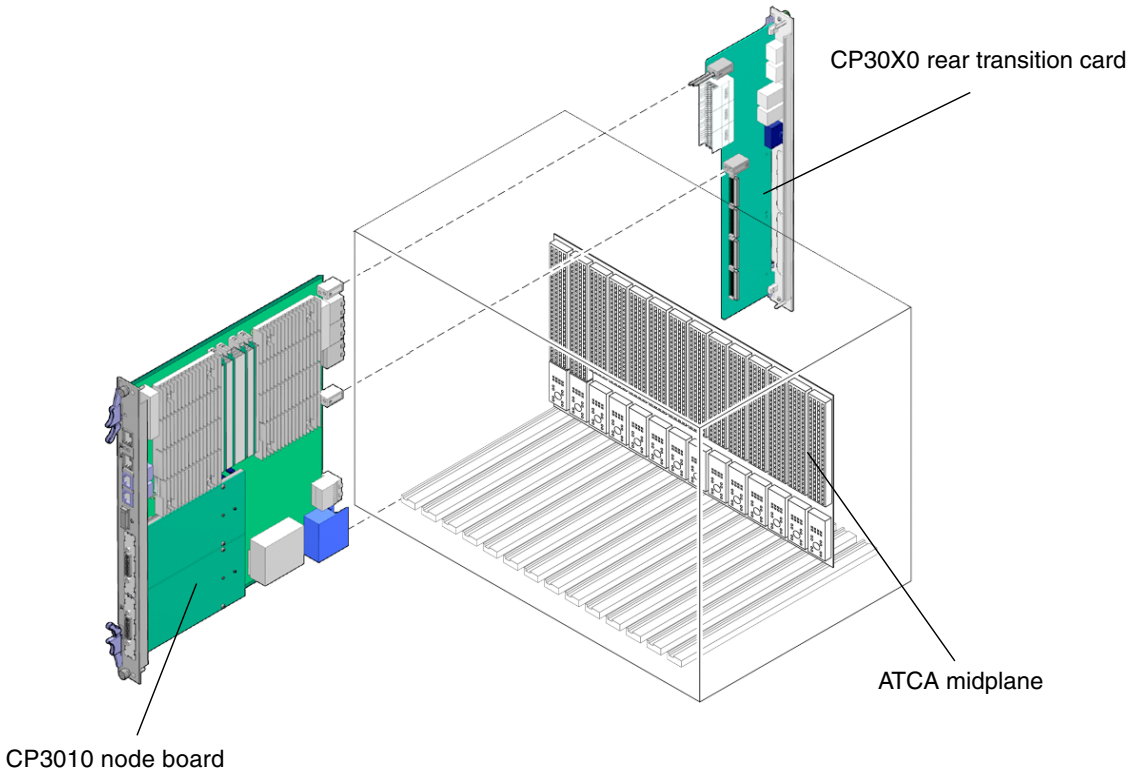
2.5 Installing the Netra CP3010 Board

If you are installing the Netra CP3010 board with the rear transition card, first install the rear transition card at the rear of the server. Then install the front card in the front of the server. Even though you will be installing the rear transition card first, look at the front of the server and locate the slot number where you will be installing the cards. Then go to the back of the server and install the rear transition card in that particular slot.

2.5.1 Installing the Netra CP3010 Board With a Rear Transition Card

A compatible rear transition card must be used with the Netra CP3010 board for rear I/O access. The card enables access to the network, to a boot device, and to a console terminal. You can use the Netra CP30x0 rear transition card, or you might design your own transition card.

FIGURE 2-9 Installing the Netra CP30x0 Rear Transition Card



2.5.1.1 Installing a Rear Transition Card

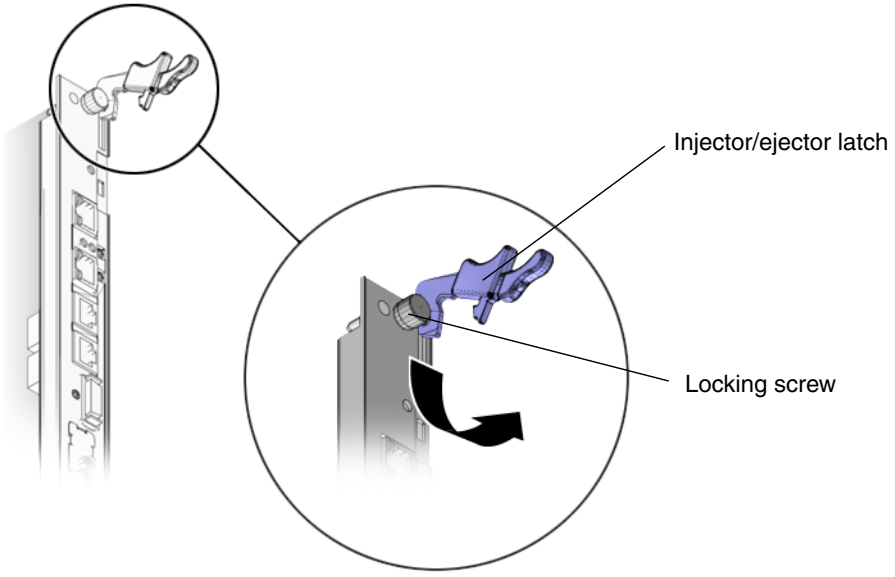
1. **Verify that you have taken the necessary antistatic precautions.**
2. **Go to the rear of the system and choose an appropriate slot for the rear transition card.**

   Rear transition cards must be installed inline behind the accompanying front board. For example, if the accompanying front board is installed in slot 3, its rear transition card must be installed at the back of the system in slot 3. See FIGURE 2-9.
3. **Remove the slot filler panel from the selected node board slot, if necessary.**
4. **Get the rear transition card from the ship kit.**
5. **Perform any card-specific hardware procedures, if necessary.**

   Refer to the documentation that you received with the card for more information.

6. **Prepare the card by opening the injector/ejector latches at the top and bottom of the card (**FIGURE 2-10**).**

FIGURE 2-10 Injector/Ejector Latch and Locking Screw



7. **Connect any internal system cabling, such as cabling to an IDE device, to the appropriate headers on the rear transition card.**

   Route the cabling so that it does not snag or kink when the card is inserted.

8. **Carefully align the edges of the card with the card guides in the appropriate slot.**

   It might be helpful to look into the enclosure to verify correct alignment of the rails in the guides.

9. **Taking care to keep the board aligned in the guides, slide the card in until the injector/ejector latches engage the card cage.**

10. **Push the board into the midplane connectors and close the latches to seat the board in the connectors.**

11. **Tighten the locking screws to ensure that the board is secured into the shelf.**

12. **Install the Netra CP3010 board into the shelf.**

    Go to "Installing the Netra CP3010 Board" on page 20 for those instructions.

2.5.2 Installing the Netra CP3010 Board

1. **If you have installed a rear transition card, go to the front of the system and locate the card slot where you installed the rear transition card at the rear of the system.**

2. **Remove the filler panel, if necessary.**

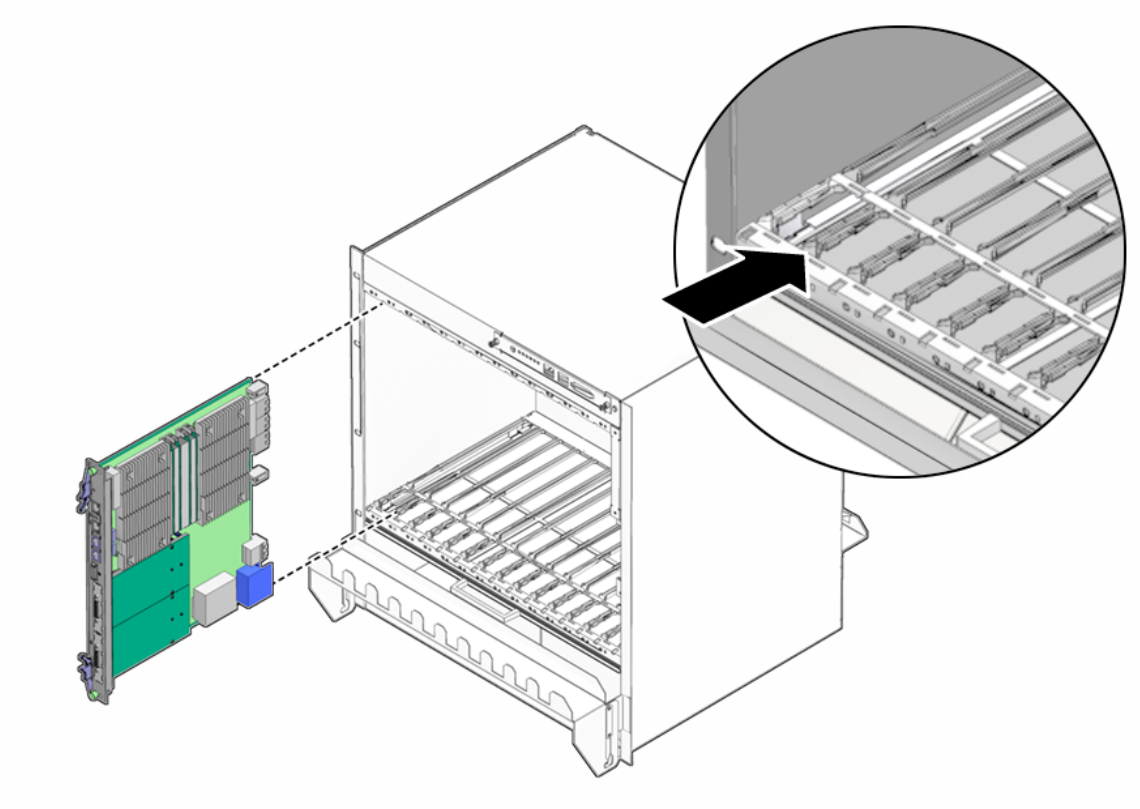
   The filler panel is secured to the card cage using two screws, one at the top of the filler panel, the other at the bottom. Store the filler panel in a safe place; you might need to use it again if you have to remove a card for an extended period of time.

3. **Prepare the board by opening the injector/ejector latches (**FIGURE 2-10**).**

4. **Carefully align the edges of the board with the card guides in the appropriate slot (**FIGURE 2-11**).**

   It might be helpful to look into the enclosure to verify correct alignment of the rails in the guides.

FIGURE 2-11 Installing Node Board Into Chassis Slot



5. **Taking care to keep the board aligned in the guides, slide the board in until the injector/ejector latches engage the card cage.**

6. **Push the board slightly into the midplane connectors, and then close the latches to seat the board in the connectors.**

   When the lower latch is closed, the blue Hot-Swap LED blinks while the board is initializing. The blue LED turns off and the green OK LED lights when the board is ready.

7. **Tighten the locking screws to ensure the board is secured into the shelf (see** FIGURE 2-10**).**

2.6 Connecting External I/O Cables

External I/O cables are connected to the Netra CP3010 board or to the Netra CP30x0 rear transition card when a rear transition card is used. Information on connecting each of these cables follows:

- For Ethernet connections, category 5e or better network cable is required. One end of the Ethernet cable is connected to a suitable 10/100BASE-T switch and the other end to one of the Ethernet ports on the Netra CP3010 board or Netra CP30x0 rear transition card. Both Ethernet port A and Ethernet port B are available (see Section 4.2.1.1, "Network Device Aliases" on page 4-6 for bge device names). By default, when a Netra CP30x0 rear transition card is installed, the Ethernet cables are connected only to the Ethernet ports on the rear transition card. Refer to the *Netra CP30x0 Rear Transition Card User's Guide* (819-1187) for more information.
- Asynchronous serial I/O cables are attached from serial communication devices to the RJ-45 serial ports on the CP3010 board or CP30X0 transition card. Both serial ports can be used on either the CP3010 board or CP30X0 transition card, but the same port should not be used on both. If serial port A is used on the CP3010 board, serial port A on the CP30X0 rear transition card should not be used.

  Once a serial cable is connected, use the `tip` utility on the host to establish a full-duplex terminal connection with the Netra CP3010 board. At the UNIX prompt in a command tool or shell tool, type:

```
# tip -9600 /dev/ttya  (for Serial Port A)
or
# tip -9600 /dev/ttyb  (for Serial Port B)
```

- The SAS port on the CP3010 board or CP30X0 rear transition card requires an external 4X SAS cable. The other end of the 4X SAS cable is typically connected to a storage device. Separate external 4X SAS cables can be attached to the CP3010 SAS port and the CP30X0 SAS port at the same time.
- For optional PMC I/O cables, such as a printer cable, connect the cables according to the manufacturer's specifications.

CHAPTER 3

Software Configuration

This chapter contains the following sections:

3.1 Operating Systems

The Netra CP3010 board supports the Solaris 10 OS and subsequent compatible versions, and the Solaris 9 9/05 OS and subsequent compatible versions, with supported Netra patches. The Solaris OS software can be downloaded from the Sun download center at:

http://www.sun.com/download

Note – Refer to the *Netra CP3010 Board Product Notes (*819-1181) for information on the Netra patches at http://www.sun.com/documentation.

For information on these versions of the Solaris OS, including installation, see the appropriate Solaris Documentation Collection at the Sun Documentation web site at:

http://www.sun.com/documentation

3.2 Installing Diskless Clients

The following procedures describes how to create a boot server for diskless clients and how to add new diskless clients to the patched boot server. For additional instructions on installing diskless clients, refer to the appropriate Solaris Documentation Collection at the Sun Documentation web site at:

http://www.sun.com/documentation

You must have a root (i.e.; superuser) password on your diskless server to perform the following tasks.

3.2.1 Creating a Boot Server for Diskless Clients

Note – This procedure sets up a boot server by starting the operating environment services required for diskless clients. Once you have set up the boot server, see Section 3.2.2, "Adding a Diskless Client" on page 3-4 for instructions on adding diskless clients to the boot server.

---

1. **Verify that the IP addresses for all other network interfaces on the boot server have corresponding hostnames in the hosts database.**

2. **Log into the network server as superuser and change directories to the** `/usr/sadm/bin` **directory.**

```
# cd /usr/sadm/bin
```

3. **Use the `smosservice` command to add boot services to the installation server.**

Note – The following command is a single long entry. Do not press the Return key until you have typed the entire text string shown in the following command.

```
# ./smosservice add -u root -p root_password -- -x mediapath=image_directory
-x platform=sparc.sun4u.Solaris_n -x cluster=SUNWCXall -x locale=locale
```

Where:

- *root_password* is the root password for the installation server
- *image_directory* is the path to the directory where the Solaris install image is stored
- *N* is the Solaris OS version you are using, either `10` or `9`.
- *locale* is the locale that you want to use

Refer to the `smosservice`(1M) man page for more information and options.

For example, if the following entries were used for each variable, the command would appear as follows.

- *root_password* = `root_password`
- *image_directory* = `/export/install`
- *locale* = `en_US`
- *n* = `10` (for Solaris 10)

```
# ./smosservice add -u root -p root_password -- -x mediapath=/export/ins
-x platform=sparc.sun4u.Solaris_10 -x cluster=SUNWCXall -x locale=en_US
```

4. **Download and install additional patches.**

   Refer to the *Netra CP3010 Board Product Notes* (819-1181) for the latest information on the patches available for the Netra CP3010 board. The document can be downloaded from the following web site:

   `http://www.sun.com/documentation`

   Follow the instructions in the *Netra CP3010 Board Product Notes* (819-1181) for downloading and applying patches to a diskless clients boot server.

5. **After the patches are installed, follow the procedure in** Section 3.2.2, "Adding a Diskless Client" on page 3-4**.**

3.2.2 Adding a Diskless Client

1. **Prepare a patched boot server for the diskless clients.**

   Follow the steps in Section 3.2.1, "Creating a Boot Server for Diskless Clients" on page 3-2 to create a boot server for the diskless clients.

2. **Log into the patched boot server as superuser.**

3. **Collect the following information for the diskless client you are adding:**

- the client's IP address
- the client's ethernet address
- the client's host name

4. **Change directories to the `/usr/sadm/bin` directory.**

```
# cd /usr/sadm/bin
```

5. **Set up the diskless clients.**

   For each diskless client, type the following command as superuser (root):

```
# ./smdiskless add -- -i ip_address -e ethernet_address -n host_name\
-x os=sparc.sun4u.Solaris_n -x root=/export/root/host_name \
-x swap=/export/swap/host_name -x swapsize=swap_size -x tz=time_zone \
-x locale=locale -x ns=name_service -x nameserver=name_server
```

Where:

- *ip_address* is the client's IP address
- *ethernet_address* is the client's Ethernet address
- *host_name* is the client's host name
- *n* is the Solaris OS version you are using, either `10` or `9`.
- *swap_size* is the size of the swap space that you will be using. The default is `24`, however your swap space should be the same amount as your memory
- *time_zone* is the client's time zone
- *locale* is the client's locale
- *name_service* is the client's nameservice
- *name_server* is the nameserver's hostname

Refer to the `smdiskless(1m)` man page for more information and options.

For example, if the following entries were used for each variable, the command would appear as follows.

- *ip_address* = `129.144.214.999`

- *ethernet_address* = `8:0:20:22:b3:aa`
- *host_name* = `client_host`
- *n* = `10` (for Solaris 10)
- *swap_size* = `128`
- *time_zone* = `US/Pacific`
- *locale* = `en_US`
- *name_service* = `NIS`
- *name_server* = `nameserver_host`

```
# ./smdiskless add -- -i 129.144.214.999 -e 8:0:20:22:b3:aa -n client_hos
os=sparc.sun4u.Solaris_10 -x root=/export/root/client_host -x swap=
/export/swap/client_host -x swapsize=999 -x tz=US/Pacific -x locale=en_U
ns=NIS -x nameserver=nameserver_host
```

You have to type your superuser password again after typing this command. The installation process should take roughly 5 minutes per client and about 15-30 minutes for the operating environment service to install; however, no progress is displayed on screen while the process is running. Do not cancel or kill the process until the process has successfully completed.

You should see messages similar to the following after a few moments, confirming that the command went through successfully the second time:

```
Login to client_host as user root was successful.
Download of com.sun.admin.osservermgr.cli.OsServerMgrCli from client_host
successful.
```

6. Boot the diskless client.

3.3 Hot Swap Information

The Netra CP3010 board supports hot-swapping and includes a blue Hot-Swap LED.

3.3.1 Hot-Swapping the Netra CP3010 Board

If the Solaris OS is running on a Netra CP3010 board and you open the board's latches, you see a message that the operating system will shut down in one minute. When the operating environment drops to the OpenBoot PROM prompt level, you can safely remove the board.

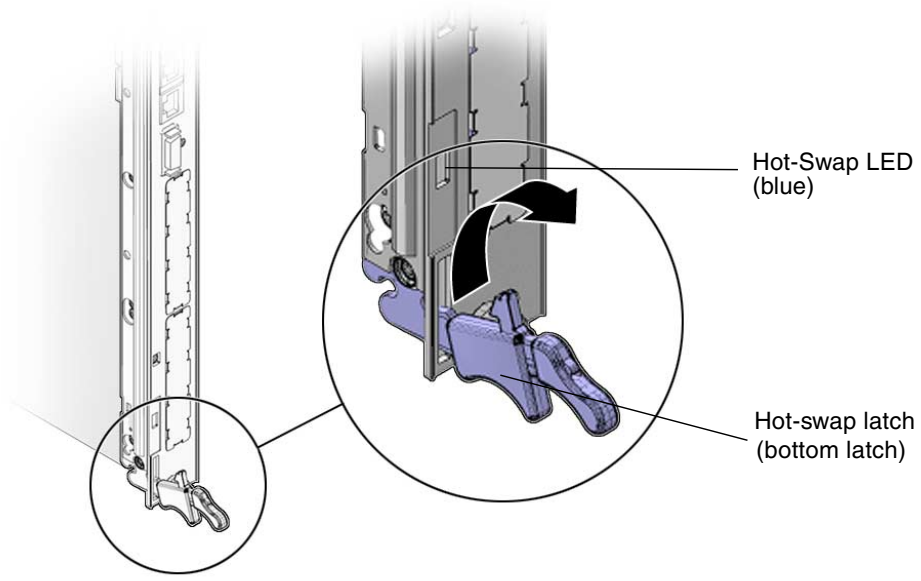
3.3.1.1 Hot-Swap LED

The blue Hot-Swap LED, located on the front panel of the Netra CP3010 board (FIGURE 1-1), blinks when a hot-swap is initiated, and lights steady when the board is ready to be removed from the system.

Unlatching the bottom latch on the Netra CP3010 board initiates the hot-swap sequence. The LED lights steady when the board can be safely removed from the system. The reverse is true when a Netra CP3010 board is installed into the system. Once the Netra CP3010 board is installed into the system and the bottom latch is latched, the blue hot-swap LED blinks until the board is ready and then turns off. The green LED lights steady when the board is ready.

FIGURE 3-1 shows the hot-swap latch and Hot-Swap LED.

FIGURE 3-1 Hot-Swap Latch and Hot-Swap LED



3.4 Retrieving Device Information

You use the Solaris platform information and control library (PICL) framework for obtaining the state and condition of the Netra CP3010 board.

The PICL framework provides information about the system configuration that it maintains in the PICL tree. Within this PICL tree is a subtree named *frutree*, which represents the hierarchy of system FRUs with respect to a root node in the tree called *chassis*. The frutree represents physical resources of the system. The PICL tree is updated whenever a change occurs in a device's status.

The `prtpicl -v` command shows the condition of all devices in the PICL tree. Sample output from the `prtpicl` command related to the Netra CP3010 board is shown in FIGURE 3-2.

FIGURE 3-2 Sample Output of the `prtpicl -v` Command

```
# prtpicl -v
...
frutree (picl, 4d00000001)
     platform (jbus, 4d00000005)
 scsi_vhci (devctl, 4d00000022)
 memory (memory, 4d000000e9)
             memory-segment (memory-segment, 4d00000420)
 memory-bank (memory-bank, 4d00000426)
 memory-bank (memory-bank, 4d0000042e)
 SUNW,UltraSPARC-IIIi (cpu, 4d000000fb)
 memory-controller (memory-controller, 4d00000117)
             memory-module-group (memory-module-group, 4d00000410)
 memory-module (memory-module, 4d00000415)
 memory-module (memory-module, 4d0000041a)
 pci (pci, 4d00000128)
             scsi (scsi-2, 4d00000148)
 i2c (i2c, 4d00000167)
             nvram (nvram, 4d00000173)
             idprom (idprom, 4d0000017d)
 pci (pci, 4d00000185)
             isa (isa, 4d000001a5)
 flashprom (flashprom, 4d000001bf)
 rtc (obp-device, 4d000001d5)
 serial (serial, 4d000001df)
 serial (serial, 4d000001f1)
 ipmc (ipmc, 4d00000201)
                      i2c (i2c, 4d00000217)
 dimm-spd (seeprom, 4d00000224)
 dimm-spd (seeprom, 4d0000022d)
 motherboard-fru-prom (seeprom, 4d00000236)
             pmu (pmu, 4d00000240)
 gpio (obp-device, 4d0000025b)
             ide (ide, 4d00000265)
             network (network, 4d00000282)
             network (network, 4d000002a6)
             ide (ide, 4d000002ca)
 dad (block, 4d000002ee)
 pci (pci, 4d00000305)
             network (network, 4d00000325)
             network (network, 4d0000034c)
 pci (pci, 4d00000370)
             ethernet (obp-device, 4d00000390)
```

TABLE 3-1 shows the frutree entries and properties that describe the condition of the Netra CP3010 board.

TABLE 3-1 PICL Frutree Entries and Description for the Netra CP3010 Board

Frutree Entry:Property	Entry Description	Example of Condition
CPU (location) :`State`	The state of the receptacle, or slot	`connected`
CPU (fru) :`Condition`	The condition of the board, or occupant	`ok`
CPU (fru) :`State`	The state of the board, or occupant	`configured`
CPU (fru) :`FRUType`	The FRU type	`bridge/fhs`

For more information on the PICL framework, refer to the `picld`(1M) man page.

3.5 Downloading and Installing SunVTS Software

SunVTS™ software is a comprehensive suite that tests and validates the Netra CP3010 board by verifying the configuration and function of most hardware controllers and devices on the board. SunVTS software is used to validate a system during development, production, inspection, troubleshooting, periodic maintenance, and system or subsystem stressing. SunVTS software can be tailored to run on machines ranging from desktops to servers with modifiable test instances and processor affinity features.

You can perform high-level system testing by using the appropriate version of SunVTS software. For detailed information on SunVTS support and downloads, refer to the following web site:

`http://www.sun.com/oem/products/vts/`

Ensure that the SunVTS software version is compatible with the Solaris OS version being used. Information on the version of the SunVTS software installed can be found in the file:

`/opt/SUNWvts/bin/.version`

To obtain SunVTS documentation, contact your local customer service representative or field application engineer.

Note – For security reasons, only a superuser is permitted to run SunVTS software. Installation and starting instructions are included with the software when it is downloaded.

CHAPTER 4

Firmware

The Netra CP3010 board contains a modular firmware architecture that gives you latitude in controlling boot initialization. You can customize the initialization, test the firmware, and even enable the installation of a custom operating system.

This platform also employs the Intelligent Platform Management controller (IPMC)—described in Section 5.1.5, "Intelligent Platform Management Controller (IPMC)" on page 5-22—which controls the system management, hot-swap control, and some board hardware. The IPMC configuration is controlled by separate firmware.

This chapter contains the following sections:

4.1 Power-On Self-Test Diagnostics

Power-on self-test (POST) is a firmware program that helps determine whether a portion of the system has failed. POST verifies the core functionality of the system, including the CPU modules, motherboard, memory, and some on-board I/O devices. The software then generates messages that can be useful in determining the nature of a hardware failure. You can run POST even if the system is unable to boot.

POST detects most system faults and is located in the motherboard's OpenBoot PROM. You can program the OpenBoot software to run POST at power-on by setting two environment variables: the `diag-switch?` and the `diag-level` flag. These two variables are stored on the system configuration card.

POST runs automatically when the system power is applied, or following an automatic system reset, if all of the following conditions apply:

- `diag-switch?` is set to `true` (default is `false`).
- `diag-level` is set to `min`, `max`, or `menus` (default is `min`).
- `diag-trigger` matches the class of reset (default is `power-on-reset`).

If `diag-level` is set to `min` or `max`, POST performs an abbreviated or extended test, respectively.

If `diag-level` is set to `menus`, a menu of all the tests executed at power-on is displayed.

POST diagnostic and error message reports are displayed on a console.

4.1.1 Controlling POST Diagnostics

You control POST diagnostics (and other aspects of the boot process) by setting OpenBoot configuration variables. Changes to OpenBoot configuration variables take effect only after the system is restarted.

TABLE 4-1 lists the most important and useful of these variables. You can find instructions for changing OpenBoot configuration variables in Section 4.5.1, "Viewing and Setting OpenBoot Configuration Variables" on page 4-10.

Refer to the *OpenBoot PROM Enhancements for Diagnostic Operation* (817-6957) document for more information.

TABLE 4-1 OpenBoot Configuration Variables

OpenBoot Configuration Variable	Description and Keywords
auto-boot	Determines whether the system automatically boots. Default is true. • true – System automatically boots after initialization, provided no firmware (diagnostics or OpenBoot) errors are detected. • false – System remains at the ok prompt until you type boot.
diag-level	Specifies the level or type of diagnostics that are executed. Default is max. • off – No testing. • min – Basic tests are run. • max – More extensive tests might be run, depending on the device. Memory extensively checked.
diag-script	Determines which devices are tested by OpenBoot Diagnostics. Default is norm • none – OpenBoot Diagnostics do not run. • normal – Tests all devices that are expected to be present in the system's bas configuration for which self-tests exist. • all – Tests all devices that have self-tests.
diag-switch?	Controls diagnostic execution in normal mode. Default is false. • true – Diagnostics are *only* executed on power-on reset events, but the level coverage, verbosity, and output is determined by user-defined settings. • false – Diagnostics are executed upon next system reset, but only for those reset events specified by the OpenBoot configuration variable. diag-trigger. The level of test coverage, verbosity, and output is determin user-defined settings.
diag-trigger	Specifies the class of reset event that causes diagnostics to run automatically. D setting is power-on-reset error-reset. • none – Diagnostic tests are not executed. • error-reset – Reset that is caused by certain hardware error events such a State Exception Reset, Watchdog Resets, Software-Instruction Reset, or Hardw Fatal Reset. • power-on-reset – Reset that is caused by power cycling the system. • user-reset – Reset that is initiated by an operating system panic or by user-initiated commands from OpenBoot (reset-all or boot) or from Sola (reboot, shutdown, or init). • all-resets – Any kind of system reset. **Note:** Both POST and OpenBoot Diagnostics run at the specified reset event if t variable diag-script is set to normal or all. If diag-script is set to none POST runs.
input-device	Selects where console input is taken from. Default is ttya. • ttya – From built-in SERIAL MGT port. • ttyb – From built-in general purpose serial port (10101).

TABLE 4-1 OpenBoot Configuration Variables *(Continued)*

OpenBoot Configuration Variable	Description and Keywords
`output-device`	Selects where diagnostic and other console output is displayed. Default is `ttya`. • `ttya`—To built-in SERIAL MGT port. • `ttyb`—To built-in general purpose serial port (10101).

Note – These variables affect OpenBoot diagnostics tests as well as POST diagnostics.

Once POST diagnostics have finished running, POST reports the status of each test to the OpenBoot firmware. Control then reverts back to the OpenBoot firmware code.

If POST diagnostics do not uncover a fault, and your server still does not start up, run OpenBoot diagnostics tests.

4.1.2 Starting POST Diagnostics

1. **Go to the `ok` prompt.**

2. **Type:**

```
ok setenv diag-switch? true
```

3. **Type:**

```
ok setenv diag-level value
```

   Where *value* is `min`, `max`, or `menus`, depending on the quantity of diagnostic information you want to see.

4. **Type:**

```
ok reset-all
```

   The system runs POST diagnostics if `post-trigger` is set to `user-reset`. Status and error messages are displayed in the console window. If POST detects an error, it displays an error message describing the failure.

5. **When you have finished running POST, restore the value of** `diag-switch?` **to** `false` **by typing:**

```
ok setenv diag-switch? false
```

Resetting `diag-switch?` to `false` minimizes boot time.

4.2 OpenBoot PROM Commands

OpenBoot PROM commands are commands you type at the `ok` prompt. OpenBoot PROM commands that can provide useful diagnostic information include:

- `probe-scsi` and `probe-scsi-all`
- `probe-ide`
- `show-devs`

4.2.1 Running OpenBoot PROM Commands

1. **Halt the system to reach the** `ok` **prompt.**

   Inform users before you shut down the system.

2. **Type the appropriate command at the console prompt.**

Refer to the *OpenBoot 4.x Command Reference Manual* (816-1177) for more commands.

4.2.1.1 Network Device Aliases

The Solaris OS provides some predefined device aliases for the network devices so that you do not need to type the full device path name. TABLE 4-2 lists the network device aliases, the default Solaris OS device names, and associated ports for the Netra CP3010 board. The `devalias` command can be used to display the device aliases.

TABLE 4-2 Network Device Aliases

	Default Solaris Device Name		
Device Alias	**Solaris 10**	**Solaris 9**	**BDM5704 Port**
net, net0	bge0	bge0	Base Fabric Ethernet 0
net1	bge1	bge1	Base Fabric Ethernet 1
net2	bge4	bge2	Management Ethernet 0 (Ethernet port A on front panel)
net3	bge5	bge3	Management Ethernet 1 (Ethernet port B on front panel)
net4	bge2	bge4	Extended Fabric Ethernet 0 (PICMG 3.1)
net5	bge3	bge5	Extended Fabric Ethernet 1 (PICMG 3.1)

4.2.2 `probe-scsi` and `probe-scsi-all` Commands

The `probe-scsi` and `probe-scsi-all` commands diagnose problems with the SCSI devices.

Caution – If you used the `halt` command or the Stop-A key sequence to reach the `ok` prompt, issuing the `probe-scsi` or `probe-scsi-all` command can hang the system.

The `probe-scsi` command communicates with all SCSI devices connected to on-board SCSI controllers. The `probe-scsi-all` command also accesses devices connected to any host adapters installed in PCI slots.

For any SCSI device that is connected and active, the `probe-scsi` and `probe-scsi-all` commands display its loop ID, host adapter, logical unit number, unique worldwide name (WWN), and a device description that includes type and manufacturer.

The following sample output is from the `probe-scsi` command.

CODE EXAMPLE 4-1 `probe-scsi` Command Output

```
{1} ok probe-scsi
Target 0
  Unit 0   Disk     SEAGATE ST373307LSUN72G 0207
Target 1
  Unit 0   Disk     SEAGATE ST336607LSUN36G 0207
{1} ok
```

The following sample output is from the `probe-scsi-all` command.

CODE EXAMPLE 4-2 `probe-scsi-all` Command Output

```
{1} ok probe-scsi-all
/pci@1c,600000/scsi@2,1

/pci@1c,600000/scsi@2
Target 0
  Unit 0   Disk     SEAGATE ST373307LSUN72G 0207
Target 1
  Unit 0   Disk     SEAGATE ST336607LSUN36G 0207

{1} ok
```

4.2.3 `probe-ide` Command

The `probe-ide` command communicates with all Integrated Drive Electronics (IDE) devices connected to the IDE bus. This is the internal system bus for media devices such as the DVD drive.

Caution – If you used the `halt` command or the Stop-A key sequence to reach the `ok` prompt, issuing the `probe-ide` command can hang the system.

CODE EXAMPLE 4-3 shows sample output from the `probe-ide` command.

CODE EXAMPLE 4-3 `probe-ide` Command Output

```
{1} ok probe-ide
Device 0  ( Primary Master )
          Not Present

  Device 1  ( Primary Slave )
          Not Present

  Device 2  ( Secondary Master )
          Not Present

  Device 3  ( Secondary Slave )
          Not Present

{1} ok
```

4.2.4 `show-devs` Command

The `show-devs` command lists the hardware device paths for each device in the firmware device tree. CODE EXAMPLE 4-4 shows some sample output.

CODE EXAMPLE 4-4 `show-devs` Command Output

```
{1} ok show-devs
/i2c@1f,464000
/pci@1f,700000
/pci@1e,600000
/pci@1d,700000
/pci@1c,600000
/memory-controller@1,0
/SUNW,UltraSPARC-IIIi@1,0
/memory-controller@0,0
/SUNW,UltraSPARC-IIIi@0,0
/virtual-memory
/memory@m0,0
/aliases
/options
/openprom
/chosen
/packages
/i2c@1f,464000/idprom@0,ae
/i2c@1f,464000/nvram@0,ae
/pci@1f,700000/scsi@1
/pci@1f,700000/scsi@1/disk
/pci@1f,700000/scsi@1/tape
/pci@1e,600000/network@2,1
```

CODE EXAMPLE 4-4 `show-devs` Command Output *(Continued)*

```
/pci@1e,600000/network@2
/pci@1e,600000/ide@d
/pci@1e,600000/pmu@6
/pci@1e,600000/isa@7
/pci@1e,600000/ide@d/cdrom
/pci@1e,600000/ide@d/disk
/pci@1e,600000/pmu@6/gpio@80000000,b9
/pci@1e,600000/isa@7/ipmc@0,2e8
/pci@1e,600000/isa@7/serial@0,3e8
/pci@1e,600000/isa@7/serial@0,3f8
/pci@1e,600000/isa@7/rtc@0,70
/pci@1e,600000/isa@7/flashprom@2,0
/pci@1e,600000/isa@7/ipmc@0,2e8/i2c@81
/pci@1e,600000/isa@7/ipmc@0,2e8/i2c@81/motherboard-fru-prom@81,a8
/pci@1e,600000/isa@7/ipmc@0,2e8/i2c@81/dimm-spd@81,a6
/pci@1e,600000/isa@7/ipmc@0,2e8/i2c@81/dimm-spd@81,a4
/pci@1e,600000/isa@7/ipmc@0,2e8/i2c@81/dimm-spd@81,a2
/pci@1e,600000/isa@7/ipmc@0,2e8/i2c@81/dimm-spd@81,a0
/pci@1d,700000/ethernet@2,1
/pci@1d,700000/ethernet@2
/pci@1c,600000/network@2,1
/pci@1c,600000/network@2
/openprom/client-services
/packages/SUNW,asr
/packages/SUNW,fru-device
/packages/SUNW,i2c-ram-device
/packages/obp-tftp
/packages/kbd-translator
/packages/dropins
/packages/terminal-emulator
/packages/disk-label
/packages/deblocker
/packages/SUNW,builtin-drivers
{1} ok
```

4.3 OpenBoot Diagnostics

See the *OpenBoot PROM Enhancements for Diagnostic Operation* (817-6957) document for information on OpenBoot diagnostics. This document can be found on the Sun documentation web site at:

http://www.sun.com/documentation

4.4 Recent Diagnostic Test Results

Summaries of the results from the most recent power-on self-test (POST) and OpenBoot diagnostics tests are saved across power cycles.

4.4.1 Viewing Recent Test Results

1. **Go to the `ok` prompt.**
2. **Do either of the following:**

- To see a summary of the most recent POST results, type:

```
ok show-post-results
```

- To see a summary of the most recent OpenBoot diagnostics test results, type:

```
ok show-obdiag-results
```

This command produces a system-dependent list of hardware components, along with an indication of which components passed and which failed POST or OpenBoot diagnostics tests.

4.5 OpenBoot Configuration Variables

Switches and diagnostic configuration variables stored in the IDPROM determine how and when POST diagnostics and OpenBoot Diagnostics tests are performed. This section explains how to access and modify OpenBoot configuration variables. For a list of important OpenBoot configuration variables, see TABLE 4-1.

Changes to OpenBoot configuration variables take effect at the next reboot.

4.5.1 Viewing and Setting OpenBoot Configuration Variables

- **Halt the server to display the `ok` prompt.**

- To display the current values of all OpenBoot configuration variables, use the `printenv` command.

  The following example shows a short excerpt of this command's output.

```
ok printenv
Variable Name         Value                          Default Value

diag-level            min                             min
diag-switch?          false                           false
```

- To set or change the value of an OpenBoot configuration variable, use the `setenv` command:

```
ok setenv diag-level max
diag-level =          max
```

- To set OpenBoot configuration variables that accept multiple keywords, separate keywords with a space.

4.5.2 Using the `watch-net` and `watch-net-all` Commands to Check the Network Connections

The `watch-net` diagnostics test monitors Ethernet packets on the primary network interface. The `watch-net-all` diagnostics test monitors Ethernet packets on the primary network interface and on any additional network interfaces connected to the system board. Good packets received by the system are indicated by a period (.). Errors such as the framing error and the cyclic redundancy check (CRC) error are indicated with an X and an associated error description.

- **To start the `watch-net` diagnostic test, type the `watch-net` command at the `ok` prompt.**

```
{0} ok watch-net
Internal loopback test -- succeeded.
Link is -- up
Looking for Ethernet Packets.
'.' is a Good Packet. 'X' is a Bad Packet.
Type any key to stop.............................
```

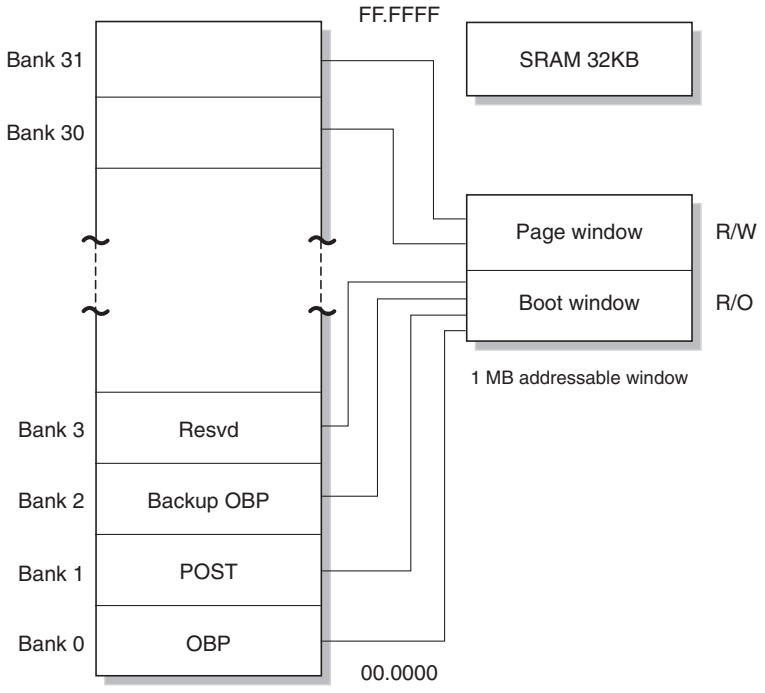
- **To start the** `watch-net-all` **diagnostic test, type** `watch-net-all` **at the** `ok` **prompt.**

```
{0} ok watch-net-all
/pci@1f,0/pci@1,1/network@c,1
Internal loopback test -- succeeded.
Link is -- up
Looking for Ethernet Packets.
'.' is a Good Packet. 'X' is a Bad Packet.
Type any key to stop.
```

4.6 Firmware Memory Map

The Netra CP3010 board boots from the 1-Mbyte system flash PROM device that contains the POST code and OpenBoot PROM. The contents map of this PROM is shown in FIGURE 4-1. User-developed code can also be programmed into the user flash memory space in the form of *drop-ins*. The system flash can be upgraded by running a program out of the OpenBoot PROM. It is not otherwise accessible by the user.

FIGURE 4-1 System Flash PROM Map



Boot window (R/O) = Bank 0,2,4,6
Page window (R/W) = Bank 0 - 31
Flash Size 16 MB
System Flash Size 2 MB
User Flash Size 14 MB
Bank Size 512KB
No. of Banks 32

4.7 Automatic System Reconfiguration

Note – Automatic system reconfiguration (ASR) is not the same as automatic server restart, which the Netra™ CT 900 server also supports.

Automatic system reconfiguration (ASR) consists of self-test features and an auto-configuring capability to detect failed hardware components and unconfigure them. By enabling ASR, the server is able to resume operating after certain nonfatal hardware faults or failures have occurred.

If a component is monitored by ASR and the server is capable of operating without it, the server automatically reboots if that component develops a fault or fails. This capability prevents a faulty hardware component from stopping operation of the entire system or causing the system to fail repeatedly.

If a fault is detected during the power-on sequence, the faulty component is disabled. If the system remains capable of functioning, the boot sequence continues.

To support this degraded boot capability, the OpenBoot firmware uses the 1275 client interface (by means of the device tree) to mark a device as either *failed* or *disabled*, creating an appropriate status property in the device tree node. The Solaris OS does not activate a driver for any subsystem marked in this way.

As long as a failed component is electrically dormant (not causing random bus errors or signal noise, for example), the system reboots automatically and resumes operation while a service call is made.

Once a failed or disabled device is replaced with a new one, the OpenBoot firmware automatically modifies the status of the device upon reboot.

Note – ASR is not enabled until you activate it (see Section 4.7.4, "Enabling ASR" on page 4-16).

4.7.1 Setting Autoboot Options

The `auto-boot?` setting controls whether the firmware automatically boots the operating system after each reset. The default setting is `true`.

The `auto-boot-on-error?` setting controls whether the system attempts a degraded boot when a subsystem failure is detected. Both the `auto-boot?` and `auto-boot-on-error?` settings must be set to `true` to enable an automatic degraded boot.

- **To set the switches, type:**

```
ok setenv auto-boot? true
ok setenv auto-boot-on-error? true
```

Note – The default setting for `auto-boot-on-error?` is `false`. Therefore, the system does not attempt a degraded boot unless you change this setting to `true`. In addition, the system does not attempt a degraded boot in response to any fatal nonrecoverable error, even if degraded booting is enabled. For examples of fatal nonrecoverable errors, see Section 4.7.2, "Error-Handling Summary" on page 4-15.

4.7.2 Error-Handling Summary

Error handling during the power-on sequence can be summarized in the following three ways:

- If no errors are detected by POST or OpenBoot Diagnostics, the system attempts to boot if `auto-boot?` is `true`.
- If only nonfatal errors are detected by POST or OpenBoot Diagnostics, the system attempts to boot if `auto-boot?` is `true` and `auto-boot-on-error?` is `true`.

Note – If POST or OpenBoot Diagnostics detect a nonfatal error associated with the normal boot device, the OpenBoot firmware automatically unconfigures the failed device and tries the next-in-line boot device, as specified by the `boot-device` configuration variable.

- If a fatal error is detected by POST or OpenBoot Diagnostics, the system does not boot regardless of the settings of `auto-boot?` or `auto-boot-on-error?`. Fatal nonrecoverable errors include the following:
  - Failure of all CPUs
  - Failure of all logical memory banks
  - Failure of flash RAM cyclical redundancy check (CRC)
  - Failure of critical field-replaceable unit (FRU) PROM configuration data
  - Failure of critical application-specific integrated circuit (ASIC)

4.7.3 Reset Scenarios

Three OpenBoot configuration variables, `diag-switch?`, `diag-trigger`, and `diag-script`, control how the system runs firmware diagnostics in response to system reset events.

The standard system reset protocol bypasses POST and OpenBoot Diagnostics unless `diag-switch?` is set to `true`. The default setting for this variable is `false`. Because ASR relies on firmware diagnostics to detect faulty devices, `diag-switch?` must be set to `true` for ASR to run. For instructions, see Section 4.7.4, "Enabling ASR" on page 4-16.

To control which reset events, if any, automatically initiate firmware diagnostics, use `diag-trigger`. For detailed explanations of these variables and their uses, see Section 4.1.1, "Controlling POST Diagnostics" on page 4-2.

4.7.4 Enabling ASR

1. **At the system `ok` prompt, type:**

```
ok setenv diag-switch? true
ok setenv auto-boot? true
ok setenv auto-boot-on-error? true
```

2. **Set the `diag-trigger` variable to `power-on-reset`, `error-reset`, or `user-reset`.**

   For example, type:

```
ok setenv diag-trigger user-reset
```

3. **Type:**

```
ok reset-all
```

The system permanently stores the parameter changes and boots automatically if the OpenBoot variable `auto-boot?` is set to `true` (its default value).

Note – To store parameter changes, you can also power-cycle the system by using the On/Standby button in the front panel.

4.7.5 Disabling ASR

1. **At the system `ok` prompt, type:**

```
ok setenv diag-switch? false
```

2. Type:

```
ok reset-all
```

The system permanently stores the parameter change.

Note – To store parameter changes, you can also power-cycle the system by using the On/Standby button in the front panel.

CHAPTER 5

Hardware and Functional Description

This chapter contains the following sections:

5.1 Hardware Architecture

The Netra CP3010 board is an ATCA node board with one or two UltraSPARC IIIi processors. The card can be hot-swapped in an ATCA midplane and supports two gigabit Ethernet interfaces as Base Fabric and two gigabit SERDES interfaces as Extended Fabric to support a redundant Dual Star topology.

The Netra CP3010 board supports four Very Low Profile (VLP) DDR-1 DIMMs, which can support the maximum memory of 8 Gbytes. (For single-CPU configurations, the maximum is 4 Gbytes).

The I/O subsystem is structured around two JBus-PCI ASICs (application-specific integrated circuit), which are the bridges between the CPU JBus and the PCI buses. Each JBus-PCI ASIC has two PCI leafs, for a total of four PCI buses. The master JBus-PCI ASIC supports two PCI buses (33 MHz on the PCI-A leaf and 66 MHz on the PCI-B leaf). The slave JBus-PCI ASIC supports two 66-MHz PCI buses out of the PCI-A leaf and PCI-B leaf.

The Base Fabric interface, Extended Fabric interface, and SAS controller are connected to 66-MHz PCI leafs.

The Netra CP3010 board supports two PMC cards for PCI expansion. Both the PMC cards are interfaced with the PCI-A leaf, which is 33 MHz, 64-bit, and 5V tolerant.

The master JBus-PCI ASIC's 33 MHz leaf is used to connect the Southbridge chip. The Southbridge chip has a built-in IDE controller and supports the Compact Flash interface. The Southbridge chip provides dual RS-232 serial ports which are used for console access. These ports are available through the front as well as the rear panel.

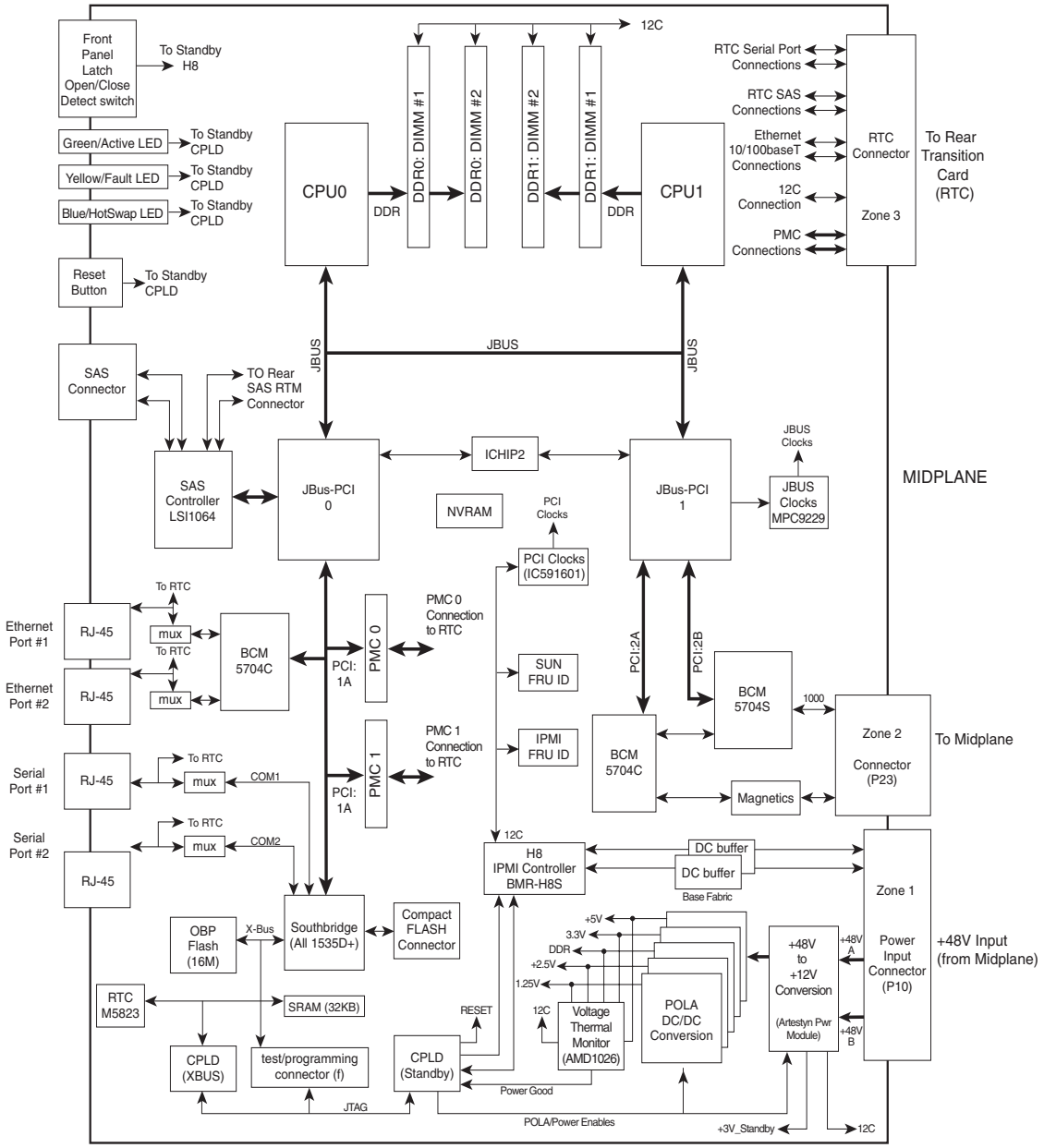
The H8 Intelligent Platform Management controller (IPMC) requires a serial connection to communicate with SPARC host CPUs. The Southbridge chip provides a serial port, which is used to interface with the H8 controller. The Pigeon Point H8 IPMC monitors all the critical functions of the board, responds to commands from the shelf manager, and reports events. In addition, the Southbridge chip provides serial port routing to the H8 and the Base Fabric Ethernet controller for the Netconsole function.

The boot flash memory is also interfaced on the XBus. The PCI-A leaf is part of the boot path. The boot path is: JBus, master JBus-PCI PCI-A leaf, Southbridge, XBus, flash memory.

The ATCA backplane provides redundant –48V power connections, and the Netra CP3010 board derives the necessary power by using on-board DC-DC converters. Standby power is generated separately from –48V and is provided for hardware management circuitry.

FIGURE 5-1 is a block diagram of the Netra CP3010 board.

FIGURE 5-1 Block Diagram



5.1.1 UltraSPARC IIIi Processor

This section provides a brief description of the salient features of the UltraSPARC IIIi processor, its package, and its socket. For more extensive information on the UltraSPARC IIIi+, see the *UltraSPARC IIIi Processor User's Manual* at http://www.sun.com/documentation.

5.1.1.1 Overview

The UltraSPARC IIIi processor is a high-performance, highly integrated, superscaler processor implementing the 64-bit SPARC-V9 RISC architecture. It contains a 32-Kbyte instruction cache and a 64-Kbyte data cache. The chip has a built-in 1-Mbyte Level2 cache, which uses a 32-byte cache line.

The UltraSPARC IIIi processor contains a DDR-1 SDRAM memory controller, a JBus controller, and power management capabilities. The chip is housed in a 959-pin ceramic Pin Grid Array (cPGA) package. The Netra CP3010 board has an on-board socket where the UltraSPARC IIIi processor resides.

5.1.1.2 UltraSPARC IIIi Processor Speed

The UltraSPARC IIIi processor supports a core frequency of up to 1.8 GHz. The maximum supported JBus speed is 200 MHz, and the maximum DDR speed is 166 MHz. The CPU core speed and JBus and DDR speeds in the Netra CP3010 board depend upon the total board power budget, which cannot exceed 200W (per the PICMG 3.0 R1.0 specification).

The targeted CPU core frequency in the Netra CP3010 board is 1.06 GHz.

5.1.1.3 UltraSPARC IIIi Processor Package

The UltraSPARC IIIi processor package is a 959-pin ceramic cPGA package. The pin-grid array on the chip is keyed so the chip can be inserted in the socket only in the correct orientation. The keying is accomplished by removing pin A1 from the chip and angling that corner so it does not fit in any of the other right-angle corners.

5.1.1.4 UltraSPARC IIIi Processor Socket

The UltraSPARC IIIi processor socket is a 959-pin ball grid array (BGA) zero-insertion-force socket. The socket is designed to be zero-insertion-force; that is, no compression is needed for the chip to make electrical contact to the pins of the

socket. However, some compression (from the heatsink) is useful in keeping the module assembly in place during shock and vibration testing. Approximately 60 pounds of force is recommended for this application.

5.1.2 DDR Memory Subsystem

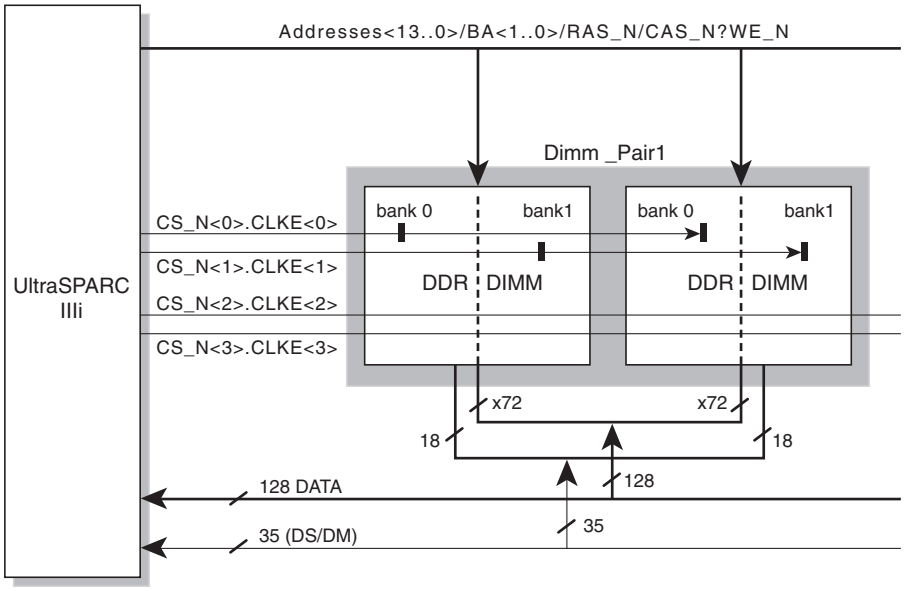
The Netra CP3010 board supports dual UltraSPARC IIIi processor CPUs, and each CPU has its own DDR memory controller. Each memory controller supports two DIMMs. Each DIMM has a 72-bit-wide data bus (64+8 ECC) and up to 14 address bits. The DIMMs run at 2.5 volts and take a 1.25 reference voltage (Vtt). PC-2100 is capable of running at up to 133 MHz.

The UltraSPARC IIIi processor defines two memory channels operating in parallel to logically create a 128-bit-wide memory data path. ECC (error correcting code) is generated and checked across 128 bits of data, allowing for significant improvement in error correction. Due to this architecture, DDR DIMMs must be installed in matched pairs.

The Netra CP3010 board can support a total of four DIMMs and a maximum memory capacity of 8 Gbytes (using 4 2-Gbyte DIMMs). The maximum memory capacity and memory speed depends upon the board's total power budget.

A DDR memory diagram is shown in FIGURE 5-2.

FIGURE 5-2 DDR Memory Diagram



5.1.2.1 Key Features

Some of the key features of the memory subsystem are:

- Four 184-pin DDR-1 VLP DIMM slots require registered/buffered DIMMs (two DIMMs per CPU)
- Maximum SDRAM clock frequency of 133 MHz
- Supports single-bank or dual-bank SDRAM DIMMs
- Supports 4-Rank DIMMs
- Memory controller supports 128 bits data plus 9-bit ECC
- Supports 512-Mbyte and 1-Gbyte DDR-1 SDRAMs (four 1-GByte or eight 512-MByte)
- Supports four internal SDRAM device banks
- Maximum of 8 Gbytes
  - Peak memory bandwidth of 4.2 Gbytes/sec at 133 MHz
  - SSTL_2 inputs and output

5.1.2.2 ECC Checking and Generation

All memory transfers have ECC. The UltraSPARC IIIi processor's memory controller unit (MCU) performs ECC generation and checking. A 9-bit syndrome is generated using the Hsiaos algorithm for each 128 bits of data. This 9-bit syndrome enables single-bit error correction and multiple-bit error detection.

The SQ generates the syndrome of data coming in from the JBus before it is sent to the MCU. This data is stored with the data when a write operation is performed by the MCU. When the data is read, the syndrome is also read and used to verify the correctness of the data. When a correctable or uncorrectable error is detected, the information is stored with the data and sent back to the JBus. If the data is for a foreign request, the uncorrectable error and correctable error information is sent with it on the J_ADTYPE bus.

5.1.2.3 Serial Presence Detect

The Netra CP3010 board supports autoconfiguration using serial presence detect (SPD). The DIMMs have small EEPROM devices that store their configuration data according to the SPD format. The OpenBoot PROM reads this data via the I^2C management bus and uses it to initialize the UltraSPARC IIIi processor memory controllers.

A 128-byte region of the SPD EEPROM is available for user data storage, allowing a limited form of FRU information to be implemented for the DIMMs.

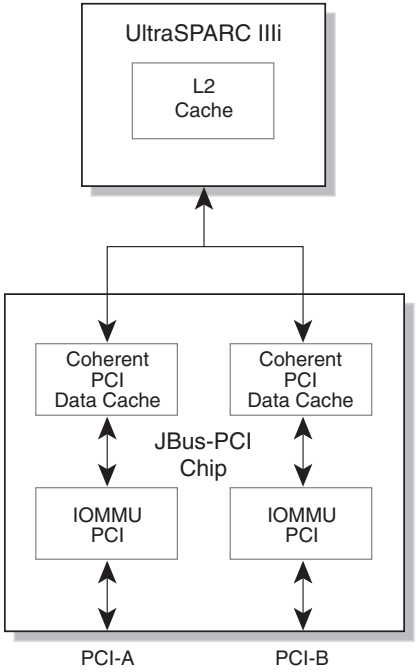
5.1.3 JBus

The JBus is the system bus developed for the UltraSPARC IIIi+ series processors. The JBus is the main interconnect between the CPUs and JBus-PCI ASICs. It uses 1.5V DTL signaling and is designed to run at a maximum speed of 200 MHz. The peak bandwidth for JBus is 2.56 Gbytes/sec at 200 MHz. FIGURE 5-3 is a diagram of the JBus.

JBus has a 128-bit address/data bus (J_AD[127:0]). In addition, there are several control bits that are part of the bus specification. There are 4-word parity bits (J_ADP[3:0]) for the data and address bus. An 8-bit code (J_ADTYPE[7:0]) identifies the packet type on the address and data bus. There are also encoded snoop information and flow control signals (J_PACK0-6[2:0]). The last few signals are:

- J_PAR, which is the parity bit for the control signals
- J_RST_L, which is the JBus reset signal (this does not reset the memory controller)
- J_POR_L, which is the JBus power on reset (this does reset the memory controller)
- J_ERR, which indicates an error on JBus.

FIGURE 5-3 JBus Diagram



5.1.3.1 JBus Device Arbitration

There is no central system arbiter in a JBus system. Each device arbitrates for control of the bus by driving six identical output signals, J_REQ_OUT{0:5}, which are distributed to the J_REQ_IN{0:5} inputs of the remaining devices. The distribution is arranged symmetrically such that each device {i} has each of its J_REQ_IN_L{j} signals driven by the J_REQ_OUT_L{i} signals of the other devices {j}, where i and j are determined by the agent IDs. See TABLE 5-1 for the arbitration scheme.

TABLE 5-1 JBus Arbitration Scheme

Device	{i}	CPU0 {j}	CPU1 {j}	JBus-PCI ASIC 0 {j}	JBus-PCI ASIC 1 {j}
CPU0	0		0	3	4

TABLE 5-1 JBus Arbitration Scheme

Device	{i}	CPU0 {j}	CPU1 {j}	JBus-PCI ASIC 0 {j}	JBus-PCI ASIC 1 {j}
CPU1	1	5			2
JBus-PCI ASIC 0 (slave)	4	2	3		0
JBus-PCI ASIC 1 (master)	5	1	2	5	

5.1.3.2 JBus Device Mapping

Each device in a JBus domain is assigned a unique agent ID, J_ID{4:0}. The agent ID is a 5-bit code that defines the identity of each device in a JBus domain (TABLE 5-2). For hardware configuration, the UltraSPARC IIIi processor offers access only to the J_ID{2:0} bits, and the JBus-PCI ASICs offers access only to the J_ID{1} bit.

TABLE 5-2 JBus Device Agent IDs

Device	J_ID{4:0}
CPU0	x0000
CPU1	x0001
JBus-PCI 0 PCI leaf	x1100
JBus-PCI 0 PCI leaf B	x1101
JBus-PCI 1 PCI leaf A	x1110
JBus-PCI 1 PCI leaf B	x1111

5.1.3.3 JBus Boot Path

The UltraSPARC IIIi processor systems do not have a dedicated boot bus. The JBus-PCI ASIC 0 is defined by its agent ID as a system master and opens its PCI-1a bus as a boot path when exiting the reset state.

In the Netra CP3010 board, the boot PROM is located on the Southbridge chip XBus, which therefore occupies a position on the PCI1a bus.

5.1.3.4 JBus Termination Scheme

JBus devices use different types of termination depending on whether they are at the center or end of the bus. The JBus architecture (reference 9) defines two types of device internal termination scheme, DTL-1 and DTL-2. Because the Netra CP3010 board has four nodes, it uses the DTL-1 scheme. Signals on the end nodes are

terminated with a 50-ohm pull-up and a 50-ohm pull-down, and have the pull-up active in receive mode. Signals on the intermediate nodes are terminated with a 50-ohm pull-up and a 25-ohm pull-down, and are high-impedance in receive mode. The terminations are configured using two input pins, DOWN_25 and UP_OPEN (TABLE 5-3).

TABLE 5-3 JBus Device Termination

Device	Node Type	DOWN_25	UP_OPEN
CPU0	Intermediate	1	1
CPU1	Intermediate	1	1
JBus-PCI 1 (master)	End	0	0
JBus-PCI 2 (slave)	End	0	0

5.1.4 I/O Subsystem

The I/O subsystem is designed around three bridges, two JBus-PCI ASICs and one 1535D+ Southbridge chip. A JBus-PCI ASICs is the bridge between the JBus and the PCI bus. The Ali1535D+ Southbridge chip is the bridge between the PCI bus and the IDE, XBus, and Super I/O functions.

5.1.4.1 JBus-PCI ASICs

The JBus-PCI ASIC is a companion core-logic ASIC to the UltraSPARC IIIi processor. The JBus-PCI ASIC and the UltraSPARC IIIi processor communicate through JBus. The central task of JBus-PCI ASIC is to be the point of access to I/O and system interrupts.

The Netra CP3010 board uses two JBus-PCI ASICs as the bridge from the JBus to the PCI. One JBus-PCI ASIC is configured as the master (JID[1]=1) and supports a 33-MHz PCI bus (PCI-A leaf) and a 66-MHz PCI bus (PCI-B leaf). The other JBus-PCI ASIC is configured as the slave (JID[1]=0) and supports two 66-MHz PCI buses through the PCI-A and the PCI-B leafs. The boot path is through the master JBus-PCI ASIC PCI-A leaf.

JBus-PCI ASIC has a built-in PCI arbiter for each leaf. The internal PCI arbiters are used for PCI arbitration. JBus-PCI ASIC's PCI-A leaf includes an interrupt block (Mondo Dispatch) that receives system interrupts from the external IChip and also deals with interrupts generated from activity within the PCI interface unit itself. The interrupt unit communicates with the JBus cluster to send the interrupt to the JBus.

Master JBus-PCI ASIC PCI-A Leaf

This bus originates from the master JBus-PCI ASIC. It is a 33-MHz, 32/64-bit, version 2.2 compliant PCI bus. The Netra CP3010 board uses this bus to interface with two PMC slots, one Broadcom BCM5704C Ethernet controller (which provides two 10/100/1000BASE-T Ethernet ports), and the Southbridge chip (Ali1535D+). BCM5704C is a 10/100BASE-T Ethernet controller. On the Netra CP3010 board, it is used as 10/100/1000BASE-T for maintenance ports. Also, the 64-bit BCM5704C device is configured as a 32-bit device due to layout routing constraints.

Master JBus-PCI ASIC PCI-B Leaf

The PCI-B leaf from the master JBus-PCI ASIC is 66 MHz, 64-bit, and PCI version 2.2 compliant. The SAS Controller LSISAS1064 is connected to this bus.

Slave JBus-PCI ASIC PCI-A Leaf

The PCI-A leaf from the slave JBus-PCI ASIC is 66 MHz, 64-bit, and PCI version 2.2 compliant. The BCM5704C gigabit Ethernet controller is connected on this bus. BCM5704C provides dual 10/100/1000BASE-T Ethernet ports to the ATCA backplane as a Base Fabric interface.

Slave JBus-PCI ASIC PCI-B Leaf

The PCI-B leaf from the slave JBus-PCI ASIC is 66 MHz, 64-bit, and PCI version 2.2 compliant. The BCM5704S gigabit Ethernet controller is connected on this bus. BCM5704S provides dual SERDES ports to the ATCA backplane as an Extended Fabric interface.

5.1.4.2 10/100/1000BASE-T Ethernet (Base Fabric)

The Netra CP3010 board provides two Ethernet 10/100/1000BASE-T interfaces to meet the Base Fabric requirements of ATCA. The Broadcom BCM5704C Ethernet controller is used to provide dual Base Fabric interfaces. The BCM5704C is integrated MAC and GMII. These controllers are connected to the 66-MHz, 64-bit-wide PCI bus.

The controllers are magnetically coupled to the ATCA backplane for a TPE network connection. Each interface supports 10BASE-T, 100BASE-TX and 1000BASE-T operation conforming to the IEEE 802.3 specification. The controllers individually negotiate transfer speeds when their network links are established.

Gigabit Ethernet With SERDES (Extended Fabric)

The Netra CP3010 board provides two gigabit Ethernet SERDES interfaces to meet the Extended Fabric requirements of ATCA in the Dual Star topology configuration. The Broadcom BCM5704S is used to provide the Extended Fabric interface. These controllers are connected to the 66-MHz, 64-bit-wide PCI bus.

10/100BASE-T Ethernet

The Netra CP3010 board provides two 10/100BASE-T interfaces as maintenance ports. These ports are available through the front panel or the rear transition card. A Broadcom Ethernet controller (BCM5704C) is used to provide 10/100BASE-T functions. These controllers are connected to a 33-MHz, 32-bit-wide PCI bus.

BCM5704C is an integrated Ethernet MAC, physical layer, and transceiver in one chip. The controllers are magnetically coupled to RJ-45 receptacles for a TPE network connection.

SAS Controller (LSISAS1064)

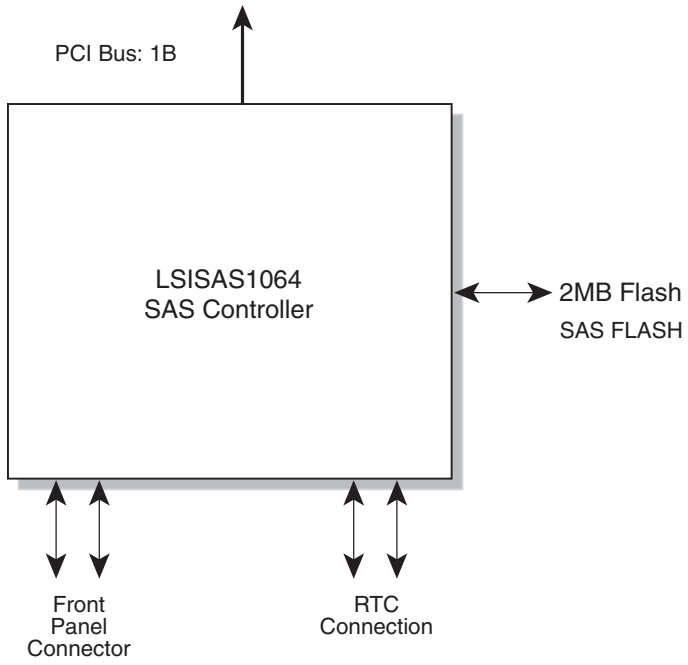
The Netra CP3010 board provides dual SAS channel ports for storage through the front panel and RTM. The LSI Logic LSISAS1064 SAS controller is used for access to high-speed storage subsystems.

The LSISAS1064 features include:

- Four fully independent physical interface functions (phs)
- Each phy supports 3.0 Gbit/sec and 1.5 Gbit/sec SAS data transfers
- A serial, point-to-point, enterprise-level storage interface
- A scalable interface that supports up to 128 devices through multiple expanders
- Operates at 66 MHz PCI
- Supports 64-bit data transfers
- Complies with the PCI Local Bus Specification, Revision 2.3
- Uses a dedicated ARM926 processor

FIGURE 5-4 is a block diagram of the SAS controller.

FIGURE 5-4 SAS Controller Block Diagram



PMC Slots

The Netra CP3010 board provides two 64-bit, 33-MHz PMC slots for PCI expansion. The PMC interface is designed to support PIM for rear I/O access availability. The Netra CP3010 board supports 5V PMC modules, and the slots are keyed accordingly. The maximum power consumption supported for each PMC slot is 7.5W.

Southbridge Chip

The Netra CP3010 board uses the ALi M1535D+ Southbridge chip from Acer Labs. M1535D+ is a highly integrated system I/O chipset in a 328-pin BGA package. The following functions of Southbridge are used on the Netra CP3010 board:

- PCI to ISA bridge with XBus and LPC interfaces
- Three serial interfaces
- PCI IDE controller (Ultra DMA 100)
- Southbridge GPIO to Interrupt H8

The Southbridge chip is interfaced on a 33-MHz, 32-bit PCI leaf.

PCI-ISA Bridge

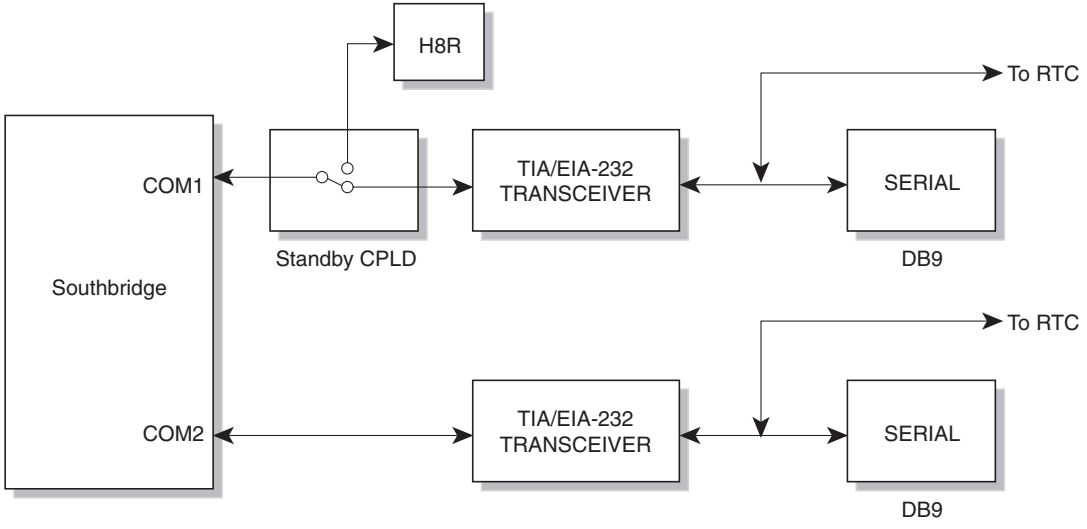
The ISA bus is an I/O bus that runs at 8 MHz. The Netra CP3010 board uses only a subset of this bus, called XBus. The OpenBoot PROM flash, SRAM, XBUS CPLD, and real-time clock are interfaced onto the XBus.

Serial Interfaces

The Netra CP3010 board provides two serial ports using Southbridge chip super I/O functions. Both the serial ports are available for front as well as rear access. The COM1 port is the output to the `netconsole` utility. When a serial port cable is connected to the front or rear COM1 port, `netconsole` is disabled and the signal passes through the standby CPLD. Without a serial port cable connected, the serial port output from the Southbridge chip is redirected to `netconsole` through the H8S. The MAX3243 RS-232 transceivers are used for these serial interfaces. The MAX3243 provides the required ESD protection to the serial ports.

FIGURE 5-5 shows a block diagram of the serial interface.

FIGURE 5-5 Serial Interface Block Diagram



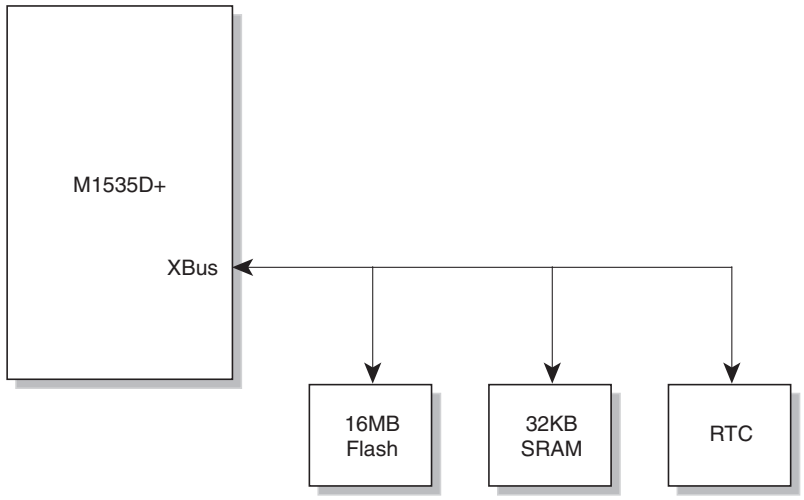
The Southbridge chip provides one additional two-wire serial port. This is used to interface with the IPMB controller BMR-H8S. This interface is referred to as the payload interface, and enables messaging between the SPARC and management interface.

XBus Controller

The M1535D+ provides an XBus controller. XBus is an 8-bit, parallel interface provided by the Southbridge chip for general use in supporting ISA style devices.

In the Netra CP3010 board, the XBus is used to interface with the flash, SRAM, XBus CPLD, and real-time clock (M5823), as seen in FIGURE 5-6.

FIGURE 5-6 XBus Block Diagram



The Southbridge chip provides chip selects for these devices, as detailed in TABLE 5-4.

TABLE 5-4 XBus Chip Select

Chip Select	Device	Notes
ROMKBCS	PROM	Shared address map, access controlled by SRAMEN GPIO signal
	SRAM	
RTCAS	RTC	Dedicated read/write/chip select signals

TABLE 5-4 XBus Chip Select

Chip Select	Device	Notes
PCS0	PROM paging register	Internal to the XBus CPLD to control the FLASH paging mechanism
PCS1	Not used	
PCS2	Not used	

Flash PROM and SRAM

The flash PROM and SRAM devices are used by the OpenBoot PROM and POST. The PROM is a 16-Mbyte flash device. Two Mbytes contain the OpenBoot PROM, OpenBoot Diagnostics, and POST firmware suites. The SRAM is a 32-Kbyte device available to OpenBoot PROM and POST for storage of temporary variables. Following a system reset, the Southbridge chip provides a boot path to the PROM to run the OpenBoot PROM system initialization code.

As a result of enabling parallel interrupts (APIC mode) within the Southbridge chip, the most significant bit (msb) of the XBus address bus is unavailable on the XA19 pin. In the Netra CP3010 board, XA19 is therefore obtained by latching PCI_AD19 directly from the PCI bus, using the first PCI clock pulse after the FRAME# signal is asserted.

For the Netra CP3010 board, a 16-Mbyte flash device is addressed. This is accomplished by breaking up the 1-Mbyte Southbridge chip addressable window into two 512-Kbytes segments. The lower segment always addresses a boot block of 512 Kbytes, whereas the upper segment can page in any of the 32 512-Kbyte pages in the flash device. The lower segment boot block can be at the 0-Mbyte, 1-Mbyte, 2-Mbyte, or 3-Mbyte offset, which is controlled by the IPMC. The lower segment is protected from write operations at all times. (If writing a boot page, it must be mapped to the upper 512 Kbytes.) In case of a flash-update failure, or a need to allow booting from userflash, the IPMC can control which of the four boot pages is selected. The upper segment can page in any of the 32 pages (including boot pages).

SRAM is mapped to upper 16M-32K (0xFF8000-0xFFFFFF). To access SRAM, SRAMEN GPIO 34 from the Southbridge chip must be set high and the CPLD register's page window must be set to page 31. FIGURE 5-7 shows the XBus memory map, FIGURE 5-8 shows the page window address aliasing map, and FIGURE 5-9 shows the boot page address aliasing map.

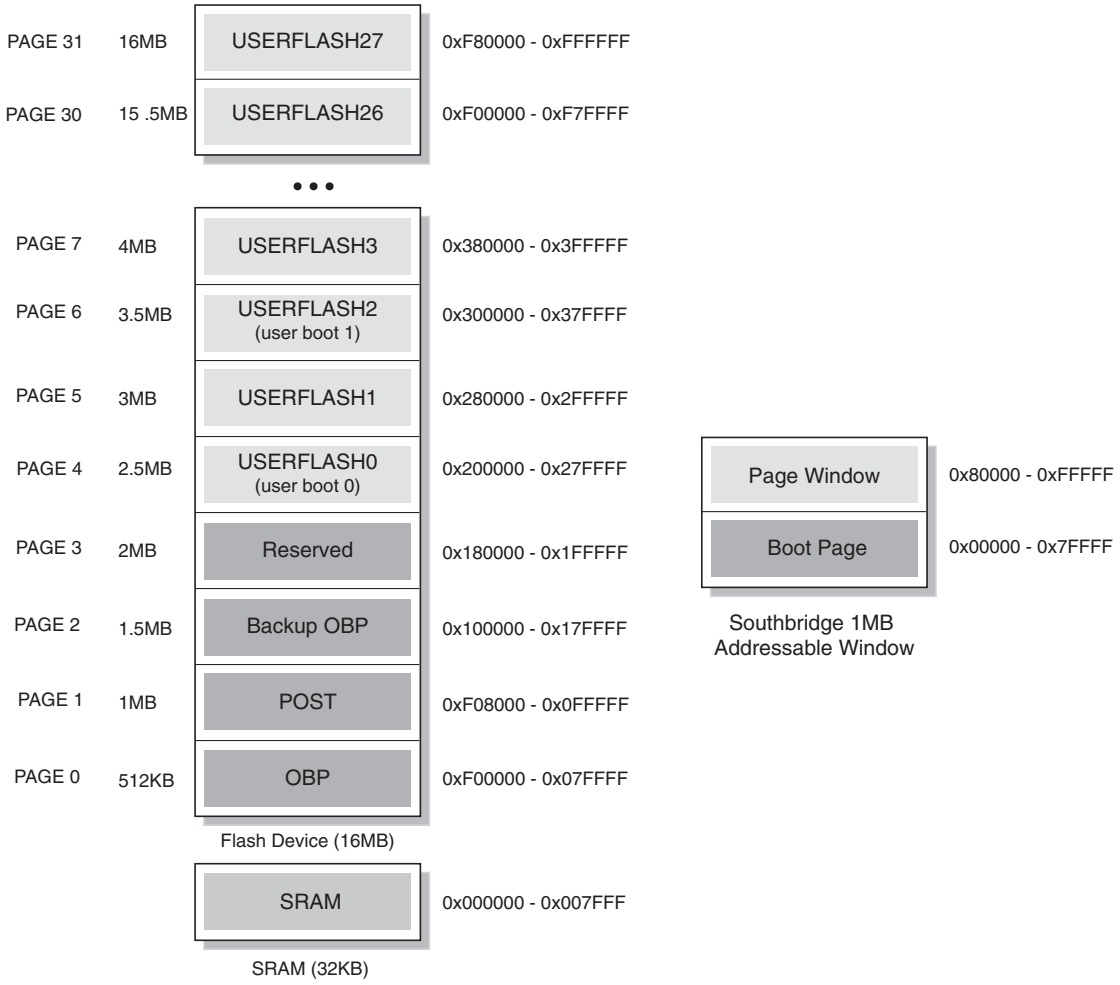

PAGE 31
16MB
USERFLASH27
0xF80000 - 0xFFFFFF
PAGE 30
15 .5MB
USERFLASH26
0xF00000 - 0xF7FFFF
PAGE 7
4MB
USERFLASH3
0x380000 - 0x3FFFFF
PAGE 6
3.5MB
USERFLASH2
(user boot 1)
0x300000 - 0x37FFFF
PAGE 5
3MB
USERFLASH1
0x280000 - 0x2FFFFF
PAGE 4
2.5MB
USERFLASH0
(user boot 0)
0x200000 - 0x27FFFF
PAGE 3
2MB
Reserved
0x180000 - 0x1FFFFF
PAGE 2
1.5MB
Backup OBP
0x100000 - 0x17FFFF
PAGE 1
1MB
POST
0xF08000 - 0x0FFFFF
PAGE 0
512KB
OBP
0xF00000 - 0x07FFFF
Flash Device (16MB)
SRAM
0x000000 - 0x007FFF
SRAM (32KB)
Page Window
0x80000 - 0xFFFFF
Boot Page
0x00000 - 0x7FFFF
Southbridge 1MB
Addressable Window

FIGURE 5-7 XBus Memory Map

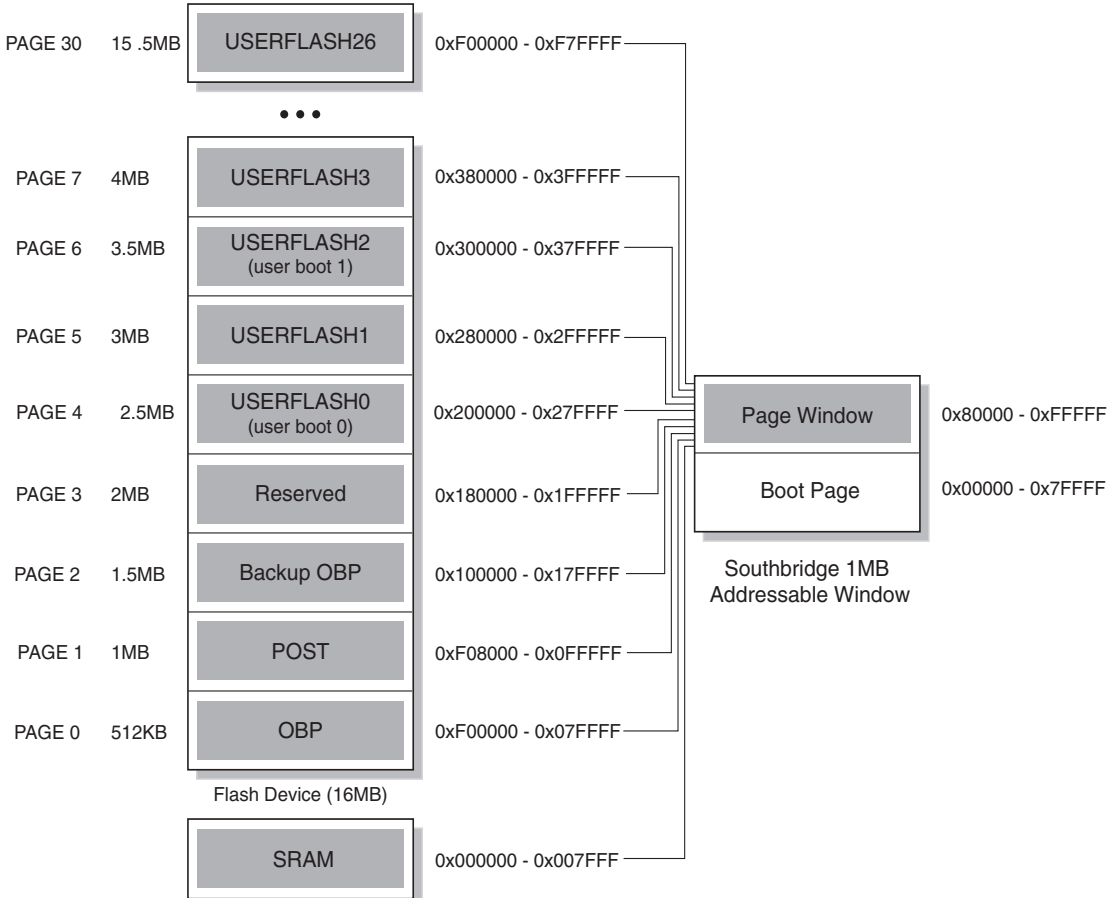
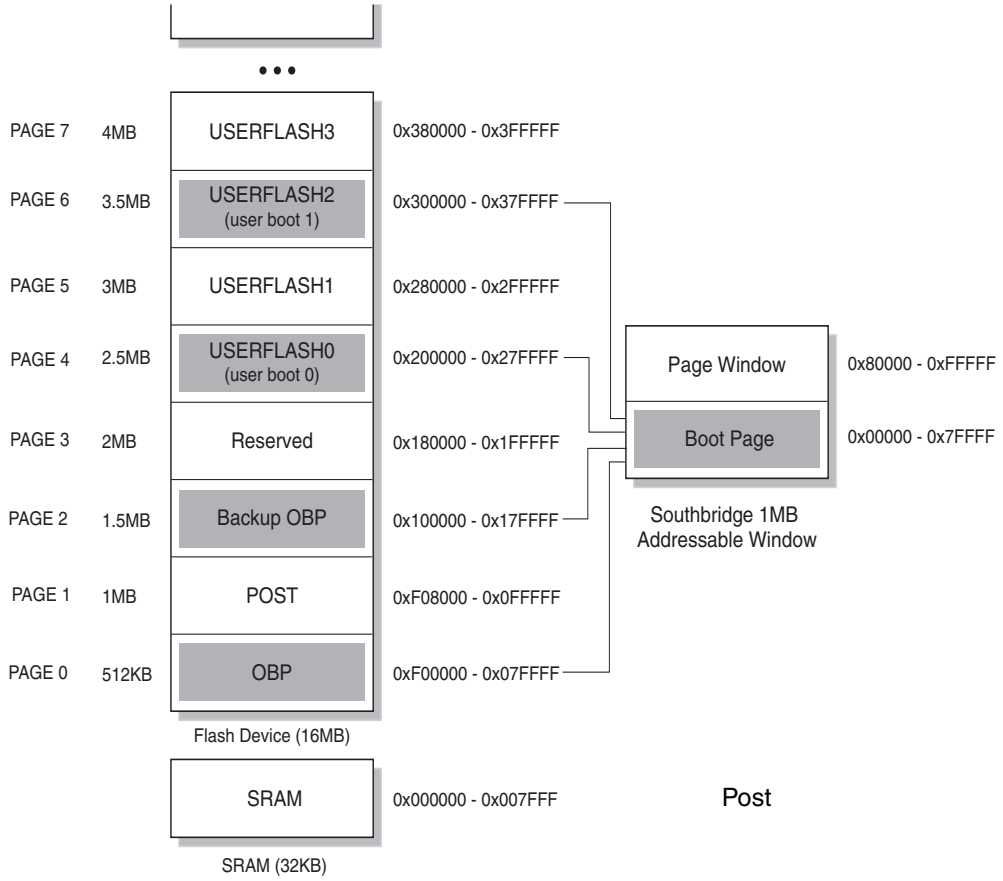


FIGURE 5-8 Page Window Address Aliasing

FIGURE 5-9 Boot Page Address Aliasing



Real-Time Clock (M5823)

The Solaris OS uses the real-time clock (RTC) as its reference source for calendar date and time. Under normal circumstances, synchronization occurs once at boot time, after which the processors maintain an internal record using their STICK counters.

The Netra CP3010 board uses an Acer M5823 device for RTC functions. The M5823 is a full BDC clock and calendar. The real-time clock counts seconds, minutes, hours, date of month, month, day of week, and year, with leap year compensation.

A battery provides the backup power to the RTC when power is not present.

PCI IDE Controller

The IDE controller is an Acer M5229 device that resides inside the M1535D+ Southbridge chip. This is a dual controller, but only the primary bus is utilized to connect the Compact Flash card in the Netra CP3010 board. The bus can operate at DMA mode 4 speed. At the present time, direct memory access (DMA) is a new enhancement to the Compact Flash specification, and the majority of Compact Flash cards use programmed I/O (PIO). There is a performance impact compared to a normal IDE disk.

Southbridge GPIO to Interrupt H8

A Southbridge chip GPIO pin connects to an interrupt input pin of the H8. This enables OS-level interrupts to be sent to the H8 due to the limitations of the watchdog within the H8 (primarily, insufficient time resolution).

GPO29 from the Southbridge chip is used to connect to /IRQ0 on the H8.

Compact Flash

The Netra CP3010 board provides the option of supporting an IDE Compact Flash (CF) card. To support higher memory capacity, a Type I CF socket is provided. The Compact Flash card is not hot-swappable and there is no access to the CF socket once the board is installed in an ATCA chassis.

Southbridge GPIO

The Southbridge chip GPIO pins are configured for the uses summarized in TABLE 5-5. Further description of the signal usage can be found in the relevant sections of this specification.

TABLE 5-5 Southbridge Chip GPIO

Pin	Signal	Function
GPO29	H8_INT	Interrupt to H8 on /INT0
GPO34	SRAMEN	Output selecting between the flash PROM and the SRAM
GPO36	PROMWE#	Output enabling writes to the flash PROM
GPO39	SB_IPMC_RST#	Output to put the IPMC in reset
GPO44	IDE_SWRST#	Output to the IDE bus to force a Compact Flash reset

5.1.5 Intelligent Platform Management Controller (IPMC)

The Renesas H8S/2168 provides the IPM controller (IPMC) function on the Netra CP3010 board. The IPMC provides PICMG 3.0 board management functionality, and it interfaces to the payload through a serial interface.

The IPMC is responsible for the following:

- Dual buffered IPMB interfaces to connect to IPMB-0
- Hot-swap latch input and LED control
- Payload power control
- Payload E-Keying control
- Payload power and temperature monitoring
- Access to on-board I^2C devices
- IPMI FRU
- Sun FRU ID
- Netconsole connectivity to Base Fabric chipset
- System monitor (ADM1026)
- Sensors monitoring and event generation

5.1.5.1 Payload Interface

The IPMC communicates with the SPARC chip through the serial interface, which connects to the M1535D+ Southbridge (COM3). The interface protocol is SIPL (Serial Interface Protocol Lite), which is based on the IPMI-defined basic mode of the serial/modem interface. The baudrate supported is 9600 bps.

5.1.5.2 Intelligent Platform Management Bus (IPMB)

The IPMC provides dual buffered IPMB interfaces to the IPMB-0 bus on the PICMG 3.0 backplane. The I^2C channels on the IPMC are connected to the IPMB-A and IPMB-B through the LTC4300A I^2C buffers. The I^2C buffers enable the board's I^2C to be isolated from the backplane until the board is fully seated and the I^2C bus on the backplane is idle.

5.1.5.3 Hot-Swap Latch and LEDs

Hot-swapping is supported by monitoring of the hot-swap handle switch and LED control. The handle switch goes directly to one of the GPIO pins on the IPMC. The LEDs are controlled through the memory mapped registers on the standby complex programmable logic device (CPLD).

5.1.5.4 Payload Power Control

The IPMC is able to control individual power rails to the payload. This is accomplished through the memory mapped registers in the standby CPLD.

5.1.5.5 Payload Base and Fabric Interface E-Keying Control

The IPMC provides E-Keying for the payload interfaces to the backplane. PICMG mandates that the software hooks for E-Keying are present, but it does not mandate that anything must be done in hardware in response. There is no hardware support for E-Keying in the Base Fabric interfaces. E-Keying for the Fabric interfaces is accomplished by setting the SIG_DET lines active into the BCM5704S. This is done through memory mapped registers in the standby CPLD.

5.1.5.6 IMPI and Sun FRU Information

Both IPMI and Sun FRU information (FRU IDs) are supplied. IPMI FRU information is supported through an 8-Kbyte serial EEPROM (AT24C64B) on the system management I^2C bus. The Sun FRU information is supported through an additional 8-Kbyte serial EEPROM.

5.1.5.7 Netconsole Connectivity to Base Fabric Chipset

The IPMC serial port 0 connects to the serial port on the Southbridge chip through the standby CPLD. The standby CPLD provides the appropriate control to enable this serial port to be routed either to the front or back (when a connection is detected on either of these ports). If there is no connection to the front or rear serial port, this serial port is routed to the H8 and from there to the Base Fabric chipset to enable Netconsole functionality.

The IPMC I^2C port 0 is used to connect to the Broadcom chipset for the Base Fabric interface.

5.1.5.8 System Monitor (ADM1026) and Thresholds

The Analog Devices ADM1026 is used for system monitoring functions. The ADM1026 is interfaced with the IPMC and the IPMC firmware is responsible for monitoring these sensors.

Voltage Monitoring

The ADM1026 measures most of the board voltages. The ADM1026 has one temperature sensor embedded in the device itself and supports two remote sensing channels that require external diodes for temperature sensing. These two remote sensors are used for measuring CPU die (or junction) temperatures.

The ADM1026 measures the voltages listed in TABLE 5-6. The ADM1206 and H8 firmware monitors these voltages. When the voltages are within regulations, the board functions with no warnings. When any voltage goes out of regulation beyond approximately ± 7%, a `Critical Warning` is generated and presented to the shelf manager. When any voltage goes out of regulation beyond approximately ± 10%, the H8 initiates a board shutdown.

Also shown in TABLE 5-6 are voltage shutdown limits set by hardware components on the Netra CP3010 board itself. In addition to the H8 shutdown, these on-board components monitor certain voltage rails and force a shutdown whenever any of these voltages go beyond the `On Board Hardwired Shutdown` voltage.

TABLE 5-6 Voltage Sensor Thresholds

			ADM1026 Generated Critical Warning (approx. 7%)		H8 Initiated Shutdown (approx. 10%)		
Sensor Number	**Net Name**	**Voltage**	**Lower**	**Upper**	**Lower**	**Upper**	**On Board Hardwired Shutdown**
5	+12V	12V	11.16V	12.6V	11V	13.2V	≤ 11.0V
6	–12V	–12V	–11.16V	–12.84V	–10.8V	–13.2V	
7	VCC(+5VDC)	5V	4.8V	5.2V	4.78V	5.23V	± 5%
8	VDD_3V	3.3V	3.07V	3.53V	3V	3.6V	± 10%
9	+3VSB	3.3V	3.07V	3.53V	2.97V	3.63V	≤ 2.93V
10	VBAT	3V	2.79V	No upper critical	No shutdown options		No upper thresholds, only lower thresholds.
11	VDD_CORE0	1.2V	1.12V	1.28V	1.08	1.32V	
12	VDD_CORE1	1.2V	1.12V	1.28V	1.08	1.32V	
13	VTT	1.25V	1.18V	1.34V	1.16V	1.38V	≤ 1.15V
14	VDD_1.2V	1.2V	1.12V	1.28V	1.08V	1.32V	
15	VCCTM	2.5V	2.33V	2.68V	2.25V	2.75V	≤ 2.1V
16	VDD_2.5V	2.5V	2.37V	2.68V	2.36V	2.75V	≤ 2.35V
17	VDD_1.5V	1.5V	1.4V	1.61V	1.35V	1.65V	≤ 1.2V

Temperature Monitoring

The ADM1026 also monitors the CPU die (or junction) temperatures of each CPU on the Netra CP3010 board. The ADM1206 and H8 firmware reports a minor, major, or critical alarm when the temperature of either CPU goes beyond the thresholds listed in TABLE 5-7. Also, if the temperature of either CPU goes beyond the `Emergency H8 Shutdown` value listed in TABLE 5-7, the H8 initiates a board shutdown independent of the shelf manager.

TABLE 5-7 CPU Temperature Alarms

Minor Alarm (UNC)	**Major Alarm (UC)**	**Critical Alarm (UNR)**	**Emergency H8 Shutdown**
>95° C	>115° C	> 120° C	> 127° C

The H8 temperature alarm equivalents are:

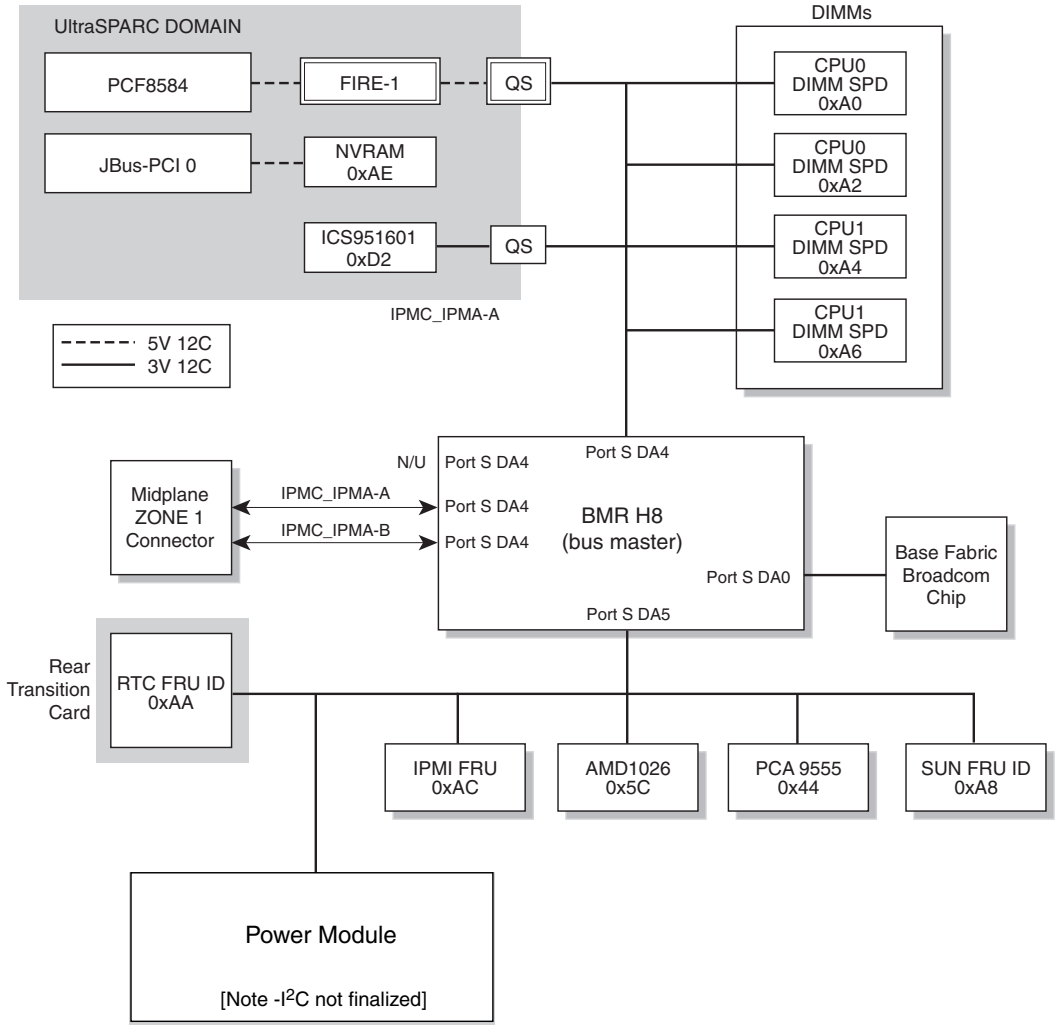
Minor Alarm = Upper Non Critical (UNC)
Major Alarm = Upper Critical (UC)
Critical Alarm = Upper Non Recoverable (UNR)
Emergency H8 Shutdown = Emergency H8 Shutdown (EMR)

Caution – These voltage and temperature thresholds should not be changed under normal operating conditions.

5.1.5.9 I^2C Architecture

FIGURE 5-10 is a block diagram of the I^2C architecture.

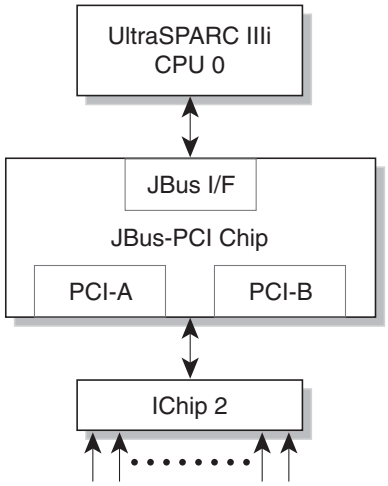
FIGURE 5-10 I²C Block Diagram



5.2 Interrupts

As shown in FIGURE 5-11, all the interrupts are delivered to the UltraSPARC IIIi processor through dedicated JBus transactions. These transactions are identical to the interrupt packets defined by Sun architecture.

FIGURE 5-11 Interrupts Block Diagram



In the Netra CP3010 board, the Sun IChip2 receives all the system interrupts and encodes the interrupts into a 6-bit interrupt vector. The interrupt vector is then issued to the JBus-PCI ASIC. The JBus-PCI ASIC issues a single JBus transaction for each active interrupt to the UltraSPARC IIIi processor.

The BMR-H8S interrupt IRQ0 is also connected to the Southbridge chip to enable the OS to interrupt the H8. Its use is left to the software application running on the H8.

5.2.1 Interrupt Transactions

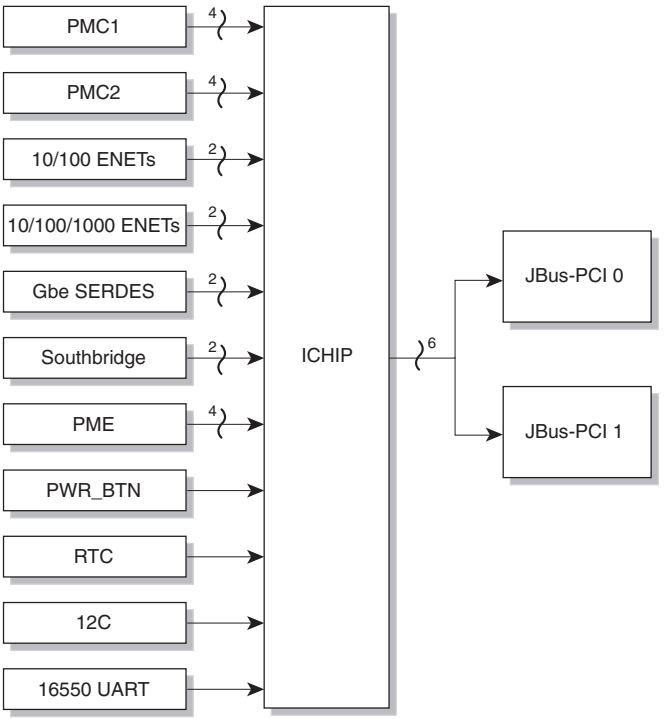
Interrupts are delivered to the processors through dedicated transactions on the JBus. These transactions employ the interrupt packets defined by the Sun architecture. The packet includes the agent ID of the JBus source, the agent ID of the

JBus target, and the source of the interrupt. Interrupt packets for I/O devices and for JBus or PCI bus errors are issued by the JBus-PCI ASICs. The processors can also initiate interrupts to each other. These interrupts are known as *cross-calls*.

5.2.2 IChip

In the Netra CP3010 board, the Sun IChip ASIC is used as an interrupt concentrator, receiving all hardware interrupts and passing them to the JBus-PCI ASICs for conversion to JBus packets. The IChip samples its discrete interrupt inputs on a round-robin basis and submits the results of each sample to the JBus-PCI ASICs in sequential format. Each interrupt is encoded as a 6-bit vector. An idle code is passed when no interrupt is detected. FIGURE 5-12 is a diagram of the IChip.

FIGURE 5-12 IChip Diagram



The IChip has two types of interrupt input, level interrupts and pulse interrupts. Only level interrupts are used in the Netra CP3010 board. Most level interrupt inputs are active-low, but four active-high inputs are included for legacy support.

Each 6-bit vector uniquely defines the interrupt source device and translates to the interrupt number offset (INO) used in the JBus packet. TABLE 5-8 shows the I/O device interrupt sources.

TABLE 5-8 I/O Device Interrupt Sources

Source	JBus-PCI ASIC	PCI Bus	IChip Input	Type	INO
Not used			PCI0_INT0	Level-low	0x00
Not used			PCI0_INT1	Level-low	0x01
Not used			PCI0_INT2	Level-low	0x02
Not used			PCI0_INT3	Level-low	0x03
PMC0 INTA	0	PCI1a	PCI1_INT0	Level-low	0x04
PMC0 INTB	0	PCI1a	PCI1_INT1	Level-low	0x05
PMC0 INTC	0	PCI1a	PCI1_INT2	Level-low	0x06
PMC0 INTD	0	PCI1a	PCI1_INT3	Level-low	0x07
Base Fabric GbE 0	0	PCI2a	PCI2_INT0	Level-low	0x08
Base Fabric GbE 1	0	PCI2a	PCI2_INT1	Level-low	0x09
Not used			PCI2_INT2	Level-low	0x0A
Not used			PCI2_INT3	Level-low	0x0B
PMC1 INTA	0	PCI1a	PCI3_INT0	Level-low	0x0C
PMC1 INTB	0	PCI1a	PCI3_INT1	Level-low	0x0D
PMC1 INTC	0	PCI1a	PCI3_INT2	Level-low	0x0E
PMC1 INTD	0	PCI1a	PCI3_INT3	Level-low	0x0F
Management port Ethernet 0	0	PCI1a	PCI4_INT0	Level-low	0x10
Management port Ethernet 1	0	PCI1a	PCI4_INT1	Level-low	0x11
Not used			PCI4_INT2	Level-low	0x12
Not used			PCI4_INT3	Level-low	0x13
Southbridge IRQ11	0	PCI1a	PCI5_INT0	Level-low	0x14
Southbridge IRQ5	0	PCI1a	PCI5_INT1	Level-low	0x15
Southbridge IRQ4	0	PCI1a	PCI5_INT2	Level-low	0x16
Southbridge IRQ3	0	PCI1a	PCI5_INT3	Level-low	0x17
Southbridge IRQ10	0	PCI1a	PCI6_INT0	Level-low	0x18
Not used			PCI6_INT1	Level-low	0x19

TABLE 5-8 I/O Device Interrupt Sources *(Continued)*

Source	JBus-PCI ASIC	PCI Bus	IChip Input	Type	INO
PCI2b PME	1	PCI2b	PCI6_INT2	Level-low	0x1A
Not used			PCI6_INT3	Level-low	0x1B
Extended Fabric GbE 0	1	PCI2b	PCI7_INT0	Level-low	0x1C
Extended Fabric GbE 1	1	PCI2b	PCI7_INT1	Level-low	0x1D
Not used			PCI7_INT2	Level-low	0x1E
IPMC interrupt			PCI7_INT3	Level-low	0x1F
Power button			OBIO0_INT0	Level-low	0x20
PCI1a PME	1	PCI1a	OBIO0_INT1	Level-low	0x21
Not used			OBIO0_INT2	Level-low	0x22
PCI2a PME	1	PCI2a	OBIO0_INT3	Level-low	0x23
Southbridge IRQ9	0	PCI1a	OBIO0_INT4	Level-low	0x24
PCI2b PME	1	PCI2b	OBIO0_INT5	Level-low	0x25
Southbridge IRQ7	0	PCI1a	OBIO0_INT6	Level-low	0x26
Southbridge IRQ6	0	PCI1a	OBIO0_INT7	Level-low	0x27
SAS interrupt	1	PCI2b	OBIO0_INT8	Level-low	0x28
Not used			OBIO0_INT9	Level-low	0x29
Not used			UPA_INT0	Level-low	0x2A
Not used			UPA_INT1	Level-low	0x2B
Southbridge IRQ1	0	PCI1a	OBDIO1_INT0	Level-high	0x2C
Southbridge IRQ12	0	PCI1a	OBDIO1_INT1	Level-high	0x2D
Not used			OBDIO1_INT2	Level-high	0x2E
Not used			OBDIO1_INT3	Level-high	0x2F

5.2.3 Southbridge Chip Interrupts

In the Netra CP3010 board, the Southbridge chip interrupt controller must be configured for APIC mode. This enables individual interrupts to be accessed on discrete pins of the Southbridge chip, rather than multiplexed onto a single serial line. Internal devices are each allocated to appropriate interrupts as part of the

configuration process. The Southbridge chip has the capability to provide 10 interrupts. In the Netra CP3010 board, only two are used. TABLE 5-9 lists the Southbridge chip interrupts.

TABLE 5-9 Southbridge Chip Interrupts

Interrupt	Function
IRQ1	Serial controllers
IRQ3	Not used
IRQ4	Not used
IRQ5	Not used
IRQ6	Not used
IRQ7	Not used
IRQ9	Not used
IRQ10	Primary IDE channel
IRQ11	Not used
IRQ12	Not used

5.2.4 JBus-PCI ASIC Interrupt Processing

The IChip interrupt vectors are passed to both JBus-PCI ASICs in parallel. A JBus-PCI ASIC processes an interrupt only if the source is recognized as belonging to one of its PCI leaves. To achieve this, the JBus-PCI ASIC has an Interrupt Routing Register and an Interrupt Mapping Register. These registers are initialized by the OpenBoot PROM to assign ownership of individual interrupt sources to the correct JBus-PCI ASIC and PCI leaf.

When a JBus-PCI ASIC recognizes an IChip interrupt vector, it dispatches an interrupt packet to the JBus. The packet defines the interrupt source in an 11-bit field known as the interrupt number (INR). The INR is composed of the interrupt group number (IGN), which specifies the JBus agent ID, and the interrupt number offset (INO), which corresponds to the IChip vector.

The JBus-PCI ASIC provides a state machine for each level interrupt assigned to it. The state machine has three states: idle, received, and pending. The state machine moves from the idle to received state when an assigned interrupt is recognized. Once the corresponding interrupt packet has been dispatched to the JBus, the state machine moves to the pending state. The pending state prevents further interrupt packets from being generated each time the IChip round-robin cycle returns to the same interrupt source. As part of the interrupt routine, the servicing processor must

both clear the IChip interrupt by writing to the appropriate register in the source device, and return the JBus-PCI ASIC state machine to the idle state by writing to the corresponding JBus-PCI ASIC Clear Interrupt Register.

5.2.5 Bus Error Interrupts

The JBus-PCI ASICs implement error checking on the JBus transfers. In addition, they respond to bus errors on the JBus and on each of their PCI buses. These errors are converted to interrupts and dispatched as JBus packets in exactly the same way as IO device interrupts. TABLE 5-10 shows the JBus-PCI ASIC error interrupts.

TABLE 5-10 JBus-PCI ASIC Error Interrupts

Error	INO
Uncorrectable JBus error	0x30
Correctable JBus error	0x31
JPCI bus A error	0x32
PCI bus B error	0x33
JBus bus error	0x34

5.2.6 H8 Interrupts

The H8/IRQ0 interrupt input is connected to a GPIO pin (GPO29) to enable the OS to interrupt the H8. The use of this interrupt is left to the application running on the H8.

5.3 Resets

The Netra CP3010 board supports two different types of resets, which can be triggered by several different methods. The two main types of resets are hard resets and soft resets.

5.3.1 Hard Reset

There are two ways to cause a hard reset. The first is when the system powers on and asserts the SYSTEM_POK signal, which connects to the PWRGD pin on the Master JBus-PCI ASIC and causes a hard reset. The JBus-PCI ASIC then asserts the J_POR_L and J_RST_L signals for 5 milliseconds (ms). The J_RST_L signal is kept asserted for 5 ms after the deassertion of the J_POR_L signal. The PCI reset pins are kept asserted until after the deassertion of the J_RST_L signal. This causes the entire system to reset.

A hard reset can also be generated by software. The CPU writes to the JBus-PCI ASIC to initiate a reset. This reset is similar to the hardware-initiated hard reset, except the JBus-PCI ASIC's clock PLLs are not reset. The Reset Source, Estar Control, Estar Init, and PCI PIO AFSR registers in the JBus-PCI ASIC preserve their state across the reset.

There are two different types of hard resets. In a long reset, J_POR_L and J_RST_L signals are asserted for 5 ms. In a short reset, J_POR_L is asserted for 32 JBus clocks and J_RST_L is asserted for 64 JBus Clocks. For the Southbridge chip, all hard resets must be long resets. FIGURE 5-13 is the block diagram and FIGURE 5-14 is the timing diagram for hard rests.

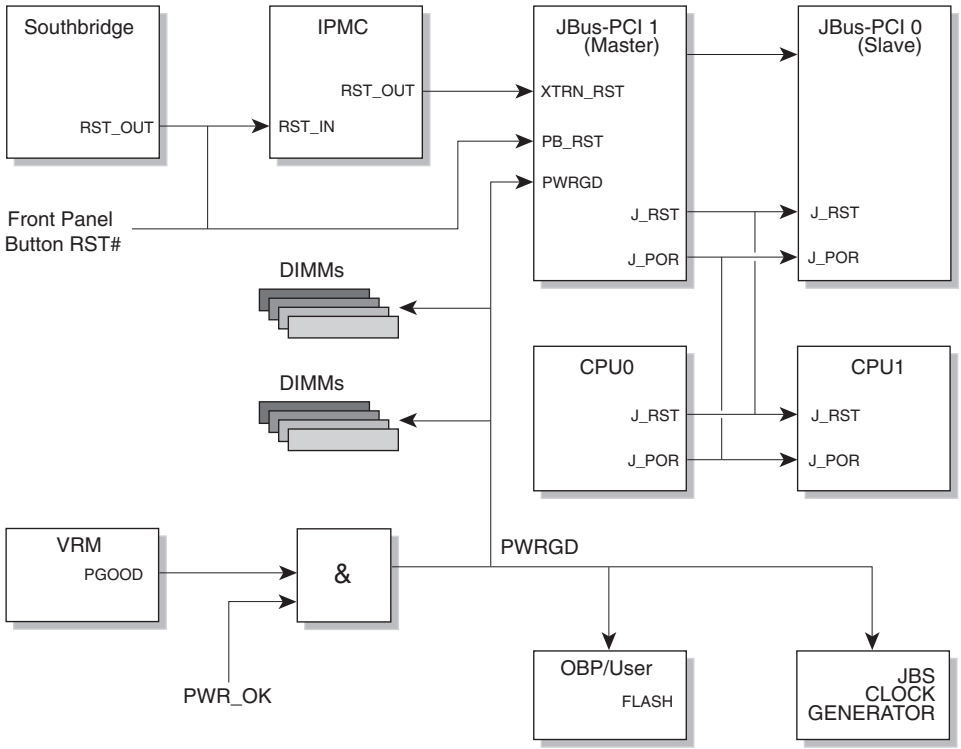
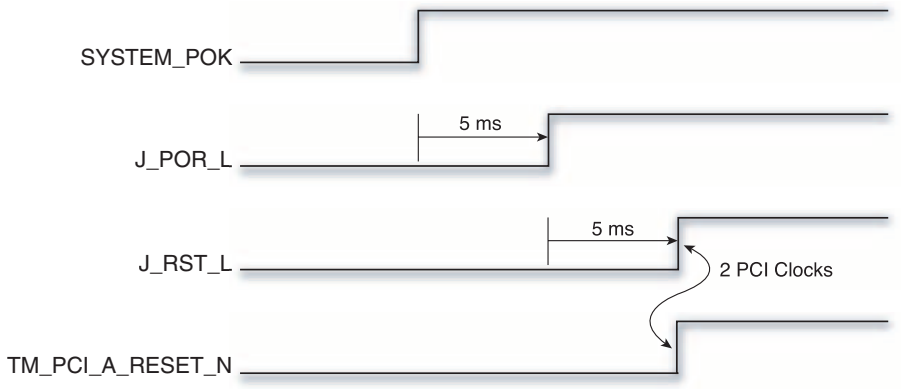


FIGURE 5-13 Hard Reset Block Diagram

FIGURE 5-14 Hard Reset Timing Diagram



5.3.2 Soft Reset

A soft reset is different from a hard reset in that the memory controller in the UltraSPARC IIIi processor continues to refresh memory to preserve the contents of the memory. The clock ratios for the CPUs are unaffected by a soft reset. The PCI resets are also generated during a soft reset.

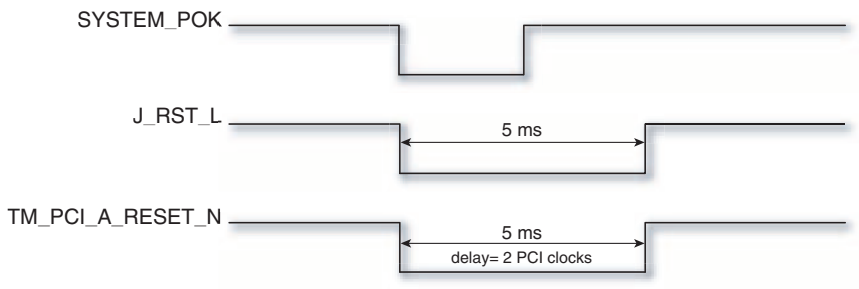
The Netra CP3010 board provides three possible sources for the soft reset in hardware, as well as a software-generated soft reset. Other than their origin, there is no difference between any of these resets.

Three hardware soft resets are generated by the host:

- IPMC – The IPMC can assert BUTTON_POR_N to reset the payload (host system).
- Watchdog reset – The watchdog timer can be programmed to issue either an XIR or reset of the host if there is a timeout.
- Front panel reset button – The front panel reset button can be used to reset the payload.

When any of the external events asserts the PB_RST input of JBus-PCI ASIC or when software issues a soft reset of the host, the J_RST_L signal is driven low for 5 ms (see FIGURE 5-15). This resets all the CPUs in the system. One or two PCI-clocks later the PCI resets are asserted, resetting the rest of the devices in the payload.

FIGURE 5-15 Soft Reset Timing Diagram

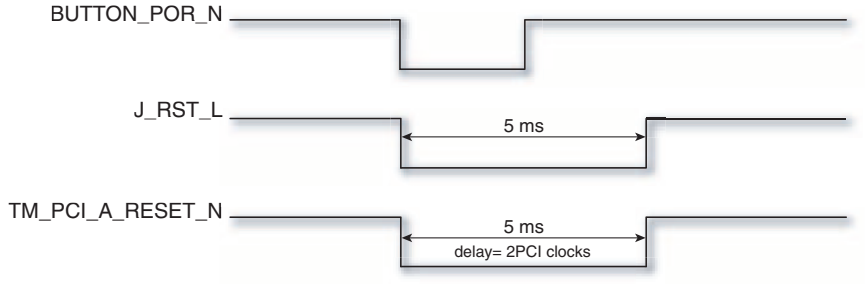


5.3.3 Externally Initiated Reset (XIR)

The XIR function on the Netra CP3010 board restarts a hung system without resetting it so that information can be retrieved from memory for analysis. An XIR can be initiated by pulsing the XTRN_RST# input of the master JBus-PCI ASICs (see FIGURE 5-16).

There are three ways to issue an XIR to the system. The first way is through setting a bit in the JBus-PCI ASIC that generates an XIR to the CPUs. The IPMC can also issue an XIR using the same input pin. The last method is using the watchdog timer. The watchdog timer can be set to generate either a reset or an XIR when a watchdog timeout occurs.

FIGURE 5-16 Externally Initiated Reset Timing Diagram



5.3.4 PCI Resets

When power is first turned on to the system, the PCI reset deasserts until the JBus-PCI ASIC begins operating. This is in violation of the PCI spec and can cause issues with PCI devices. The solution is to gate the PCI resets with the SYSTEM_POK signal, which ensures that the reset signal is held low until the JBus-PCI chip brings the system out of reset.

5.3.4.1 PCI Devices

PCI devices are reset by signals from the JBus-PCI ASICs. Each JBus-PCI ASIC generates a separate reset signal for each of its PCI buses. The JBus-PCI ASIC asserts the PCI reset signals during a POR event.

5.3.4.2 Southbridge Chip

Because the Southbridge chip is the source of PCI resets in the PC architecture, it does not have a PCI reset input. In the Netra CP3010 board, the Southbridge chip receives PCI resets via its PWG input. The Southbridge chip requires a delay of at least 2.5 ms after the reset is negated before the OpenBoot PROM can be accessed.

The delay is produced by implementing the Southbridge chip reset as a nominal 1.2 ms pulse at the leading edge of the PCI reset, derived from the 32.768 kHz resume clock. The P_RST# signal of the master JBus-PCI ASIC is used as the source of the reset. To meet the 2.5 ms requirement, this reset must be programmed for its maximum duration.

During the power on initialization sequence, the 2.5 ms requirement is met automatically because the master JBus-PCI chip delays release of the JBus from reset until after the PCI reset signals are negated. The PWRGD signal is therefore fed directly to the Southbridge PWG input at power-on.

5.3.4.3 IPMC Reset

The host software can reset the IPMC at any time by generating a low-going pulse on the GPO39 pin of the Southbridge chip. This pin connects to the IPMC_RST# signal.

The IPMC is also able to reset the host system by generating a low-going pulse on the RST_OUT# pin of the H8. This is connected to XTRN_RST# input of the master JBus-PCI chip and causes soft reset.

5.3.5 Processor Internal Resets

5.3.5.1 Software-Initiated Reset (SIR)

A software-initiated reset (SIT) is triggered by execution of an SIR instruction. An SIR resets only the processor that executes the instruction and has no effect on the remaining system.

5.3.5.2 Watchdog Reset (WDR)

If a processor tries to take a trap when the trap level is already at its maximum value (TL=MAX_TL), an error is generated, resulting in a watchdog reset (WDR). A WDR resets only the processor that executes the instruction and has no effect on the remaining system.

5.4 Clocks

5.4.1 System Clock Sources

TABLE 5-11 gives fundamental clock sources in the Netra CP3010 board. All are referenced from crystal sources. Other clocks within the system are derived from these crystal sources by synthesis or division.

TABLE 5-11 Clock Sources

Sl. No	Clock Frequency	Used By	Description
1	32.768 kHz	M5823	Time-of-Day chip used for RTC
2	12 MHz	CPU0 and CPU1	Sys Tic Clock
3	14.318 MHz	Southbridge chip	Used as Ref.clock
4	14.318 MHz	ICS 951601	Used as Ref.clock to generate other clocks
5	16 MHz	MC12429	Clock GEN for CPU, BELL, and JBus-PCI ASIC
6	25 MHz	BCM5704C	Used for 10/100BASE-T
7	25 MHz	BCM5704C	Used for 10/100BASE-T

TABLE 5-11 Clock Sources *(Continued)*

Sl. No	Clock Frequency	Used By	Description
8	25 MHz	BCM5704S	Used for SERDES
9	7.373 MHz	H8(IPMC)	Clock input to IPMI controller
10	29.48 MHz	CPLD	Used in CPLD
11	33 MHz	PMC slots, JBus-PCI ASIC, Southbridge chip, BCM5704C	PCI clocks
12	48 MHz	Ali M1535D+ (SB)	Used by Southbridge chip for USB ports
13	66 MHz	JBus-PCI ASICs, BCM5704C, BCM5704S, SAS1064	PCI clocks
14	75 MHz	SAS controller	
15	120 MHz to 160 MHz	CPUs and JBus-PCI ASICs for JBus clocks	The clock frequency is configurable
16	133 MHz	Memory DIMMs	CPU generates memory clocks for DIMM
17	1280 MHz to 1600 MHz	CPUs	Core frequency for CPU

5.4.2 JBus Device Clocks

5.4.2.1 JBus Clock Generator

All JBus devices in the system share a common clock. This is a low-voltage PECL signal generated by a Motorola MC9229FA clock generator and distributed by a Motorola MC100ES6014 phase-locked loop. FIGURE 5-17 shows a block diagram of the JBus Clock.

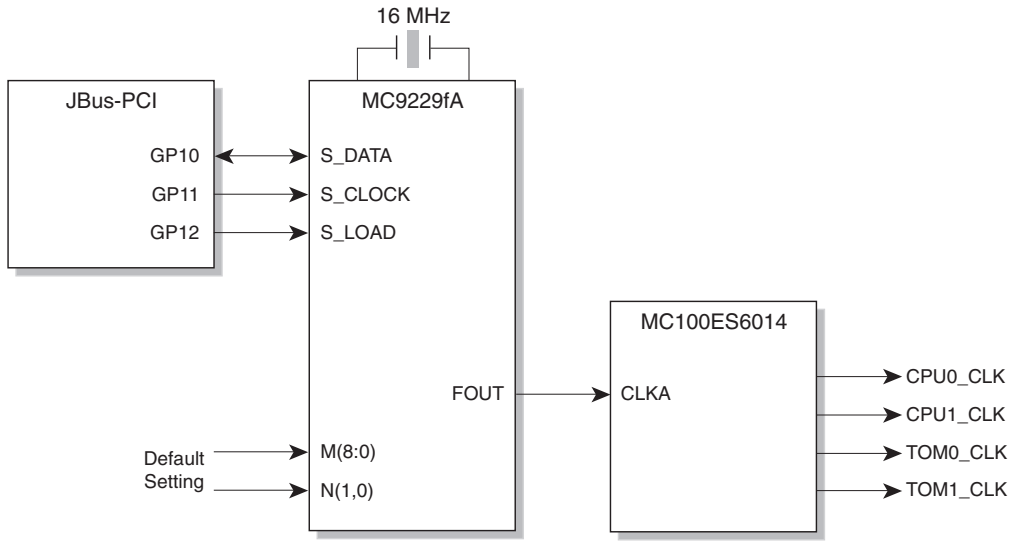
The JBus clock speed is determined by the MC9229FA, which synthesizes the desired frequency, Fout, from a 16-MHz crystal source, Fxtal, and programmable constants *M* and *N*, according to the formula:

Fout = (Fxtal / 8) x *M* / *N*

where *M* is a 9-bit binary code taking values from 200 to 400, and *N* is a 2-bit geometric code.

N{1,0}	Divisor
00	2
01	4
10	8
11	16

FIGURE 5-17 JBus Clock Block Diagram



The MC9229FA provides both parallel and serial interfaces for programming its *M* and *N* values. Following a power-on reset, the initial frequency is determined by the *M* and *N* settings programmed at the parallel interface. During system initialization, the serial interface is used to update the *M* and *N* values to reflect the actual required operating frequency appropriate for the speed grades of the components fitted. The serial interface is constructed from the *GPIO{2:0}* pins of the slave JBus-PCI ASIC. The GPIO pins must be *bit-banged* by the OpenBoot PROM to simulate the required transfer protocol for the MC9229FA.

5.4.2.2 CPU and Memory Clock Frequency Selection

The UltraSPARC IIIi processor contains internal phase-locked loops that synthesize clocks for the CPU core and the memory controller from the input JBus clock. The synthesizers have programmable ratios that can accommodate a wide variety of clock conditions (see FIGURE 5-18).

FIGURE 5-18 CPU and Memory Clock Diagram

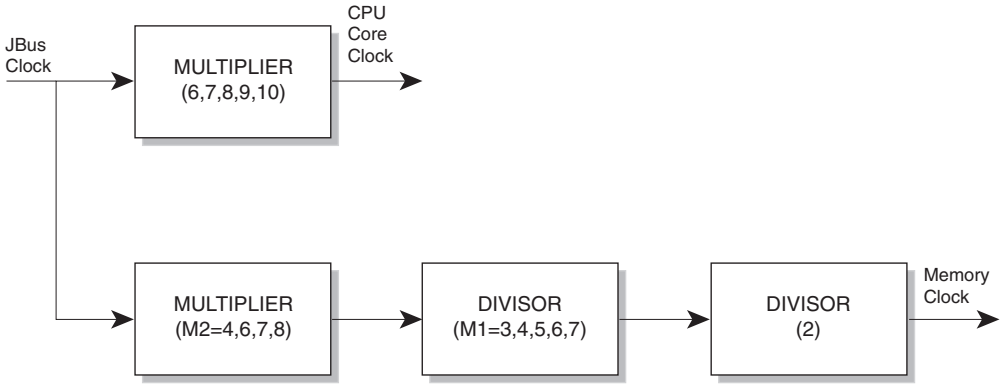


TABLE 5-12 lists the clock frequencies.

TABLE 5-12 Clock Frequencies

JBus Frequency (MHz)	Core Clock Multiple	CPU Core Clock Frequency (MHz)	M1	M2	Memory Clock Frequency (MHz)
120	6	720	4	3	80
0	6	0	6	4	0
138.86 – 152.38	7	972 – 1066.7	7	4	121.5 – 133.33
133.33 – 162	8	1066.7 – 1296	8	5	106.67 – 129.6
144 – 162	9	1296 – 1458	6	4	108 – 121.5
145.8 – 162	10	1458 – 1620	8	5	116.64 – 129.6

5.4.2.3 JBus Device Clock Programming

The required system clock operating frequencies are set by configuration parameters stored in a look-up table in the FRU ID EEPROM on the motherboard.

5.4.2.4 JBus Clock Generator Programming

In the Netra CP3010 board, the default frequency is set to 120 MHz, the minimum supported operating frequency of the JBus chipset. This frequency enables all systems to initialize from the same default setting, regardless of the speed grades of the components. The default value is determined by the *M* and *N* values configured at the parallel interface of the MC12429. TABLE 5-13 gives the JBus default clock frequencies.

TABLE 5-13 JBus Default Clock Frequencies

M{8:0}	N{1,0}	Default JBus Frequency (MHz)	Default CPU Core Frequency (MHz)	Default Memory Frequency (MHz)
011110000	01	120	720	80

Once the OpenBoot PROM has determined the actual operating frequency from the motherboard FRU ID EEPROM, the MC9229FA *M* and *N* values are revised via the serial interface.

Sudden disturbances in the output of the MC9229FA might cause instability in the various phase-locked loops, resulting in a crash. To prevent this, make changes to the JBus frequency progressively in 1-MHz steps.

5.4.3 STICK Clock

The STICK clock is a 12-MHz crystal oscillator. The STICK clock is provided primarily to allow the processors to maintain an internal source of real time. The crystal oscillator accuracy should be better than 25 ppm at 25ºC, which equates to 2.16 seconds of error per day.

5.4.3.1 STICK Timer

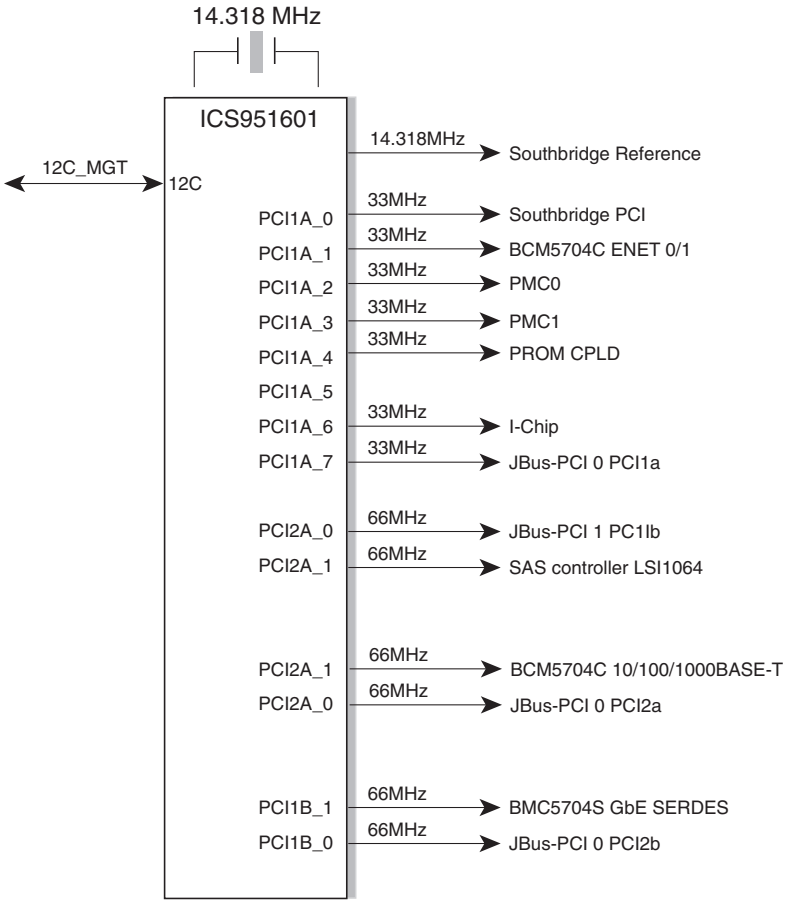
Each processor has a STICK input. The SPARC V9 architecture defines a system "tick" counter that provides a synchronized system-wide clock source for use by software applications. The counter provides a way to accurately time stamp multithreaded programs. The STICK timer is initialized from the RTC during boot, after which real time is maintained by counting overflows of the "tick" counter.

5.4.4 PCI Device Clocks

PCI clocks for devices on the four PCI buses are generated by an ICS951601 clock synthesizer with a 14.318-MHz crystal source. This device also generates two reference clocks for the Southbridge chip. Each of the four PCI buses has its own clock group operating at the appropriate frequency.

The ICS951601 is accessible through the I^2C management bus. This enables the OpenBoot PROM to turn off individual clocks to the PCI slots if cards are not detected when these slots are probed. FIGURE 5-19 is a block diagram of the PCI device clock.

FIGURE 5-19 PCI Device Clock Block Diagram



5.4.5 IO Device Clocks

5.4.5.1 RTC Clock

The RTC clock operates from a 32.768-kHz crystal. This is provided by a small crystal on the board. To allow the RTC to maintain representative real time, the crystal accuracy should be better than 20 ppm at 25ºC. This equates to 1.728 seconds of error per day.

5.4.5.2 Ethernet Clocks

Each Ethernet controller operates from a 25-MHz crystal. There are three Ethernet controllers on the board. To maintain adequate network timing performance, the crystal accuracy should be better than 20 ppm at 25ºC. Cypress Programmable clock generator CY2205 is used to generate 25-MHz Ethernet clocks and the 12-MHz STICK clock.

5.4.5.3 SAS Clock

The SAS controller requires a 40-MHz clock. This is provided using a crystal oscillator. The accuracy requirement for this clock is 25 ppm at 25ºC.

5.4.5.4 IPM Controller Clock

The BMR-H8S operates from a 7.3728-MHz crystal oscillator.

5.5 Power Requirements

The Netra CP3010 board is powered from dual-redundant –48V power supply inputs from the backplane power connector (P10). The Netra CP3010 board takes redundant –48V as input and derives the other necessary power using DC-DC converters. The Netra CP3010 board design complies with the ATCA power distribution specification and includes:

- Inrush current limiting
- Hot-plug capability
- Input under-voltage, over-voltage, and transient protection

- EMI filtering for conducted emissions
- Isolated management power
- External holdup and energy storage capacitors to meet 0 volts transient for 5 ms
- A/B Feed loss alarm

5.5.1 Fuses

As required by the PICMG 3.0 R1.0 specification, the Netra CP3010 board provides fuses on each of the –48V power feeds and on the return (RTN) connections. The fuses on the return feeds are critical to protect against overcurrent when an ORing diode in the return path fails. There are eight fuses on board and connections to –48V_A, –48V_B, RET_A, RET_B, EARLY_A, EARLY_B, ENABLE_A, and ENABLE_B power feeds. The fuses are single-blow type and must be replaced when blown.

5.5.2 ATCA Power Module (–48V to 12V)

The Netra CP3010 board uses the Artesyn ATCA power module solution. The Artesyn power module provides an integrated ATCA power solution that meets PICMG 3.0 requirements, including dual bus input, DC isolation, hold up, hot plug, and management power (3.3V standby). It provides a 12V intermediate bus as backend power. Some of the salient features of the module are:

- 210 watts output power.
- Input to output isolation.
- 12V with current rating of 17.5A.
- 3.3V standby at 1.82A. The IPMC draws power from IPMI Power (3.3V_STBY) so it can remain functional even if back-end logic is powered down.
- Isolated remote ON/OFF.
- Isolated “A” and “B” bus detect signals.
- High efficiency, typically 88 percent.
- Operating input voltage: –39V to –72V.
- Cutoff voltage: TBD
- Holdup time: TBD
- The I^2C interface monitors the status of fuse, input voltages, output voltages, and temperature and sends an alarm if any of the parameters are outside the programmable threshold.
- FRU information.

5.5.3 On-Board Voltage Converters

The Netra CP3010 board uses Point-of-Load Alliance (POLA) compatible power modules for generating other on-board power requirements. All the voltages are generated from +12V input power. TABLE 5-14 provides Sun part numbers and manufacturing part numbers.

TABLE 5-14 Part Numbers for Voltage Converters

Sun Part Number	Manufacturing Part Number	Access	Voltage
300-1703-01	PTH12020WAH	Through hole	3.3V
300-1722-01	PTH12060WAH	Through hole	1.5V, 5V
300-1723-01	PTH12050WAH	Through hole	2.5V (JBus-PCI ASIC PWR)
300-1765-01	PTH12060YAH	Through hole	1.25V
300-1730-01	PTH12030WAH	Through hole	2.5V (DDR PWR)

5.5.4 CPU Core Power

The UltraSPARC IIIi processor takes 1.2V for its internal core logic. An Artesyn Haymaker50 SIP module is used to generate CPU core power. The operating characteristics are:

- Output voltage is fixed at 1.2V. The voltage can be changed by adjusting the resistor values R6701 and R6801, which are connected to a trim pin on the converter.
- Input voltage: +12V.
- Output voltage: Fixed at 1.2V. Can be adjusted from 0.6V to 5V with an accuracy of plus or minus 2.5 percent.
- Maximum output current: 50A at 1.2V for one CPU.
- Efficiency: 94 percent at typical load.
- Provides “output power good” status.

5.5.4.1 DDR Memory Power

DDR memory requires 2.5V, which is also generated by POLA module PTH12030WAH. The operating characteristics are:

- Input voltage source: +12V
- Maximum output current: 26A at 2.5V
- Output ripple: 25 mVpp

- Efficiency: 94 percent at typical load

5.5.4.2 DTL I/O Power

All the DTL I/O power (1.5V) is generated using POLA module PTH12060WAH and delivered to CPUs and JBus-PCI ASICs for the DTL I/O. The operating characteristics are:

- Input voltage source: +12V
- Maximum output current: 10A
- Output ripple: 25 mVpp
- Efficiency: 95 percent at typical load

5.5.4.3 DDR Memory Termination Power (Vtt)

The PTH12060YAH POLA module is used to provide the termination voltage (1.25V) for all the DDR memory interface signals. It should be set to 1.25V output and should be tracking the DC variation of VDDQ. The operating characteristics are:

- Input voltage source: +12V
- Maximum output current: 10A
- Output ripple: 20 mVpp
- Output tracks the Vref (2.5V DDR voltage)
- Efficiency: 91 percent at typical load

5.5.4.4 JBus-PCI ASIC Power

The PTH12050WAH POLA module is used to provide the +2.5V power for the JBus-PCI ASIC core only. Both the JBus-PCI ASICs are powered from a single power converter. The operating characteristics are:

- Input voltage source: +12V
- Maximum output current: 6A
- Output ripple: 25 mVpp
- Efficiency: 91percent at typical load

5.5.4.5 Ethernet Controller Power

All the Ethernet controllers (Broadcom BCM5704C or BCM5704S) need 1.2V as core power, 2.5V analog supply voltage, and 3.3V for PCI. The 1.2V core power and 2.5V analog power are derived from 3.3V using a Broadcom built-in power converter.

5.5.4.6 SAS Controller Power

The SAS controller requires 1.2V core power. The LTC1772 is used to generate 1.2V core power for SAS. The output voltage is generated from 3.3V.

APPENDIX **A**

Physical Characteristics

Specifications for the Netra CP3010 board are provided in the following sections:

A.1 Form Factor

The Netra CP3010 board is a standard 8U form factor, a single slot wide, and complies with the board mechanical dimensions required by the PICMG 3.0 R1.0 Specification:

- 322.25 mm x 280 mm (length by width)
- 1.2-inch-wide front panel

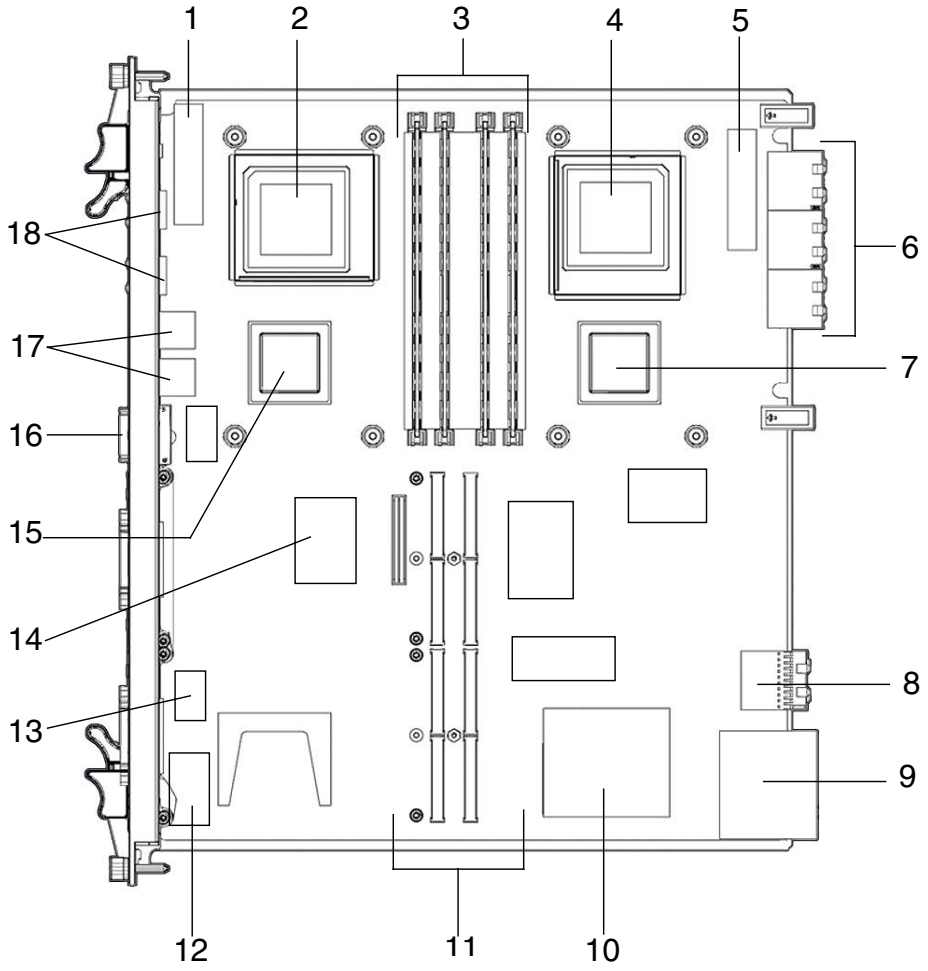
A.2 Thermal Management

A heat sink was designed for each UltraSPARC IIIi and JBus-PCI bridge pair. The heat sink is mechanically mounted to the Netra CP3010 board. The heat sink and DIMMs are positioned with respect to the overall board airflow (bottom to top).

A.3 Layout

The Netra CP3010 board layout is shown in FIGURE A-1.

FIGURE A-1 Netra CP3010 Board Layout



1 - CPU 0 power supply
2 - CPU 0 (master)
3 - DIMMs (x4)
4 - CPU 1 (slave)
5 - CPU 1 power supply
6 - Zone 3 connectors
7 - JBus-PCI bridge (slave)
8 - Zone 2 connector
9 - Zone 1 power connector
10 - Power module (-48 to 12V)
11 - PMC connectors
12 - H8
13 - CPLD
14 - SAS
15 - JBus-PCI bridge (master)
16 - SAS connector
17 - Ethernet ports
18 - Serial ports

A.4 Front Panel

The single-slot-wide, 8U front panel was designed to meet PICMG 3.0 R 1.0 and other specifications.

A.4.1 Visual Indicators

The Netra CP3010 board has the following indicators on the front panel:

- Green LED – Board's healthy status or user programmable (ACTIVE).
- Yellow LED – Board's fault condition (FAULT).
- Blue LED – Indicates safe removal (hot-swap activity).

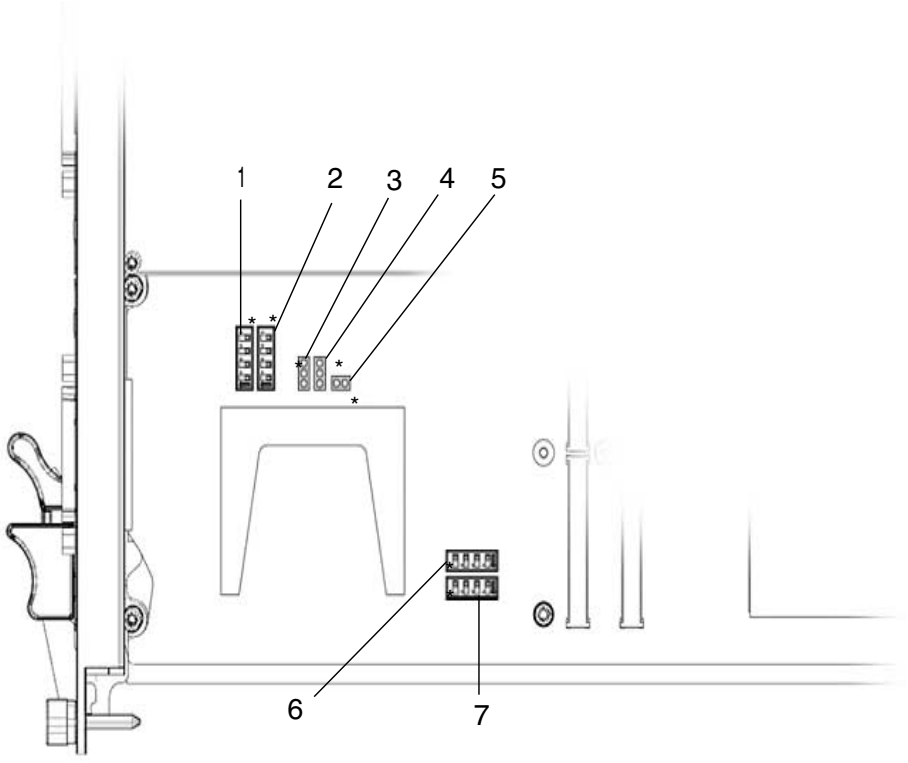
The front panel's Ethernet ports do not have LED indicators.

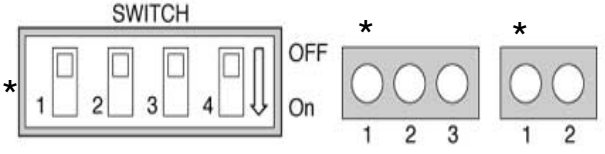
A.5 Switches and Jumpers

There are four switches, two three-pronged jumpers, and one two-prong jumper on the Netra CP3010 board assembly. They are located on the primary side of the printed circuit board (PCB) between the front panel and the PMC #1 connectors. See FIGURE A-2 for details.

Each switch has four positions: 1 to 4. Each position can be OFF or ON. Each jumper can be shorted (or jumped) to an adjacent pin. The star (*) on the PCB by the jumpers indicates pin 1 (see FIGURE A-2). TABLE A-1 shows the switches and TABLE A-2 jumpers for operation.

FIGURE A-2 Switches and Jumpers





1 - SW6101
2 - SW6001
3 - J2601
4 - J3301
5 - J3702
6 - SW3701
7 - SW3702

TABLE A-1 Switch Setting

	Position 1		Position 2		Position 3		Position 4	
Switch	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**
SW3701	Config bit no effect [default]	Config bit no effect	Config bit no effect [default]	Config bit no effect	Config bit no effect [default]	Config bit no effect	Config bit no effect [default]	Config bit no effect
SW3702	Config bit no effect [default]	Config bit no effect	Config bit no effect [default]	Config bit no effect	Not connected		Not connected	
SW6001	MD2* mode Bit2 =1	MD2* mode Bit2 =0 [default]	MD1 mode Bit1 =1 [default]	MD1 mode Bit1 =0	H8 Non-Maskable Interrupt NMI=1 (enabled) [default]	H8 Non-Maskable Interrupt NMI=0 (disabled)	H8 Flash Write Enable FWE=1 (enabled) [default]	H8 Flash Write Enable FWE=0 (disabled)
SW6101	Bootpage bit 0 =1	Bootpage bit 0 =0 [default]	Bootpage bit 1 =1	Bootpage bit 1 =0 [default]	Serial hardware flow control OFF	Serial hardware flow control ON [default]	H8 controls power on (stand-alone)	Hardware controls power on (in chassis) [default]

Note – The MD2*, MD1, NMI, and FWE defaults set the H8 to mode 2, User Programming mode.

TABLE A-2 Jumper Settings

Jumper	Open	Short Pin 1 to Pin 2	Short Pin 2 to Pin 3
J2601	Normal operation [default]	Force power-on reset	Force XIR reset
J3301	Do not use	Normal operation [default]	Clear Real-Time_Clock
J3702	Write protect SUN FRU ID [default]	Enable write of SUN FRU ID	N/A

A.6 Connectors and Pinout

FIGURE A-1 shows all the basic I/O connectors to the front and the rear of the Netra CP3010 board. Also shown is the placement of the PMC connectors.

A.6.1 Front Panel Connectors

The front panel has the following connectors:

- Two 10/100BASE-T Ethernet ports (RJ-45)
- Two serial ports (SubDB-9)
- One 4X SAS port (supports only two SAS channels)

A.6.1.1 Ethernet Ports

The Ethernet connectors are RJ-45 connectors. The controller autonegotiates to either 10BASE-T or 100BASE-T. The Ethernet connector pin numbering is shown in FIGURE A-3.

FIGURE A-3 Ethernet RJ-45 Connector

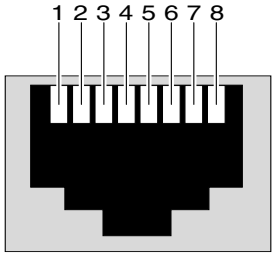


TABLE A-3 shows the Ethernet connector pin assignments.

TABLE A-3 Ethernet Port Connector Pin Assignments

Pin	Signal Name	Pin	Signal Name
1	TXD+	5	Not used
2	TXD–	6	RXD–
3	RXD+	7	Not used
4	Not Used	8	Not used

A.6.1.2 Serial Ports

FIGURE A-4 contains the connector pin assignments for the front panel serial port.

FIGURE A-4 Front Panel Serial Port Diagram

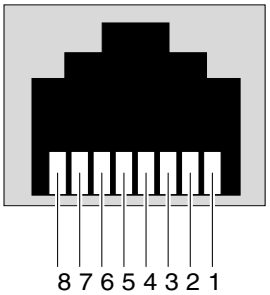


TABLE A-4 shows the serial port connector pin assignments.

TABLE A-4 Serial Port Mini Din 8-pin Connector Pinouts

Pin	Signal Name	Pin	Signal Name
1	RTS	5	DCD
2	DTR	6	RXD
3	TXD	7	DSR
4	GND	8	CTS

A.6.1.3 SAS Port

The Netra CP3010 board provides a Serial Attached SCSI (SAS) port using a standard 4x SAS port connector. Only two SAS channels are routed to the 4x port connector. The SAS access is through both the front panel and the rear; the rear access requires the RTM.

A.6.2 PMC Connectors

There are four 64-pin connectors that make up the PMC card connection. These connectors and pinouts are defined by the following industry-standard specifications:

- Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC IEEE (MMSC) P1386.1/Draft 2.3, October 9, 2000
- Draft Standard for a Common Mezzanine Card Family: CMC IEEE (MMSC) P1386/Draft 2.3, October 9, 2000

The PMC slots are available on the front panel. The PMC I/O transactions are passed to the RTM and are available using PIM cards and cables.

A.6.3 Midplane Power Connector (Zone 1)

The Netra CP3010 board uses a 34-pin Positronic connector as the Zone 1 power connector. It provides support for the following signals:

- Two –48 volt DC power feeds (four signals each; eight signals total)
- Two IPMB ports (two signals each, four signals total)
- Geographic address (eight signals)

The analog test and ring voltage pins are left unconnected.

FIGURE A-5 shows the pin assignments.

FIGURE A-5 Power Distribution Connector (Zone 1) P10

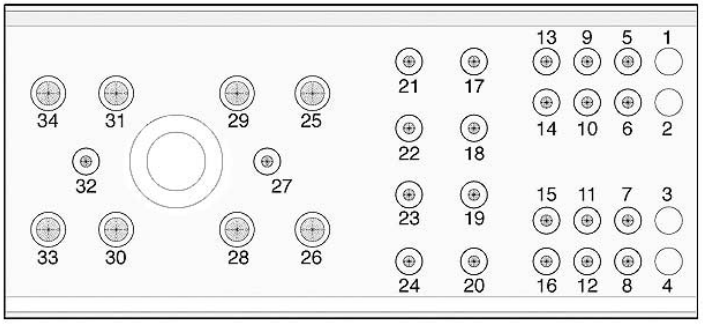


TABLE A-5 lists the power connector pin assignments.

TABLE A-5 Zone 1 Power Distribution Connector Pin Assignments

Pin Number	Name	Description
1	Reserved	Reserved
2	Reserved	Reserved
3	Reserved	Reserved
4	Reserved	Reserved
5	HA0	HA0 Hardware Address Bit 0
6	HA1	HA1 Hardware Address Bit 1
7	HA2	HA2 Hardware Address Bit 2
8	HA3	HA3 Hardware Address Bit 3
9	HA4	HA4 Hardware Address Bit 4
10	HA5	HA5 Hardware Address Bit 5
11	HA6	HA6 Hardware Address Bit 6
12	HA7/P	HA7/P Hardware Address Bit 7(Odd Parity Bit)
13	SCL_A	IPMB Clock, Port A
14	SDA_A	IPMB Data, Port A
15	SCL_B	IPMB Clock, Port B
16	SDA_B	IPMB Data, Port B
17	Unused	
18	Unused	

TABLE A-5 Zone 1 Power Distribution Connector Pin Assignments *(Continued)*

Pin Number	Name	Description
19	Unused	
20	Unused	
21	Unused	
22	Unused	
23	Unused	
24	Unused	
25	SHELF_GND	Shelf Ground
26	LOGIC_GND	Logic Ground
27	ENABLE_B	Enable B
28	VRTN_A	Voltage Return A
29	VRTN_B	Voltage Return B
30	EARLY_A	–48V Early A
31	EARLY_B	–48V Early B
32	ENABLE_A	Enable A
33	–48V_A	–48V A
34	–48V_B	–48V B

A.6.4 Data Transport Connector (Zone 2)

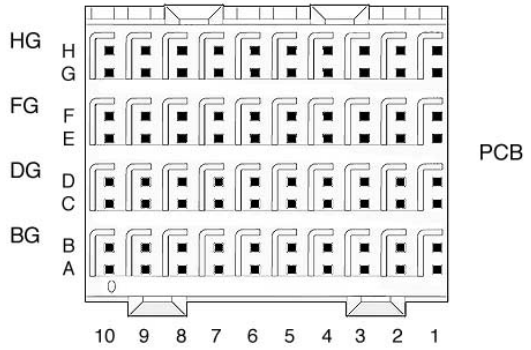
The data transport connector consists of one 120-pin HM-Zd connector, labeled P23, with 40 differential pairs. This is called the Zone 2 connector.

The Zone 2 connector provides the following signals:

- Two 10/100/1000BASE-T/TX Ethernet Base Fabric channels (four differential signal pairs each, 16 signals total)
- Two 2-Gb SERDES ports on the Extended Fabric interface (2 differential signal pairs each, 8 signals total)

The connector vendor part number is Tyco: 1469001-1. FIGURE A-6 shows the Zone 2 connector.

FIGURE A-6 Zone 2 Connector



A.6.5 RTM Connector (Zone 3)

The Netra CP3010 board provides all the I/O connections for rear access through the Zone 3 RTM connector. The connector view and the pinout for the Zone 3 connectors is shown in FIGURE A-7.

FIGURE A-7 Zone 3 Connectors

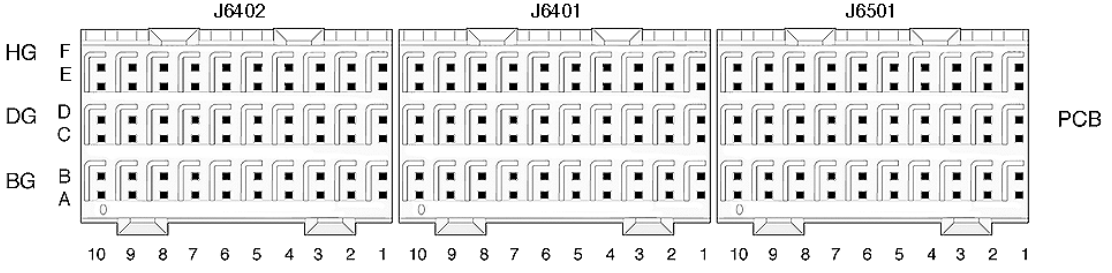


TABLE A-6 gives the Zone 3 J6402 connector pin assignments.

TABLE A-6 Zone 3 J6402 Connector Pin Assignments

Row	A	B	BG	C	D	DG	E	F	FG
1	PMC1_IO1	PMC1_IO2		PMC1_IO3	PMC1_IO4		PMC1_IO5	PMC1_IO6	GND
2	PMC1_IO7	PMC1_IO8		PMC1_IO9	PMC1_IO10		PMC1_IO11	PMC1_IO12	
3	PMC1_IO13	PMC1_IO14		PMC1_IO15	PMC1_IO16		PMC1_IO17	PMC1_IO18	
4	PMC1_IO19	PMC1_IO20		PMC1_IO21	PMC1_IO22		PMC1_IO23	PMC1_IO24	
5	PMC1_IO25	PMC1_IO26		PMC1_IO27	PMC1_IO28		PMC1_IO29	PMC1_IO30	
6	PMC1_IO31	PMC1_IO32		PMC1_IO33	PMC1_IO34		PMC1_IO35	PMC1_IO36	GND
7	PMC1_IO37	PMC1_IO38		PMC1_IO39	PMC1_IO40		PMC1_IO41	PMC1_IO42	
8	PMC1_IO43	PMC1_IO44		PMC1_IO45	PMC1_IO46		PMC1_IO47	PMC1_IO48	
9	PMC1_IO49	PMC1_IO50		PMC1_IO51	PMC1_IO52		PMC1_IO53	PMC1_IO54	
10	PMC1_IO55	PMC1_IO56		PMC1_IO57	PMC1_IO58		PMC1_IO59	PMC1_IO60	

TABLE A-7 gives the Zone 3 J6401 connector pin assignments.

TABLE A-7 Zone 3 J6401 Connector Pin Assignments

Row	A	B	BG	C	D	DG	E	F	FG
1	PMC0_IO1	PMC0_IO2		PMC0_IO3	PMC0_IO4		PMC0_IO5	PMC0_IO6	GND
2	PMC0_IO7	PMC0_IO8		PMC0_IO9	PMC0_IO10		PMC0_IO11	PMC0_IO12	
3	PMC0_IO24	PMC0_IO23		PMC0_IO22	PMC0_IO21		PMC0_IO20	PMC0_IO19	
4	PMC0_IO18	PMC0_IO17		PMC0_IO16	PMC0_IO15	GND	PMC0_IO14	PMC0_IO13	
5	PMC0_IO36	PMC0_IO35	GND	PMC0_IO34	PMC0_IO33		PMC0_IO32	PMC0_IO31	
6	PMC0_IO30	PMC0_IO29		PMC0_IO28	PMC0_IO27		PMC0_IO26	PMC0_IO25	
7	PMC0_IO48	PMC0_IO47		PMC0_IO46	PMC0_IO45	GND	PMC0_IO44	PMC0_IO43	
8	PMC0_IO42	PMC0_IO41		PMC0_IO40	PMC0_IO39		PMC0_IO38	PMC0_IO37	
9	PMC0_IO49	PMC0_IO50		PMC0_IO51	PMC0_IO52		PMC0_IO53	PMC0_IO54	
10	PMC0_IO55	PMC0_IO56		PMC0_IO57	PMC0_IO58		PMC0_IO59	PMC0_IO60	

TABLE A-8 gives the Zone 3 J6501 connector pin assignments.

TABLE A-8 Zone 3 J6501 Connector Pin Assignments

Row	A	B	BG	C	D	DG	E	F	FG
1	PMC0_IO61	PMC1_IO2		PMC0_IO63	PMC0_IO64			–12V	
2	PMC1_IO61	PMC1_IO8	5V	PMC1_IO63	PMC1_IO64	5V	+12V	+12V	5V
3	RTM_SER1_CTS	PMC1_IO14	3.3V	RTM_SER1_DCD	RTM_SER1_DSR	3.3V	RTM_SER1_RXD	RTM_SER1_TXD	3.3V
4	RTM_SER1_RTS	PMC1_IO20	3.3V	RTM_SER2_CTS	RTM_SER2_DTR	3.3V	RTM_SER2_DCD	RTM_SER2_DSR	3.3V
5	RTM_SER2_RXD	PMC1_IO26	5V	RTM_SER2_RTS		5V			5V
6	RTM_HDD2_RX_P	PMC1_IO32	GND			GND	RTM_HDD2_TX_N	RTM_HDD2_TX_P	GND
7	RTM_PRSNT_N	PMC1_IO38	GND	SYS_I2C_SDA	SYS_I2C_SCL	GND	3V_STBY	3V_STBY	GND
8	RTM_HDD3_RX_P	PMC1_IO44	GND			GND	RTM_HDD3_TX_N	RTM_HDD3_TX_P	GND
9	RTM_TXD_1P	PMC1_IO50	GND	2.5V	2.5V	GND	RTM_RXD_1P	RTM_RXD_1N	GND
10	RTM_TXD_0P	PMC1_IO56	GND	2.5V	2.5V	GND	RTM_RXD_0P	RTM_RXD_0N	GND

APPENDIX **B**

Sun OEM IPMI Commands

This appendix contains the following sections:

The commands described in this appendix are specific to ATCA node boards designed by Sun Microsystems. The Internet Assigned Numbers Authority (IANA) number assigned to Sun Microsystems is 42.

Refer to `http://www.iana.org/assignments/enterprise-numbers` for more information about IANA number assignments.

The netfunction (NetFn) used for these commands is 0x2E, which is the OEM netfunction as defined in the IPMI specification. For this netfunction, the first three data bytes in the request packet must be this IANA number and the first three bytes in the response packet following the completion code are the IANA number. For Sun ATCA node boards, these three bytes are `00 00 2A`.

The Sun OEM IPMI commands are listed in TABLE B-1 and described in the following sections.

TABLE B-1 Sun OEM IPMI Commands

Command	Opcode	Syntax
`Get Version`	0x80	`#GET_VERSION`
`Set Boot Page`†	0x81	`#SET_BOOT_PAGE`
`Get Boot Page`†	0x82	`#GET_BOOT_PAGE`
`Set Front panel reset button state`	0x83	`#SET_FP_RESET_BUTTON`
`Get Front panel reset button state`	0x84	`#GET_FP_RESET_BUTTON_STATE`
`Set Ethernet Force Front bit`	0x85	`#SET_ETH_FORCE_FRONT`
`Get Ethernet Force Front bit`	0x86	`#GET_ETH_FORCE_FRONT`
`Get RTM status`	0x88	`#GET_RTM_STATUS`

† Valid for the Netra CP3010 board only

B.1 `Get Version` Command

`Get Version` returns the IPM controller (IPMC) firmware version and Standby CPLD version. Bytes 8, 9, and A are reserved for future use.

Command	NetFn	Opcode	Reference
`Get Version`	0x2E (OEM)	0x80	- -

Data Bytes

Type	Byte	Data Field
Request data	Byte1	00
	Byte2	00
	Byte3	2A

Type	Byte	Data Field
Response data	Byte1	Completion code: 00 = OK C1 = Command not supported CC = Invalid data in request (Refer to IPMI specification for more completion codes)
	Byte2	00
	Byte3	00
	Byte4	2A
	Byte5	CPLD version
	Byte6	REV1 byte of IPMC firmware
	Byte7	REV2 byte of IPMC firmware
	Byte8	Reserved for future use (ignore)
	Byte9	Reserved for future use (ignore)
	ByteA	Reserved for future use (ignore)

Example (Terminal Mode):

```
[B8 00 80 00 00 2A] <-------Request
[BC 00 80 00 00 00 2A 02 02 00 00 00 00] <----Response
```

- The IPMC version is read as the following:

  lower nibble of REV1 . high nibble of REV2 . low nibble of REV2

  In the preceding example, the IPMC version is `2.0.0.`

- The CPLD version is read as:

  -> lower nibble of CPLD version byte

  In the example, the CPLD version is `2.`

B.2 `Set Boot Page` Command

`Set Boot Page` sets the boot page bits in the standby CPLD to select the boot page for the Open Boot PROM. This feature can be used in boot Flash failure recovery. This command is valid only for the Netra CP3010 node board.

Command	NetFn	Opcode	Reference
`Set Boot Page`	0x2E (OEM)	0x81	CPLD Specification 1.0

Data Bytes

Type	Byte	Data Field
Request data	Byte1	00
	Byte2	00
	Byte3	2A
	Byte4	Boot page setting. Bits 7 to 2 = 0 Bits 1 and 0 = Boot page number
Response data	Byte1	Completion code: 00 = OK C1 = Command not supported CC = Invalid data in request (Refer to IPMI specification for more completion codes)
	Byte2	00
	Byte3	00
	Byte4	2A

Example (Terminal Mode):

```
[B8 00 81 00 00 2A 02] <------Request
[BC 00 81 00 00 00 2A] <------Response
```

B.3 `Get Boot Page` Command

`Get Boot Page` returns current settings of the selected OpenBoot PROM boot page and the current settings of the hardware switch selecting the boot page. This command is valid only for the Netra CP3010 node board.

Command	NetFn	Opcode	Reference
`Get Boot Page`	0x2E (OEM)	0x82	--

Data Bytes

Type	Byte	Data Field
Request data	Byte1	00
	Byte2	00
	Byte3	2A
Response data	Byte1	Completion code: 00 = OK C1 = Command not supported CC = Invalid data in request (Refer to IPMI specification for more completion codes)
	Byte2	00
	Byte3	00
	Byte4	2A
	Byte5	Boot Page Settings Bit 7 to 4 = Ignore. Shall be zeros Bit 3, 2 = Hardware switch settings Bit 1, 0 = Currently set boot page

Example (Terminal Mode):

```
[B8 00 82 00 00 2A] <------Request
[BC 00 82 00 00 00 2A  02] <------Response
```

B.4 Set Front Panel Reset Button State Command

Set Front panel reset button state is used by the software to change the way the front panel reset is handled by CPLD when this button is pressed. Default on CPLD power up is 10.

Command	NetFn	Opcode	Reference
Set Front panel reset button state	0x2E (OEM)	0x83	CPLD Specification 1.0

Data Bytes

Type	Byte	Data Field
Request data	Byte1	00
	Byte2	00
	Byte3	2A
	Byte4	Front panel reset button setting. Bits 7 to 2 = 0 Bits 1 and 0 = Front panel button state: 00 = Reset IPMC and assert POR to CPU 01 = XIR to CPU 10 = POR to CPU 11 = Front panel reset button disabled
Response data	Byte1	Completion code: 00 = OK C1 = Command not supported CC = Invalid data in request (Refer to IPMI specification for more completion codes)
	Byte2	00
	Byte3	00
	Byte4	2A

Example (Terminal Mode):

```
[B8 00 83 00 00 2A 02] <------Request
[BC 00 83 00 00 00 2A] <------Response
```

B.5 Get Front Panel Reset Button State Command

`Get Front panel reset button state` returns current settings of the front panel reset button handling. By default, on CPLD power-on it comes up as 10, that is, pressing this button causes a Power-on reset to the CPU.

Command	NetFn	Opcode	Reference
`Get Front panel reset button state`	0x2E (OEM)	0x84	CPLD Specification 1.0

Data Bytes

Type	Byte	Data Field
Request data	Byte1	00
	Byte2	00
	Byte3	2A

Type	Byte	Data Field
Response data	Byte1	Completion code: 00 = OK C1 = Command not supported CC = Invalid data in request (Refer to IPMI specification for more completion codes)
	Byte2	00
	Byte3	00
	Byte4	2A
	Byte5	Front panel reset button setting. Bits 7 to 2 = Zeros. Bits 1 and 0 = Front panel button state: 00 = Reset IPMC and assert POR to CPU 01 = XIR to CPU 10 = POR to CPU 11 = Front panel reset button disabled

Example (Terminal Mode):

```
[B8 00 84 00 00 2A] <------Request
[BC 00 84 00 00 00 2A 02] <------Response
```

B.6 Set Ethernet Force Front Bit Command

Set Ethernet Force Front Bit is used by software to force the Ethernet connection to the front I/O panel even if the rear transition card is present in the system. Setting this bit to 1 forces the Ethernet connection to front I/O panel.

Command	NetFn	Opcode	Reference
Set Ethernet Force Front Bit	0x2E (OEM)	0x85	CPLD Specification 1.0

Data Bytes

Type	Byte	Data Field
Request data	Byte1	00
	Byte2	00
	Byte3	2A
	Byte4	Ethernet Force front bit setting Bits 7 to 1 = 0 Bits 0 = Force front state (1 = Force Ethernet connection to front)
Response data	Byte1	Completion code: 00 = OK C1 = Command not supported CC = Invalid data in request (Refer to IPMI specification for more completion codes)
	Byte2	00
	Byte3	00
	Byte4	2A

Example (Terminal Mode):

```
[B8 00 85 00 00 2A 01] <------Request
[BC 00 85 00 00 00 2A] <------Response
```

B.7 Get Ethernet Force Front Bit Command

Get Ethernet Force Front Bit returns the current setting of the Ethernet force front bit.

Command	NetFn	Opcode	Reference
Get Ethernet Force Front Bit	0x2E (OEM)	0x86	CPLD Specification 1.0

Data Bytes

Type	Byte	Data Field
Request data	Byte1	00
	Byte2	00
	Byte3	2A
Response data	Byte1	Completion code: 00 = OK C1 = Command not supported CC = Invalid data in request (Refer to IPMI specification for more completion codes)
	Byte2	00
	Byte3	00
	Byte4	2A
	Byte5	Ethernet Force front bit setting Bits 7 to 1 = 0 Bits 0 = Ethernet force front bit setting (1 = Force Ethernet connection to front)

Example (Terminal Mode):

```
[B8 00 86 00 00 2A] <------Request
[BC 00 86 00 00 00 2A 01] <------Response
```

B.8 `Get RTM Status` Command

`Get RTM Status` can be used to detect the presence of a rear transition module (RTM) in the system.

Command	NetFn	Opcode	Reference
`Get RTM Status`	0x2E (OEM)	0x88	CPLD Specification

Data Bytes

Type	Byte	Data Field
Request data	Byte1	00
	Byte2	00
	Byte3	2A
Response data	Byte1	Completion code: 00 = OK C1 = Command not supported CC = Invalid data in request
	Byte2	00
	Byte3	00
	Byte4	2A
	Byte5	RTM presence Bits 7 to 1 = 0 Bits 0 = RTM presence (0 = RTM not detected, 1 = RTM detected)

Example (Terminal Mode):

```
[B8 00 88 00 00 2A] <------Request
[BC 00 88 00 00 00 2A 01] <------Response
```

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