Oracle® Database Appliance Licensing Information User Manual





Oracle Database Appliance Licensing Information User Manual, Release 19.24

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Preface

This document, which is part of the Program Documentation under the terms of your Oracle licensing agreement, is intended to help you understand the features, functionality, and options available for Oracle Programs.

If you have a question about your licensing needs, then contact your Oracle sales representative or the License Management Services representative at http://www.oracle.com/us/corporate/license-management-services/index.html. You can also refer to the resources listed in "Related Documents" for more information.

- Audience
- Documentation Accessibility
- Related Documents
- Conventions

Audience

This book is intended for all purchasers of Oracle Database Appliance.

Documentation Accessibility

For information about Oracle's commitment to accessibility, visit the Oracle Accessibility Program website at http://www.oracle.com/pls/topic/lookup?ctx=acc&id=docacc.

Access to Oracle Support

Oracle customers that have purchased support have access to electronic support through My Oracle Support. For information, visit http://www.oracle.com/pls/topic/lookup?ctx=acc&id=info or visit http://www.oracle.com/pls/topic/lookup?ctx=acc&id=trs if you are hearing impaired.

Related Documents

For more information about Oracle Database Appliance, go to http://www.oracle.com/goto/oda/docs and click the appropriate release.

For more information about using Oracle Database, go to http://docs.oracle.com/database/ and select the database release from the menu.

For more information about Oracle Integrated Lights Out Manager 3.2, see https://docs.oracle.com/cd/E37444_01/.

For more details about other Oracle products that are mentioned in Oracle Database Appliance documentation, see the Oracle Documentation home page at http://docs.oracle.com.

Conventions

The following text conventions are used in this document:

Convention	Meaning
boldface	Boldface type indicates graphical user interface elements associated with an action, or terms defined in text or the glossary.
italic	Italic type indicates book titles, emphasis, or placeholder variables for which you supply particular values.
monospace	Monospace type indicates commands within a paragraph, URLs, code in examples, text that appears on the screen, or text that you enter.



1

Introduction

This Licensing Information document is a part of the product or program documentation under the terms of your Oracle license agreement and is intended to help you understand the program editions, entitlements, restrictions, prerequisites, special license rights, and/or separately licensed third party technology terms associated with the Oracle software program(s) covered by this document (the "Program(s)").

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2

Oracle Database Appliance Licensing Overview

This chapter provides an overview of the licensing process for each hardware platform.

Topics:

- About Licensing
 Oracle Database Appliance provides capacity-on-demand licensing.
- CPUs and Core Count
 Review this section for information about core license options for your Oracle Database
 Appliance hardware.
- Oracle Database Appliance KVM Hard Partitioning Compliance
 Review this section for information about Oracle Database Appliance KVM Hard Partitioning compliance.

About Licensing

Oracle Database Appliance provides capacity-on-demand licensing.

Capacity-on-demand (CoD) refers to an Oracle Database Appliance server that has a subset of its cores turned off so that the Oracle Database Enterprise Edition or Oracle Database Standard Edition 2 software license cost can be reduced. The number of cores can be reduced before or after the deployment. The number of active cores can be increased at a later time, when more capacity is needed. Oracle Database is licensed separately. Refer to Database Licensing Information User Manual for additional information.

When you add your hardware Support Identifier (SI) for Oracle Database Appliance to your My Oracle Support account, you establish a license for all the cores on your system. Oracle Database Appliance models can be deployed as bare metal systems or KVM-based virtualized systems. Both platform types offer capacity-on-demand licensing.

With bare-metal installations, you disable cores that you do not intend Oracle Database to use:

For Oracle Database Appliance X10, X9-2S, X9-2L, X9-2-HA, X8-2S, X8-2M, X8-2-HA, X7-2S, X7-2M, X7-2-HA: Issue the command odacli modify-cpucore to set the low water mark and to increase the cores.

Chapter three explains how to obtain a licensing key and record your initial license requirements with My Oracle Support. It also explains how to change the licensed core count, if necessary, later. Chapter three is appropriate for bare metal installations where your license covers the cores that you are using for Oracle Database.

Chapter four contains information about the third-party products that are included with Oracle Database Appliance.

If you use the Integrated Oracle Data Guard feature only, then you **do not** require a separate Oracle Active Data Guard license.

About License Options for Oracle Database Standard Edition 2 on Oracle Database Appliance

For the purposes of licensing Oracle Database Standard Edition 2 on Oracle Database Appliance running multi-chip modules, where each chip in a multi-chip module is counted as an occupied socket for licensing purposes, you may exceed the 2 sockets per server limit. Oracle Database Standard Edition 2 requires one processor license for every 8 enabled cores on Oracle Database Appliance running multi-chip modules. If the number of enabled cores is not divisible by 8, the quotient must be rounded up to the nearest whole number to determine the number of Oracle Database Standard Edition 2 processor licenses required.



The minimum licenses when licensing by SE2 Named User Plus (NUP) metric are 10 NUP licenses per server.

CPUs and Core Count

Review this section for information about core license options for your Oracle Database Appliance hardware.

- Oracle Database Appliance X10-HA has 2 servers, each with 2 CPUs of 32 cores each.
 When you deploy Oracle Database Appliance X10-HA, all 128 cores (64 cores in each server) are active with hyper-threading enabled by default.
- Oracle Database Appliance X10-L contains 2 CPUs with 32 cores for a total of 64 cores.
 When you deploy Oracle Database Appliance X10-L, all 64 cores are active with hyperthreading enabled by default.
- Oracle Database Appliance X10-S contains 1 CPU with 32 cores. When you deploy Oracle
 Database Appliance X10-S, all 32 cores are active with hyper-threading enabled by
 default.
- Oracle Database Appliance X9-2-HA has 2 servers, each with 2 CPUs of 16 cores each.
 When you deploy Oracle Database Appliance X9-2-HA, all 64 cores (32 cores in each server) are active with hyper-threading enabled by default.
- Oracle Database Appliance X9-2L contains 2 CPUs with 16 cores for a total of 32 cores.
 When you deploy Oracle Database Appliance X9-2L, all 32 cores are active with hyperthreading enabled by default.
- Oracle Database Appliance X9-2S contains 1 CPU with 16 cores. When you deploy Oracle
 Database Appliance X9-2S, all 16 cores are active with hyper-threading enabled by
 default.
- Oracle Database Appliance X8-2-HA has 2 servers, each with 2 CPUs of 16 cores each.
 When you deploy Oracle Database Appliance X8-2-HA, all 64 cores (32 cores in each server) are active with hyper-threading enabled by default.



- Oracle Database Appliance X8-2M contains 2 CPUs with 16 cores for a total of 32 cores.
 When you deploy Oracle Database Appliance X8-2M, all 32 cores are active with hyperthreading enabled by default.
- Oracle Database Appliance X8-2S contains 1 CPU with 16 cores. When you deploy Oracle
 Database Appliance X8-2S, all 16 cores are active with hyper-threading enabled by
 default.
- Oracle Database Appliance X7-2-HA has 2 servers, each with 2 CPUs of 18 cores each.
 When you deploy Oracle Database Appliance X7-2-HA, all 72 cores (36 cores in each server) are active with hyper-threading enabled by default.
- Oracle Database Appliance X7-2M contains 2 CPUs with 18 cores for a total of 36 cores.
 When you deploy Oracle Database Appliance X7-2M, all 36 cores are active with hyperthreading enabled by default.
- Oracle Database Appliance X7-2S contains 1 CPU with 10 cores. When you deploy Oracle
 Database Appliance X7-2S, all 10 cores are active with hyper-threading enabled by
 default.

Oracle Database Appliance bare metal licensing is determined by the number of enabled cores that you have on your system. The capacity-on-demand licensing feature enables you to change the enabled core count as your system resource needs change.

Initialize the number of licensed cores to the level currently required by your applications. Each server node has the same number of active cores. Later, increase the licensed core count as your applications require more capacity. Change the number of licensed cores by obtaining and applying a core key to configure your appliance, using the tables for your Oracle Database Appliance platform.

Oracle Database Appliance X10-HA Licensed Core Licensing Options

The table provides an example of how the licensed cores for each node of an Oracle Database Appliance X10-HA relate to active cores for Oracle RAC and Oracle Enterprise Edition and active cores for Oracle RAC One Node.

Table 2-1 Example of Bare Metal License Options for Oracle Database Appliance X10-HA Systems

Licensed Cores for Each Node (X10-HA Only)	Active Cores for Oracle RAC and Oracle Enterprise Edition (X10-HA Only)	Active Cores for Oracle RAC One Node (X10-HA Only)
2	4	2
4	8	4
6	12	6
8	16	8
10	20	10
12	24	12
14	28	14
16	32	16
18	36	18
20	40	20
22	44	22
24	48	24



Table 2-1 (Cont.) Example of Bare Metal License Options for Oracle Database Appliance X10-HA Systems

Licensed Cores for Each Node (X10-HA Only)	Active Cores for Oracle RAC and Oracle Enterprise Edition (X10-HA Only)	Active Cores for Oracle RAC One Node (X10-HA Only)
26	52	26
28	56	28
30	60	30
32	64	32

Oracle Database Appliance X10-L and X10-S Licensed Core Licensing Options

Table 2-2 Bare Metal License Options for all Oracle Database Appliance X10-L and X10-S Systems

Licensed Cores for Single Node (X10-S)	Licensed Cores for Single Node (X10-L)
2	2
4	4
6	6
8	8
10	10
12	12
14	14
16	16
Not applicable	18
Not applicable	20
Not applicable	22
Not applicable	24
Not applicable	26
Not applicable	28
Not applicable	30
Not applicable	32

Oracle Database Appliance X9-2-HA Licensed Core Licensing Options

The table provides an example of how the licensed cores for each node of an Oracle Database Appliance X9-2-HA relate to active cores for Oracle RAC and Oracle Enterprise Edition and active cores for Oracle RAC One Node.

Table 2-3 Example of Bare Metal License Options for Oracle Database Appliance X9-2-HA Systems

Licensed Cores for Each Node (X9-2-HA Only)	Active Cores for Oracle RAC and Oracle Enterprise Edition (X9-2-HA Only)	Active Cores for Oracle RAC One Node (X9-2-HA Only)
2	4	2
4	8	4
6	12	6
8	16	8
10	20	10
12	24	12
14	28	14
16	32	16
18	36	18
20	40	20
22	44	22
24	48	24
26	52	26
28	56	28
30	60	30
32	64	32

Oracle Database Appliance X9-2L and X9-2S Licensed Core Licensing Options

Table 2-4 Bare Metal License Options for all Oracle Database Appliance X9-2L and X9-2S Systems

Licensed Cores for Single Node (X9-2S)	Licensed Cores for Single Node (X9-2L)
2	2
4	4
6	6
8	8
10	10
12	12
14	14
16	16
Not applicable	18
Not applicable	20
Not applicable	22
Not applicable	24
Not applicable	26
Not applicable	28
Not applicable	30

Table 2-4 (Cont.) Bare Metal License Options for all Oracle Database Appliance X9-2L and X9-2S Systems

Licensed Cores for Single Node (X9-2S)	Licensed Cores for Single Node (X9-2L)
Not applicable	32

Oracle Database Appliance X8-2-HA Licensed Core Licensing Options

The table provides an example of how the licensed cores for each node of an Oracle Database Appliance X8-2-HA relate to active cores for Oracle RAC and Oracle Enterprise Edition and active cores for Oracle RAC One Node.

Table 2-5 Example of Bare Metal License Options for Oracle Database Appliance X8-2-HA Systems

Licensed Cores for Each Node (X8-2-HA Only)	Active Cores for Oracle RAC and Oracle Enterprise Edition (X8-2-HA Only)	Active Cores for Oracle RAC One Node (X8-2-HA Only)
2	4	2
4	8	4
6	12	6
8	16	8
10	20	10
12	24	12
14	28	14
16	32	16
18	36	18
20	40	20
22	44	22
24	48	24
26	52	26
28	56	28
30	60	30
32	64	32

Oracle Database Appliance X8-2M and X8-2S Licensed Core Licensing Options

Table 2-6 Bare Metal License Options for all Oracle Database Appliance X8-2M and X8-2S Systems

Licensed Cores for Single Node (X8-2S)	Licensed Cores for Single Node (X8-2M)
2	2
4	4
6	6
8	8
10	10



Table 2-6 (Cont.) Bare Metal License Options for all Oracle Database Appliance X8-2M and X8-2S Systems

Licensed Cores for Single Node (X8-2S)	Licensed Cores for Single Node (X8-2M)
12	12
14	14
16	16
Not applicable	18
Not applicable	20
Not applicable	22
Not applicable	24
Not applicable	26
Not applicable	28
Not applicable	30
Not applicable	32

Oracle Database Appliance X7-2-HA Licensed Core Licensing Options

The table provides an example of how the licensed cores for each node of an Oracle Database Appliance X7-2-HA relate to active cores for Oracle RAC and Oracle Enterprise Edition and active cores for Oracle RAC One Node.

Table 2-7 Example of Bare Metal License Options for Oracle Database Appliance X7-2-HA Systems

Licensed Cores for Each Node (X7-2-HA Only)	Active Cores for Oracle RAC and Oracle Enterprise Edition (X7-2-HA Only)	Active Cores for Oracle RAC One Node (X7-2-HA Only)
2	4	2
4	8	4
6	12	6
8	16	8
10	20	10
12	24	12
14	28	14
16	32	16
18	36	18
20	40	20
22	44	22
24	48	24
26	52	26
28	56	28
30	60	30
32	64	32
34	68	34



Table 2-7 (Cont.) Example of Bare Metal License Options for Oracle Database Appliance X7-2-HA Systems

Licensed Cores for Each Node (X7-2-HA Only)	Active Cores for Oracle RAC and Oracle Enterprise Edition (X7-2-HA Only)	Active Cores for Oracle RAC One Node (X7-2-HA Only)
36	72	36

Oracle Database Appliance X7-2 Licensed Core Licensing Options

Table 2-8 Bare Metal License Options for all Oracle Database Appliance X7-2 Systems

Licensed Cores for Single Node (X7-2S)	Licensed Cores for Single Node (X7-2M)
2	2
4	4
6	6
8	8
10	10
Not applicable	12
Not applicable	14
Not applicable	16
Not applicable	18
Not applicable	20
Not applicable	22
Not applicable	24
Not applicable	26
Not applicable	28
Not applicable	30
Not applicable	32
Not applicable	34
Not applicable	36

Oracle Database Appliance KVM Hard Partitioning Compliance

Review this section for information about Oracle Database Appliance KVM Hard Partitioning compliance.

Oracle Database Appliance DB systems and application KVMs conform to Oracle Linux KVM Hard Partitioning requirements as specified in Hard Partitioning with Oracle Linux KVM:

https://www.oracle.com/a/ocom/docs/linux/ol-kvm-hard-partitioning.pdf

Considerations for CPU Pool Subscription

CPU Pools are used for management of CPU resources only. Database license requirements are determined by KVM Hard Partitioning only.



In a DB system with a shared or internal CPU pool, the cores are pinned based on the database shape selected for the DB system. For example, if you create a DB system with odb2, then you must license 2 cores.

In a DB system with a shared CPU pool, consider both undersubscription and oversubscription scenarios.

- Undersubscription: Consider a shared CPU pool with 8 cores. If you create a DB system with odb2 and another with odb4, then a total of 6 cores are used. So, although the shared CPU pool is undersubcribed, you must run the virsh command in each KVM or DB system to determine the pinned cores that need to be licensed. In this case, it is the same 8 cores visible to both DB systems.
- Oversubscription: Consider a shared CPU pool with 8 cores, and you create a DB system with odb4 and another with odb6. Although the shared CPU pool is oversubscribed, you must run the virsh command in each KVM or DB System to determine the pinned cores that need to be licensed. In this case, it is the same 8 cores visible to both DB systems.

Note that the same CPU pool subscription policy applies to shared CPU pools for application KVMs too.

Validating the CPUs for an Oracle Database Appliance DB System and Application KVM

You must run the <code>virsh</code> command for every DB system to identify the pinned vCPUs and CPU cores licensing requirements.

To validate that the CPUs for a virtual machine are pinned to a physical thread or core, run the following command:

```
# virsh --readonly vcpuinfo VM name --pretty
```

The following example illustrates how you can validate the CPUs for an Oracle Database Appliance DB System with the db shape odb2 that uses 2 cores (4 vCPUs):

1. Determine the VM Name by running this command:

```
# odacli describe-dbsystem -n dbs1 | grep "VM Name"
VM Name: x97f18b518
```

In this example, the DB System name is dbs1.

2. Run the virsh command to confirm that vCPUs are pinned to physical threads or cores for x97f18b518:

```
# virsh --readonly vcpuinfo x97f18b518 --pretty
VCPU:
               Λ
CPU:
               19
              running
State:
CPU time:
              79.3s
CPU Affinity: 19,24,55,60 (out of 72)
VCPU:
               1
               55
CPU:
State:
               running
CPU time:
               71.5s
```



CPU Affinity: 19,24,55,60 (out of 72)

VCPU: 2
CPU: 60
State: running
CPU time: 71.7s

CPU Affinity: 19,24,55,60 (out of 72)

VCPU: 3
CPU: 24
State: running
CPU time: 73.1s

CPU Affinity: 19,24,55,60 (out of 72)

In this example, the pinned vCPUs are 19, 24, 55, and 60, out of 72.



Capacity-On-Demand Licensing Information

This chapter provides capacity-on-demand licensing information for Oracle Database Appliance bare metal installations.

- Oracle Database Appliance Capacity-on-Demand Licensing
 Capacity-on-Demand software licensing enables you to deploy as few or as many
 processors in Oracle Database Appliance as your workload requires.
- Capacity-On-Demand Licensing for Oracle Database Appliance X10-S, X10-L, and X10-HA
 - Review capacity-on-demand licensing for Oracle Database Appliance X10-S, X10-L, and X10-HA.
- Capacity-On-Demand Licensing for Oracle Database Appliance X9-2S, X9-2L, and X9-2-HA
 - Review capacity-on-demand licensing for Oracle Database Appliance X9-2S, X9-2L, and X9-2-HA.
- Capacity-On-Demand Licensing for Oracle Database Appliance X8-2S, X8-2M, and X8-2-HA
 - Review capacity-on-demand licensing for Oracle Database Appliance X8-2S, X8-2M, and X8-2-HA.
- Capacity-On-Demand Licensing for Oracle Database Appliance X7-2S, X7-2M, and X7-2-HA
 - Review capacity-on-demand licensing for Oracle Database Appliance X7-2S, X7-2M, and X7-2-HA.

Oracle Database Appliance Capacity-on-Demand Licensing

Capacity-on-Demand software licensing enables you to deploy as few or as many processors in Oracle Database Appliance as your workload requires.

Oracle Database Appliance's Capacity-on-Demand feature enables you to add more processor cores to scale up to increased system demands as you need to, without incurring the excessive costs and downtime usually associated with hardware upgrades. Additional cores are increased in 2-core increments.

Oracle Database Appliance Scaling Capabilities

The following table lists the scaling capacities for Oracle Database Appliance bare metal and virtualized platform deployments. The decision to use bare-metal or Oracle Database Appliance Virtualized Platform depends on your company policies and the benefits that each implementation offers your company.

Table 3-1 Oracle Database Appliance Scaling Capacities

Oracle Database Appliance Platform	Minimum Number Processor Cores	Maximum Number Processor Cores
X10-S	2	32

Table 3-1 (Cont.) Oracle Database Appliance Scaling Capacities

Oracle Database Appliance Platform	Minimum Number Processor Cores	Maximum Number Processor Cores
X10-L	2	64
X10-HA	2	128
X9-2S	2	16
X9-2L	2	32
X9-2-HA	2	64
X8-2S	2	16
X8-2M	2	32
X8-2-HA	2	64
X7-2S	2	10
X7-2M	2	36
X7-2-HA	2	72
X6-2S	2	10
X6-2M	2	20
X6-2L	2	20
X6-2-HA	2	40
X5-2	2	72
X4-2	2	48

Applications Deployed on Oracle Database Appliance and Capacity-on-Demand

All Oracle products that are deployed on Oracle Database Appliance can take advantage of Capacity-on-Demand licensing.



For the procedure to set the CPU Core Count, see the *Oracle Database Appliance Deployment and User Guide* for your hardware model.

Capacity-On-Demand Licensing for Oracle Database Appliance X10-S, X10-L, and X10-HA

Review capacity-on-demand licensing for Oracle Database Appliance X10-S, X10-L, and X10-HA.

For the procedure to set the CPU Core Count, see the *Oracle Database Appliance Deployment* and *User Guide* for your hardware model.

The following list describes the number of cores for each Oracle Database Appliance X10-S model:

Oracle Database Appliance X10-S is a single server consisting of 32 cores.

- Oracle Database Appliance X10-L is a single server consisting of 64 cores.
- Oracle Database Appliance X10-HA consists of two servers. Each server has 64 cores, for a total of 128 cores.

By default, Oracle Database Appliance ships with all cores enabled. You can reduce the number of active cores before or after deployment. You can increase the number of active cores when additional capacity is needed. This is known as **capacity-on-demand**. Additional cores are increased in 2-core increments.

Rules and Restrictions for Setting CPU Core Count on Oracle Database Appliance X10-S, X10-L, and X10-HA Bare Metal Deployments

Review the following rules and restrictions before changing the CPU core count:

- You can change the CPU core count to a value that is a multiple of two between 2 and the
 maximum number of cores for the hardware model. For example, for X10-HA, between 2
 and 64 cores for each server for a maximum of 128 cores.
- If you change the CPU core count, then you can subsequently only increase the CPU core count.
- You should only change the CPU core count if you need less than the maximum number of cores.

For example, if you change the CPU core count to 8, then you can subsequently increase the CPU core count to a higher number (in increments of 2 cores), but you cannot decrease the CPU core count.

 If you want the maximum number of cores for each server (32 cores per server for X10-L and X10-HA), then use the default configuration. There is no need to set the CPU core count.



If you mistakenly followed the procedure to set your CPU core count to the maximum, thereby preventing you from subsequently decreasing your CPU core count, and the error is caught immediately, then contact Oracle Support.

Capacity-On-Demand Licensing for Oracle Database Appliance X9-2S, X9-2L, and X9-2-HA

Review capacity-on-demand licensing for Oracle Database Appliance X9-2S, X9-2L, and X9-2-HA.

For the procedure to set the CPU Core Count, see the *Oracle Database Appliance Deployment* and *User Guide* for your hardware model.

The following list describes the number of cores for each Oracle Database Appliance X9-2 model:

- Oracle Database Appliance X9-2S is a single server consisting of 16 cores.
- Oracle Database Appliance X9-2L is a single server consisting of 32 cores.
- Oracle Database Appliance X9-2-HA consists of two servers. Each server has 32 cores, for a total of 64 cores.



By default, Oracle Database Appliance ships with all cores enabled. You can reduce the number of active cores before or after deployment. You can increase the number of active cores when additional capacity is needed. This is known as **capacity-on-demand**. Additional cores are increased in 2-core increments.

Rules and Restrictions for Setting CPU Core Count on Oracle Database Appliance X9-2S, X9-2L, and X9-2-HA Bare Metal Deployments

Review the following rules and restrictions before changing the CPU core count:

- You can change the CPU core count to a value that is a multiple of two between 2 and the
 maximum number of cores for the hardware model. For example, for X9-2-HA, between 2
 and 32 cores for each server for a maximum of 64 cores.
- If you change the CPU core count, then you can subsequently only increase the CPU core count.
- You should only change the CPU core count if you need less than the maximum number of cores.

For example, if you change the CPU core count to 8, then you can subsequently increase the CPU core count to a higher number (in increments of 2 cores), but you cannot decrease the CPU core count.

 If you want the maximum number of cores for each server (32 cores per server for X9-2L and X9-2-HA), then use the default configuration. There is no need to set the CPU core count.

Note:

If you mistakenly followed the procedure to set your CPU core count to the maximum, thereby preventing you from subsequently decreasing your CPU core count, and the error is caught immediately, then contact Oracle Support.

Capacity-On-Demand Licensing for Oracle Database Appliance X8-2S, X8-2M, and X8-2-HA

Review capacity-on-demand licensing for Oracle Database Appliance X8-2S, X8-2M, and X8-2-HA.

For the procedure to set the CPU Core Count, see the *Oracle Database Appliance Deployment* and *User Guide* for your hardware model.

The following list describes the number of cores for each Oracle Database Appliance X8-2 model:

- Oracle Database Appliance X8-2S is a single server consisting of 16 cores.
- Oracle Database Appliance X8-2M is a single server consisting of 32 cores.
- Oracle Database Appliance X8-2-HA consists of two servers. Each server has 32 cores, for a total of 64 cores.

By default, Oracle Database Appliance ships with all cores enabled. You can reduce the number of active cores before or after deployment. You can increase the number of active cores when additional capacity is needed. This is known as **capacity-on-demand**. Additional cores are increased in 2-core increments.



Rules and Restrictions for Setting CPU Core Count on Oracle Database Appliance X8-2S, X8-2M, and X8-2-HA Bare Metal Deployments

Review the following rules and restrictions before changing the CPU core count:

- You can change the CPU core count to a value that is a multiple of two between 2 and the
 maximum number of cores for the hardware model. For example, for X8-2-HA, between 2
 and 32 cores for each server for a maximum of 64 cores.
- If you change the CPU core count, then you can subsequently only increase the CPU core count.
- You should only change the CPU core count if you need less than the maximum number of cores.

For example, if you change the CPU core count to 8, then you can subsequently increase the CPU core count to a higher number (in increments of 2 cores), but you cannot decrease the CPU core count.

 If you want the maximum number of cores for each server (32 cores per server for X8-2M and X8-2-HA), then use the default configuration. There is no need to set the CPU core count.



If you mistakenly followed the procedure to set your CPU core count to the maximum, thereby preventing you from subsequently decreasing your CPU core count, and the error is caught immediately, then contact Oracle Support.

Capacity-On-Demand Licensing for Oracle Database Appliance X7-2S, X7-2M, and X7-2-HA

Review capacity-on-demand licensing for Oracle Database Appliance X7-2S, X7-2M, and X7-2-HA.

For the procedure to se the CPU Core Count, see the *Oracle Database Appliance Deployment* and *User Guide* for your hardware model.

The following list describes the number of cores for each Oracle Database Appliance X7-2 model:

- Oracle Database Appliance X7-2S is a single server consisting of 10 cores.
- Oracle Database Appliance X7-2M is a single server consisting of 36 cores.
- Oracle Database Appliance X7-2-HA consists of two servers. Each server has 36 cores, for a total of 72 cores.

By default, Oracle Database Appliance ships with all cores enabled. You can reduce the number of active cores before or after deployment. You can increase the number of active cores when additional capacity is needed. This is known as **capacity-on-demand**. Additional cores are increased in 2-core increments.

Rules and Restrictions for Setting CPU Core Count on Oracle Database Appliance X7-2S, X7-2M, and X7-2-HA Bare Metal Deployments

Review the following rules and restrictions before changing the CPU core count:



- You can change the CPU core count to a value that is a multiple of two between 2 and the maximum number of cores for the hardware model. For example, for X7-2-HA, between 2 and 36 cores for each server for a maximum of 72 cores.
- If you change the CPU core count, then you can subsequently only increase the CPU core count.
- You should only change the CPU core count if you need less than the maximum number of cores.

For example, if you change the CPU core count to 8, then you can subsequently increase the CPU core count to a higher number (in increments of 2 cores), but you cannot decrease the CPU core count.

 If you want the maximum number of cores for each server (36 cores per server for X7-2M and X7-2-HA), then use the default configuration. There is no need to set the CPU core count.



If you mistakenly followed the procedure to set your CPU core count to the maximum, thereby preventing you from subsequently decreasing your CPU core count, and the error is caught immediately, then contact Oracle Support.



4

Third-Party Product Licenses for This Release

This chapter contains the licenses for the third-party products that are included with Oracle Database Appliance for this release.

- Oracle Database Third-Party Licensing Information
 Understand licensing information about third-party products used by Oracle Database.
- Other Third-Party Product Licenses
 Review other third-party product licenses for Oracle Database Appliance.
- Written Offer for Source Code

Oracle Database Third-Party Licensing Information

Understand licensing information about third-party products used by Oracle Database.

Oracle Database Appliance includes Oracle Database19c. To view the licenses for these third-party products, refer to the release-specific *Oracle Database Licensing Information User Manual*.

Related Topics

- Licensing Information User Manual Oracle Database 21c
- Licensing Information User Manual Oracle Database 19c

Other Third-Party Product Licenses

Review other third-party product licenses for Oracle Database Appliance.

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Simple Logging Facade for Java (SLF4J)

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dragon4

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		unuran-1.8.1/doc/figures/Makefile.in
		unuran-1.8.1/doc/figures/
		discrete_inversion.eps
		unuran-1.8.1/doc/figures/
		discrete_inversion.pdf
		unuran-1.8.1/doc/figures/
		discrete_inversion.png
		unuran-1.8.1/doc/figures/
		<pre>discrete_inversion.txt unuran-1.8.1/doc/figures/inversion.eps</pre>
		unuran-1.8.1/doc/figures/inversion.eps unuran-1.8.1/doc/figures/inversion.pdf
		unuran-1.8.1/doc/figures/inversion.png
		unuran-1.8.1/doc/figures/inversion.txt
		unuran-1.8.1/doc/figures/
		rejection from constant hat.eps
		unuran-1.8.1/doc/figures/
		rejection from constant hat.pdf
		unuran-1.8.1/doc/figures/
		rejection from constant hat.png
		unuran-1.8.1/doc/figures/
		rejection from constant hat.txt
		unuran-1.8.1/doc/figures/rou-cauchy.eps
		unuran-1.8.1/doc/figures/rou-cauchy.pdf
		unuran-1.8.1/doc/figures/rou-cauchy.png
		unuran-1.8.1/doc/figures/rou-cauchy.txt
		unuran-1.8.1/doc/figures/texpict2img.pl
		unuran-1.8.1/doc/src/Makefile.am
		unuran-1.8.1/doc/src/Makefile.in
		unuran-1.8.1/doc/src/README
		unuran-1.8.1/doc/src/arvag.dh
		unuran-1.8.1/doc/src/error_debug.dh
		unuran-1.8.1/doc/src/examples.dh
		unuran-1.8.1/doc/src/glossary.dh
		unuran-1.8.1/doc/src/index.dh
		unuran-1.8.1/doc/src/installation.dh
		unuran-1.8.1/doc/src/intro.dh
		unuran-1.8.1/doc/src/make_texi.pl
		unuran-1.8.1/doc/src/methods.dh unuran-1.8.1/doc/src/methods cemp.texi
		unuran-1.8.1/doc/src/methods_cemp.texi unuran-1.8.1/doc/src/methods_cont.texi
		unuran-1.8.1/doc/src/methods_cont.texi unuran-1.8.1/doc/src/methods_cvec.texi
		unuran-1.8.1/doc/src/methods_cvemp.texi
		unuran-1.8.1/doc/src/methods_cvemp.texi unuran-1.8.1/doc/src/methods_discr.texi
		unuran-1.8.1/doc/src/methods_discr.texi unuran-1.8.1/doc/src/methods matr.texi
		unuran-1.8.1/doc/src/methods_matr.texi unuran-1.8.1/doc/src/methods_mcmc.texi
		unuran-1.8.1/doc/src/misc.dh
		iiniiran-I X I/doc/erc/miec dh

Table 4-1 (Cont.) Open Source or Other Separately Licensed Software

unuran-1.8.1/doc/src/ref_example_anti.texi unuran-1.8.1/doc/src/ref_example_cext.texi unuran-1.8.1/doc/src/ref_example_cont.texi unuran-1.8.1/doc/src/ref_example_cont.texi unuran-1.8.1/doc/src/ref_example_cont.texi unuran-1.8.1/doc/src/ref_example_discr.texi unuran-1.8.1/doc/src/ref_example_discr.texi unuran-1.8.1/doc/src/ref_example_discr.texi unuran-1.8.1/doc/src/ref_example_discr.texi unuran-1.8.1/doc/src/ref_example_emp.texi unuran-1.8.1/doc/src/ref_example_emp.texi unuran-1.8.1/doc/src/ref_example_emp.texi unuran-1.8.1/doc/src/ref_example_mixt.texi unuran-1.8.1/doc/src/ref_example_mixt.texi unuran-1.8.1/doc/src/ref_example_mixt.texi unuran-1.8.1/doc/src/ref_example_win32_1.te unuran-1.8.1/doc/src/ref_example_win32_1.te unuran-1.8.1/doc/src/ref_example_win32_2.te unuran-1.8.1/doc/src/ref_example_win32_2.te unuran-1.8.1/doc/src/ref_example_win32_3.te unuran-1.8.1/doc/src/texfddist.dh unuran-1.8.1/doc/src/texfddist.dh unuran-1.8.1/doc/src/texfunuran_src.texi unuran-1.8.1/doc/src/texfunuran_src.texi unuran-1.8.1/doc/unuran.pdf unuran-1.8.1/doc/unuran.pdf unuran-1.8.1/doc/unuran.pdf unuran-1.8.1/doc/unuran.texi unuran-1.8.1/doc/unuran.texi unuran-1.8.1/doc/unuran.texi unuran-1.8.1/doc/unuran.texi unuran-1.8.1/doc/unuran.win32.texi unuran-1.8.1/doc/unuran.win32.texi unuran-1.8.1/doc/unuran.win32.texi unuran-1.8.1/doc/unuran.win32.texi unuran-1.8.1/doc/unuran.win32.texi unuran-1.8.1/doc/unuran.win32.texi unuran-1.8.1/doc/unuran.win32.texi unuran-1.8.1/doc/unuran.win32.texi unuran-1.8.1/doc/unuran.lexi.exampleo.c unuran-1.8.1/doc/unuran.lexi.exampleo.c unuran-1.8.1/doc/exampleo.c unuran-1.8.1/examples/exampleo.c unuran-1.8.1/examples/exampleo.c unuran-1.8.1/examples/exampleo.c	unuran-1.8.1/doc/src/ref_example1_texi unuran-1.8.1/doc/src/ref_example2_texi unuran-1.8.1/doc/src/ref_example2_texi unuran-1.8.1/doc/src/ref_example2_texi unuran-1.8.1/doc/src/ref_example3_texi unuran-1.8.1/doc/src/ref_example3_texi unuran-1.8.1/doc/src/ref_example3_texi unuran-1.8.1/doc/src/ref_example3_texi unuran-1.8.1/doc/src/ref_example_funcStr.texi unuran-1.8.1/doc/src/ref_example_ext.texi unuran-1.8.1/doc/src/ref_example_cont.texi unuran-1.8.1/doc/src/ref_example_cont.texi unuran-1.8.1/doc/src/ref_example_cont.texi unuran-1.8.1/doc/src/ref_example_discr.texi unuran-1.8.1/doc/src/ref_example_discr.texi unuran-1.8.1/doc/src/ref_example_emp.texi unuran-1.8.1/doc/src/ref_example_emp.texi unuran-1.8.1/doc/src/ref_example_emp.texi unuran-1.8.1/doc/src/ref_example_emp.texi unuran-1.8.1/doc/src/ref_example_mixt.texi unuran-1.8.1/doc/src/ref_example_mixt.texi unuran-1.8.1/doc/src/ref_example_mixt.texi unuran-1.8.1/doc/src/ref_example_mixt.texi unuran-1.8.1/doc/src/ref_example_win32_1.te unuran-1.8.1/doc/src/ref_example_win32_1.te unuran-1.8.1/doc/src/ref_example_win32_1.te unuran-1.8.1/doc/src/ref_example_win32_1.te unuran-1.8.1/doc/src/ref_example_win32_1.te unuran-1.8.1/doc/src/ref_example_win32_1.te unuran-1.8.1/doc/src/ref_example_win32_1.te unuran-1.8.1/doc/src/texf_example_win32_1.te unuran-1.8.1/doc/src/texf_example_win32_1.te unuran-1.8.1/doc/src/texf_example_win32_1.te unuran-1.8.1/doc/unuran.txt unuran-1.8.1/doc/unuran.info unuran-1.	Provider	Component	Licensing Information
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unuran-1.8.1/doc/version_win32.texi unuran-1.8.1/examples/Makefile.am unuran-1.8.1/examples/Makefile.in unuran-1.8.1/examples/example0.c unuran-1.8.1/examples/example0_str.c unuran-1.8.1/examples/example1.c	unuran-1.8.1/doc/version_win32.texi unuran-1.8.1/examples/Makefile.am unuran-1.8.1/examples/Makefile.in unuran-1.8.1/examples/example0.c unuran-1.8.1/examples/example0_str.c unuran-1.8.1/examples/example1.c			
unuran-1.8.1/examples/Makefile.am unuran-1.8.1/examples/Makefile.in unuran-1.8.1/examples/example0.c unuran-1.8.1/examples/example0_str.c unuran-1.8.1/examples/example1.c	unuran-1.8.1/examples/Makefile.am unuran-1.8.1/examples/Makefile.in unuran-1.8.1/examples/example0.c unuran-1.8.1/examples/example0_str.c unuran-1.8.1/examples/example1.c			
unuran-1.8.1/examples/Makefile.in unuran-1.8.1/examples/example0.c unuran-1.8.1/examples/example0_str.c unuran-1.8.1/examples/example1.c	unuran-1.8.1/examples/Makefile.in unuran-1.8.1/examples/example0.c unuran-1.8.1/examples/example0_str.c unuran-1.8.1/examples/example1.c			-
unuran-1.8.1/examples/example0.c unuran-1.8.1/examples/example0_str.c unuran-1.8.1/examples/example1.c	unuran-1.8.1/examples/example0.c unuran-1.8.1/examples/example0_str.c unuran-1.8.1/examples/example1.c			
<pre>unuran-1.8.1/examples/example0_str.c unuran-1.8.1/examples/example1.c</pre>	unuran-1.8.1/examples/example0_str.c unuran-1.8.1/examples/example1.c			
unuran-1.8.1/examples/example1.c	unuran-1.8.1/examples/example1.c			
	unuran-1.8.1/examples/examplel_str.c			

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		unuran-1.8.1/examples/example2.c
		unuran-1.8.1/examples/example2 str.c
		unuran-1.8.1/examples/example3.c
		unuran-1.8.1/examples/example3_str.c
		unuran-1.8.1/examples/example_FuncStr.c
		unuran-1.8.1/examples/example_anti.c
		unuran-1.8.1/examples/example_anti_str.c
		unuran-1.8.1/examples/example_cext.c
		unuran-1.8.1/examples/example_cont.c
		unuran-1.8.1/examples/example_cont_str.c
		unuran-1.8.1/examples/example_cpp.cpp
		unuran-1.8.1/examples/example_dext.c
		unuran-1.8.1/examples/example_discr.c
		unuran-1.8.1/examples/example_discr_str.c
		unuran-1.8.1/examples/example_emp.c
		unuran-1.8.1/examples/example_emp_str.c
		unuran-1.8.1/examples/example_errorhandler.
		unuran-1.8.1/examples/example_gsl.c
		unuran-1.8.1/examples/example_mcorr.c
		unuran-1.8.1/examples/example_mixt.c
		unuran-1.8.1/examples/example mixt inv.c
		unuran-1.8.1/examples/example prng.c
		unuran-1.8.1/examples/example prng str.c
		unuran-1.8.1/examples/example rngstreams.c
		unuran-1.8.1/examples/example vemp.c
		unuran-1.8.1/experiments/Makefile.am
		unuran-1.8.1/experiments/Makefile.in
		unuran-1.8.1/experiments/make timing table.
		unuran-1.8.1/experiments/timings chap 10.co
		unuran-1.8.1/experiments/timings chap 8.com
		unuran-1.8.1/scripts/Makefile.am
		unuran-1.8.1/scripts/Makefile.in
		unuran-1.8.1/scripts/
		compute machine constants.c
		unuran-1.8.1/scripts/make urng header.pl
		unuran-1.8.1/scripts/merge h.pl
		unuran-1.8.1/scripts/read PDF.pl
		unuran-1.8.1/scripts/remove comments.pl
		unuran-1.8.1/scripts/run valgrind.sh
		unuran-1.8.1/scripts/win32/Makefile.win32
		unuran-1.8.1/scripts/win32/build.sh
		unuran-1.8.1/scripts/win32/example1.c
		unuran-1.8.1/scripts/win32/example2.c
		unuran-1.8.1/scripts/win32/make dll def.pl
		unuran-1.8.1/src/Makefile.am
		unuran-1.8.1/src/Makefile.in
		unuran-1.8.1/src/README
		unuran-1.8.1/src/distr/Makefile.am
		unuran-1.8.1/src/distr/Makefile.in
		unuran-1.8.1/src/distributions/Makefile.am
		unuran-1.8.1/src/distributions/Makefile.in
		unuran-1.8.1/src/distributions/README
		unuran-1.8.1/src/methods/Makefile.am

unuran-1.8.1/src/methods/Makefile.in unuran-1.8.1/src/parser/Makefile.am

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		unuran-1.8.1/src/parser/Makefile.in
		unuran-1.8.1/src/parser/functparser_doc.dh
		unuran-1.8.1/src/parser/make_stringparser.pl
		unuran-1.8.1/src/parser/stringparser_doc.dh
		unuran-1.8.1/src/specfunct/Makefile.am
		unuran-1.8.1/src/specfunct/Makefile.in
		unuran-1.8.1/src/tests/Makefile.am
		unuran-1.8.1/src/tests/Makefile.in
		unuran-1.8.1/src/uniform/Makefile.am
		unuran-1.8.1/src/uniform/Makefile.in
		unuran-1.8.1/src/uniform/fish.c
		unuran-1.8.1/src/uniform/mrg31k3p.c
		unuran-1.8.1/src/uniform/mstd.c
		unuran-1.8.1/src/uniform/unuran_urng_gsl.h
		unuran-1.8.1/src/uniform/unuran_urng_prng.h
		unuran-1.8.1/src/uniform/
		unuran_urng_rngstreams.h
		unuran-1.8.1/src/uniform/urng_builtin.c
		unuran-1.8.1/src/uniform/urng_builtin.h
		unuran-1.8.1/src/uniform/urng_fvoid.c
		unuran-1.8.1/src/uniform/urng_fvoid.h
		unuran-1.8.1/src/uniform/urng_gsl.c
		unuran-1.8.1/src/uniform/urng_gsl.h
		unuran-1.8.1/src/uniform/urng_gslqrng.c
		unuran-1.8.1/src/uniform/urng_gslqrng.h
		unuran-1.8.1/src/uniform/urng_prng.c
		unuran-1.8.1/src/uniform/urng_prng.h
		unuran-1.8.1/src/uniform/urng_randomshift.c
		unuran-1.8.1/src/uniform/urng_randomshift.h
		unuran-1.8.1/src/uniform/urng_rngstreams.c
		unuran-1.8.1/src/uniform/urng_rngstreams.h
		unuran-1.8.1/src/unuran.h.in
		unuran-1.8.1/src/urng/Makefile.am
		unuran-1.8.1/src/urng/Makefile.in
		unuran-1.8.1/src/utils/Makefile.am
		unuran-1.8.1/src/utils/Makefile.in
		unuran-1.8.1/tests/Makefile.am
		unuran-1.8.1/tests/Makefile.in
		unuran-1.8.1/tests/README.conf
		unuran-1.8.1/tests/make_test_files.pl
		unuran-1.8.1/tests/t_arou.c
		unuran-1.8.1/tests/t_arou.conf unuran-1.8.1/tests/t ars.c
		unuran-1.8.1/tests/t_ars.c unuran-1.8.1/tests/t ars.conf
		unuran-1.8.1/tests/t_ars.com
		unuran-1.8.1/tests/t_auto.c unuran-1.8.1/tests/t auto.conf
		unuran-1.8.1/tests/t_auto.comi unuran-1.8.1/tests/t_cext.c
		unuran-1.8.1/tests/t_cext.c unuran-1.8.1/tests/t cext.conf
		unuran-1.8.1/tests/t_cext.com/ unuran-1.8.1/tests/t_cstd.c
		unuran-1.8.1/tests/t_cstd.c unuran-1.8.1/tests/t cstd.conf
		unuran-1.8.1/tests/t_cstd.com unuran-1.8.1/tests/t dari.c
		unuran-1.8.1/tests/t_dari.c unuran-1.8.1/tests/t dari.conf
		unuran-1.8.1/tests/t_dar1.conf unuran-1.8.1/tests/t dau.c
		unuran-1.8.1/tests/t_dau.c unuran-1.8.1/tests/t_dau.conf
		unuran-1.8.1/tests/t_dau.conf unuran-1.8.1/tests/t deprecated tdrgw.c
		unuran-1.0.1/tests/t_deprecated_targw.c

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Provider	Component	Licensing Information
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unuran-1.8.1/tests/t deprecated vmt.c unuran-1.8.1/tests/t deprecated vmt.conf unuran-1.8.1/tests/t dext.c unuran-1.8.1/tests/t_dext.conf unuran-1.8.1/tests/t dgt.c unuran-1.8.1/tests/t dgt.conf unuran-1.8.1/tests/t distr.c unuran-1.8.1/tests/t distr.conf unuran-1.8.1/tests/t distr cemp.c unuran-1.8.1/tests/t distr cemp.conf unuran-1.8.1/tests/t_distr_condi.c unuran-1.8.1/tests/t distr condi.conf unuran-1.8.1/tests/t_distr_cont.c unuran-1.8.1/tests/t_distr_cont.conf unuran-1.8.1/tests/t distr corder.c unuran-1.8.1/tests/t distr corder.conf unuran-1.8.1/tests/t_distr_cvec.c unuran-1.8.1/tests/t_distr_cvec.conf unuran-1.8.1/tests/t_distr_cvemp.c unuran-1.8.1/tests/t_distr_cvemp.conf unuran-1.8.1/tests/t_distr_cxtrans.c unuran-1.8.1/tests/t distr cxtrans.conf unuran-1.8.1/tests/t distr discr.c unuran-1.8.1/tests/t distr discr.conf unuran-1.8.1/tests/t distr matr.c unuran-1.8.1/tests/t distr matr.conf unuran-1.8.1/tests/t dsrou.c unuran-1.8.1/tests/t dsrou.conf unuran-1.8.1/tests/t dss.c unuran-1.8.1/tests/t dss.conf unuran-1.8.1/tests/t dstd.c unuran-1.8.1/tests/t dstd.conf unuran-1.8.1/tests/t_empk.c unuran-1.8.1/tests/t_empk.conf unuran-1.8.1/tests/t empl.c unuran-1.8.1/tests/t_empl.conf unuran-1.8.1/tests/t gibbs.c unuran-1.8.1/tests/t gibbs.conf unuran-1.8.1/tests/t hinv.c unuran-1.8.1/tests/t hinv.conf unuran-1.8.1/tests/t hist.c unuran-1.8.1/tests/t hist.conf unuran-1.8.1/tests/t hitro.c unuran-1.8.1/tests/t hrb.c unuran-1.8.1/tests/t hrb.conf unuran-1.8.1/tests/t hrd.c unuran-1.8.1/tests/t hrd.conf unuran-1.8.1/tests/t hri.c unuran-1.8.1/tests/t hri.conf unuran-1.8.1/tests/t info.c unuran-1.8.1/tests/t info.conf unuran-1.8.1/tests/t itdr.c unuran-1.8.1/tests/t itdr.conf unuran-1.8.1/tests/t mcorr.c unuran-1.8.1/tests/t mcorr.conf



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Provider	Component	Licensing Information
		unuran-1.8.1/tests/t_mixt.c
		unuran-1.8.1/tests/t mvstd.c
		unuran-1.8.1/tests/t mvstd.conf
		unuran-1.8.1/tests/t_mvtdr.c
		unuran-1.8.1/tests/t ninv.c
		unuran-1.8.1/tests/t ninv.conf
		unuran-1.8.1/tests/t norta.c
		unuran-1.8.1/tests/t norta.conf
		unuran-1.8.1/tests/t_nrou.c
		unuran-1.8.1/tests/t_nrou.conf
		unuran-1.8.1/tests/t pinv
		unuran-1.8.1/tests/t pinv.c
		unuran-1.8.1/tests/t srou.c
		unuran-1.8.1/tests/t_srou.conf
		unuran-1.8.1/tests/t_ssr.c
		unuran-1.8.1/tests/t ssr.conf
		unuran-1.8.1/tests/t stringparser.c
		unuran-1.8.1/tests/t stringparser.conf
		unuran-1.8.1/tests/t_tabl.c
		unuran-1.8.1/tests/t_tabl.conf
		unuran-1.8.1/tests/t tdr.c
		unuran-1.8.1/tests/t tdr.conf
		unuran-1.8.1/tests/t tdr gw.c
		unuran-1.8.1/tests/t_tdr_gw.conf
		unuran-1.8.1/tests/t_tdr_ia.c
		unuran-1.8.1/tests/t tdr ia.conf
		unuran-1.8.1/tests/t tdr ps.c
		unuran-1.8.1/tests/t tdr ps.conf
		unuran-1.8.1/tests/t_unif.c
		unuran-1.8.1/tests/t unif.conf
		unuran-1.8.1/tests/t_unur_error.c
		unuran-1.8.1/tests/t_unur_error.conf
		unuran-1.8.1/tests/t unur tests.c
		unuran-1.8.1/tests/t_unur_tests.conf
		unuran-1.8.1/tests/t_urng.c
		unuran-1.8.1/tests/t urng.conf

unuran-1.8.1/tests/t_utdr.c
unuran-1.8.1/tests/t_utdr.conf
unuran-1.8.1/tests/t_util_matrix.c
unuran-1.8.1/tests/t_util_matrix.conf

unuran-1.8.1/tests/t_vempk.c
unuran-1.8.1/tests/t_vempk.conf
unuran-1.8.1/tests/t_vnrou.c
unuran-1.8.1/tests/t_vnrou.conf
unuran-1.8.1/tests/t_x_gen.c
unuran-1.8.1/tests/t_x_gen.conf
unuran-1.8.1/tests/test_StdDistr.c
unuran-1.8.1/tests/test_StdDistr.m
unuran-1.8.1/tests/test_functionparser.c
unuran-1.8.1/tests/test_functionparser.m

unuran-1.8.1/tests/testcounter.c
unuran-1.8.1/tests/testdistributions/

unuran-1.8.1/tests/testdistributions/

Makefile.am

Makefile.in



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		unuran-1.8.1/tests/testdistributions/ c_sawtooth_contpdf.c unuran-1.8.1/tests/testdistributions/
		<pre>c_sawtooth_discpdf.c</pre>
		unuran-1.8.1/tests/testdistributions/ c with multiple of pdf.c
		unuran-1.8.1/tests/testdistributions/
		<pre>c_wo_logpdf.c unuran-1.8.1/tests/testdistributions/ testdistributions.h</pre>
		unuran-1.8.1/tests/testdistributions/ vc cauchy RoU ball.c
		unuran-1.8.1/tests/testdistributions/ vc special correlations ar1.c
		unuran-1.8.1/tests/testdistributions/ vc special correlations constantrho.c
		unuran-1.8.1/tests/testdistributions/
		vc_w_marginals.c
		unuran-1.8.1/tests/testdistributions/ vc wo logpdf.c
		unuran-1.8.1/tests/testroutines.c
		unuran-1.8.1/tests/testunuran.h
		unuran-1.8.1/src/distr/deprecated_distr.c
		unuran-1.8.1/src/distr/deprecated_distr.h
		unuran-1.8.1/src/methods/deprecated_methods.c unuran-1.8.1/src/methods/deprecated_methods.h unuran-1.8.1/src/methods/deprecated_tdrgw.h
		unuran-1.8.1/src/methods/deprecated_tdrgw.n
		<pre>unuran-1.8.1/src/methods/deprecated_vmt.h unuran-1.8.1/src/methods/</pre>
		deprecated_vmt_struct.h
		<pre>unuran-1.8.1/src/parser/ stringparser_lists.ch.in</pre>
		UNU.RAN relies on a modified version of the library Cephes, see ./src/src/specfunct/
		cephes_source.h
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Adapted from a C++ implementation of Chris Doty-Humphrey's SFC PRNG.

https://gist.github.com/imneme/f1f7821f07cf76504a97f6537c818083

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		to use the UNU.RAN code excluding the uniform
		<pre>random number generator in src/uniform/</pre>
		mrg31k3p.c (copyright by Renee Touzin)
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		been removed from the original library:
		unuran-1.8.1/COPYING
		unuran-1.8.1/INSTALL unuran-1.8.1/Makefile.am
		unuran-1.8.1/Makefile.in
		unuran-1.8.1/NEWS
		unuran-1.8.1/UPGRADE
		unuran-1.8.1/acinclude.m4
		unuran-1.8.1/aclocal.m4
		unuran-1.8.1/autoconf/config.guess
		unuran-1.8.1/autoconf/config.sub
		unuran-1.8.1/autoconf/depcomp
		unuran-1.8.1/autoconf/install-sh
		unuran-1.8.1/autoconf/ltmain.sh unuran-1.8.1/autoconf/mdate-sh
		unuran-1.8.1/autoconf/mdate-sn unuran-1.8.1/autoconf/missing
		unuran-1.8.1/autocom/missing unuran-1.8.1/autogen.sh
		unuran-1.8.1/configure
		unuran-1.8.1/doc/Makefile.am
		unuran-1.8.1/doc/Makefile.in
		unuran-1.8.1/doc/figures/Makefile.am
		unuran-1.8.1/doc/figures/Makefile.in
		unuran-1.8.1/doc/figures/
		discrete inversion.eps

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		unuran-1.8.1/doc/figures/
		discrete_inversion.pdf
		unuran-1.8.1/doc/figures/
		discrete inversion.png
		unuran-1.8.1/doc/figures/
		discrete inversion.txt
		unuran-1.8.1/doc/figures/inversion.eps
		unuran-1.8.1/doc/figures/inversion.pdf
		unuran-1.8.1/doc/figures/inversion.png
		unuran-1.8.1/doc/figures/inversion.txt
		unuran-1.8.1/doc/figures/
		rejection from constant hat.eps
		unuran-1.8.1/doc/figures/
		rejection from constant hat.pdf
		unuran-1.8.1/doc/figures/
		rejection from constant hat.png
		unuran-1.8.1/doc/figures/
		rejection from constant hat.txt
		unuran-1.8.1/doc/figures/rou-cauchy.eps
		unuran-1.8.1/doc/figures/rou-cauchy.pdf
		unuran-1.8.1/doc/figures/rou-cauchy.png
		unuran-1.8.1/doc/figures/rou-cauchy.txt
		unuran-1.8.1/doc/figures/texpict2img.pl
		unuran-1.8.1/doc/src/Makefile.am
		unuran-1.8.1/doc/src/Makefile.in
		unuran-1.8.1/doc/src/README
		unuran-1.8.1/doc/src/arvag.dh
		unuran-1.8.1/doc/src/error_debug.dh
		unuran-1.8.1/doc/src/examples.dh
		unuran-1.8.1/doc/src/glossary.dh
		unuran-1.8.1/doc/src/index.dh
		unuran-1.8.1/doc/src/installation.dh
		unuran-1.8.1/doc/src/intro.dh
		unuran-1.8.1/doc/src/make_texi.pl
		unuran-1.8.1/doc/src/methods.dh
		unuran-1.8.1/doc/src/methods_cemp.texi
		unuran-1.8.1/doc/src/methods_cont.texi
		unuran-1.8.1/doc/src/methods_cvec.texi
		unuran-1.8.1/doc/src/methods_cvemp.texi
		unuran-1.8.1/doc/src/methods_discr.texi
		unuran-1.8.1/doc/src/methods_matr.texi
		unuran-1.8.1/doc/src/methods_mcmc.texi
		unuran-1.8.1/doc/src/misc.dh
		unuran-1.8.1/doc/src/ref_example0.texi
		unuran-1.8.1/doc/src/ref_example0_str.texi
		unuran-1.8.1/doc/src/ref_example1.texi
		unuran-1.8.1/doc/src/ref_example1_str.texi
		unuran-1.8.1/doc/src/ref_example2.texi
		unuran-1.8.1/doc/src/ref_example2_str.texi
		unuran-1.8.1/doc/src/ref_example3.texi
		unuran-1.8.1/doc/src/ref_example3_str.texi
		unuran-1.8.1/doc/src/ref_example_FuncStr.te
		unuran-1.8.1/doc/src/ref_example_anti.texi
		unuran-1.8.1/doc/src/

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		unuran-1.8.1/doc/src/ref_example_cont.texi
		unuran-1.8.1/doc/src/
		ref_example_cont_str.texi
		unuran-1.8.1/doc/src/ref_example_dext.texi
		unuran-1.8.1/doc/src/ref_example_discr.texi
		unuran-1.8.1/doc/src/
		ref_example_discr_str.texi
		unuran-1.8.1/doc/src/ref_example_emp.texi
		unuran-1.8.1/doc/src/ref_example_emp_str.tex
		unuran-1.8.1/doc/src/ref_example_gsl.texi
		unuran-1.8.1/doc/src/ref_example_mixt.texi
		unuran-1.8.1/doc/src/
		ref_example_mixt_inv.texi
		unuran-1.8.1/doc/src/
		ref_example_rngstreams.texi
		unuran-1.8.1/doc/src/ref_example_vemp.texi
		unuran-1.8.1/doc/src/ref_example_win32_1.tex
		unuran-1.8.1/doc/src/ref_example_win32_2.tex unuran-1.8.1/doc/src/references.dh
		unuran-1.8.1/doc/src/references.an unuran-1.8.1/doc/src/stddist.dh
		unuran-1.8.1/doc/src/stdd1st.an unuran-1.8.1/doc/src/texinfo.tex
		unuran-1.8.1/doc/src/texinfo.tex unuran-1.8.1/doc/src/top.dh
		unuran-1.8.1/doc/src/unuran src.texi
		unuran-1.8.1/doc/stamp-1
		unuran-1.8.1/doc/stamp-vti
		unuran-1.8.1/doc/unuran.html
		unuran-1.8.1/doc/unuran.info
		unuran-1.8.1/doc/unuran.pdf
		unuran-1.8.1/doc/unuran.texi
		unuran-1.8.1/doc/unuran.txt
		unuran-1.8.1/doc/unuran win32.html
		unuran-1.8.1/doc/unuran win32.info
		unuran-1.8.1/doc/unuran win32.pdf
		unuran-1.8.1/doc/unuran win32.texi
		unuran-1.8.1/doc/unuran_win32_libname.texi
		unuran-1.8.1/doc/version.texi
		unuran-1.8.1/doc/version win32.texi
		unuran-1.8.1/examples/Makefile.am
		unuran-1.8.1/examples/Makefile.in
		unuran-1.8.1/examples/example0.c
		unuran-1.8.1/examples/example0_str.c
		unuran-1.8.1/examples/example1.c
		unuran-1.8.1/examples/example1_str.c
		unuran-1.8.1/examples/example2.c
		unuran-1.8.1/examples/example2_str.c
		unuran-1.8.1/examples/example3.c
		unuran-1.8.1/examples/example3_str.c
		unuran-1.8.1/examples/example_FuncStr.c
		unuran-1.8.1/examples/example_anti.c
		unuran-1.8.1/examples/example_anti_str.c
		unuran-1.8.1/examples/example_cext.c
		unuran-1.8.1/examples/example_cont.c
		unuran-1.8.1/examples/example cont str.c
		unuran-1.8.1/examples/example cpp.cpp

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		unuran-1.8.1/examples/example dext.c
		unuran-1.8.1/examples/example discr.c
		unuran-1.8.1/examples/example_discr_str.c
		unuran-1.8.1/examples/example_emp.c
		unuran-1.8.1/examples/example_emp_str.c
		unuran-1.8.1/examples/example_errorhandler.
		unuran-1.8.1/examples/example_gsl.c
		unuran-1.8.1/examples/example_mcorr.c
		unuran-1.8.1/examples/example_mixt.c
		unuran-1.8.1/examples/example_mixt_inv.c
		unuran-1.8.1/examples/example_prng.c
		unuran-1.8.1/examples/example_prng_str.c
		unuran-1.8.1/examples/example_rngstreams.c
		unuran-1.8.1/examples/example_vemp.c
		unuran-1.8.1/experiments/Makefile.am
		unuran-1.8.1/experiments/Makefile.in
		unuran-1.8.1/experiments/make_timing_table unuran-1.8.1/experiments/timings_chap_10.co
		unuran-1.8.1/experiments/timings_chap_10.co
		unuran-1.8.1/scripts/Makefile.am
		unuran-1.8.1/scripts/Makefile.in
		unuran-1.8.1/scripts/makerire.in
		compute machine constants.c
		unuran-1.8.1/scripts/make urng header.pl
		unuran-1.8.1/scripts/merge h.pl
		unuran-1.8.1/scripts/read PDF.pl
		unuran-1.8.1/scripts/remove comments.pl
		unuran-1.8.1/scripts/run valgrind.sh
		unuran-1.8.1/scripts/win32/Makefile.win32
		unuran-1.8.1/scripts/win32/build.sh
		unuran-1.8.1/scripts/win32/example1.c
		unuran-1.8.1/scripts/win32/example2.c
		unuran-1.8.1/scripts/win32/make dll def.pl
		unuran-1.8.1/src/Makefile.am
		unuran-1.8.1/src/Makefile.in
		unuran-1.8.1/src/README
		unuran-1.8.1/src/distr/Makefile.am
		unuran-1.8.1/src/distr/Makefile.in
		unuran-1.8.1/src/distributions/Makefile.am
		unuran-1.8.1/src/distributions/Makefile.in
		unuran-1.8.1/src/distributions/README
		unuran-1.8.1/src/methods/Makefile.am
		unuran-1.8.1/src/methods/Makefile.in
		unuran-1.8.1/src/parser/Makefile.am
		unuran-1.8.1/src/parser/Makefile.in
		unuran-1.8.1/src/parser/functparser_doc.dh
		unuran-1.8.1/src/parser/make_stringparser.
		unuran-1.8.1/src/parser/stringparser_doc.di
		unuran-1.8.1/src/specfunct/Makefile.am
		unuran-1.8.1/src/specfunct/Makefile.in
		unuran-1.8.1/src/tests/Makefile.am
		unuran-1.8.1/src/tests/Makefile.in
		unuran-1.8.1/src/uniform/Makefile.am
		unuran-1.8.1/src/uniform/Makefile.in

unuran-1.8.1/src/uniform/fish.c

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		unuran-1.8.1/src/uniform/mstd.c
		unuran-1.8.1/src/uniform/unuran_urng_gsl.h
		unuran-1.8.1/src/uniform/unuran_urng_prng.h
		unuran-1.8.1/src/uniform/
		unuran_urng_rngstreams.h
		unuran-1.8.1/src/uniform/urng_builtin.c
		unuran-1.8.1/src/uniform/urng_builtin.h
		unuran-1.8.1/src/uniform/urng_fvoid.c
		unuran-1.8.1/src/uniform/urng_fvoid.h
		unuran-1.8.1/src/uniform/urng_gsl.c
		unuran-1.8.1/src/uniform/urng_gsl.h
		unuran-1.8.1/src/uniform/urng_gslqrng.c
		unuran-1.8.1/src/uniform/urng_gslqrng.h
		unuran-1.8.1/src/uniform/urng_prng.c
		unuran-1.8.1/src/uniform/urng_prng.h unuran-1.8.1/src/uniform/urng randomshift.c
		unuran-1.8.1/src/uniform/urng_randomshift.8 unuran-1.8.1/src/uniform/urng_randomshift.8
		unuran-1.8.1/src/uniform/urng_randomshirt.i
		unuran-1.8.1/src/uniform/urng_rngstreams.h
		unuran-1.8.1/src/unuran.h.in
		unuran-1.8.1/src/urng/Makefile.am
		unuran-1.8.1/src/urng/Makefile.in
		unuran-1.8.1/src/utils/Makefile.am
		unuran-1.8.1/src/utils/Makefile.in
		unuran-1.8.1/tests/Makefile.am
		unuran-1.8.1/tests/Makefile.in
		unuran-1.8.1/tests/README.conf
		unuran-1.8.1/tests/make_test_files.pl
		unuran-1.8.1/tests/t_arou.c
		unuran-1.8.1/tests/t_arou.conf
		unuran-1.8.1/tests/t_ars.c
		unuran-1.8.1/tests/t_ars.conf
		unuran-1.8.1/tests/t_auto.c
		unuran-1.8.1/tests/t_auto.conf
		unuran-1.8.1/tests/t_cext.c
		unuran-1.8.1/tests/t_cext.conf
		unuran-1.8.1/tests/t_cstd.c
		unuran-1.8.1/tests/t_cstd.conf
		<pre>unuran-1.8.1/tests/t_dari.c unuran-1.8.1/tests/t_dari.conf</pre>
		unuran-1.8.1/tests/t_dar1.com1 unuran-1.8.1/tests/t_dau.c
		unuran-1.8.1/tests/t_dau.conf
		unuran-1.8.1/tests/t_dau.com unuran-1.8.1/tests/t_deprecated_tdrgw.c
		unuran-1.8.1/tests/t_deprecated_vmt.c
		unuran-1.8.1/tests/t_deprecated_vmt.conf
		unuran-1.8.1/tests/t dext.c
		unuran-1.8.1/tests/t dext.conf
		unuran-1.8.1/tests/t_dgt.c
		unuran-1.8.1/tests/t dgt.conf
		unuran-1.8.1/tests/t distr.c
		unuran-1.8.1/tests/t distr.conf
		unuran-1.8.1/tests/t distr cemp.c
		unuran-1.8.1/tests/t distr cemp.conf

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Provider	Component	Licensing Information

unuran-1.8.1/tests/t distr condi.conf unuran-1.8.1/tests/t distr cont.c unuran-1.8.1/tests/t distr cont.conf unuran-1.8.1/tests/t_distr_corder.c unuran-1.8.1/tests/t distr corder.conf unuran-1.8.1/tests/t distr cvec.c unuran-1.8.1/tests/t distr cvec.conf unuran-1.8.1/tests/t distr cvemp.c unuran-1.8.1/tests/t distr cvemp.conf unuran-1.8.1/tests/t_distr_cxtrans.c unuran-1.8.1/tests/t_distr_cxtrans.conf unuran-1.8.1/tests/t distr discr.c unuran-1.8.1/tests/t_distr_discr.conf unuran-1.8.1/tests/t_distr_matr.c unuran-1.8.1/tests/t distr matr.conf unuran-1.8.1/tests/t dsrou.c unuran-1.8.1/tests/t dsrou.conf unuran-1.8.1/tests/t dss.c unuran-1.8.1/tests/t dss.conf unuran-1.8.1/tests/t dstd.c unuran-1.8.1/tests/t dstd.conf unuran-1.8.1/tests/t empk.c unuran-1.8.1/tests/t empk.conf unuran-1.8.1/tests/t empl.c unuran-1.8.1/tests/t empl.conf unuran-1.8.1/tests/t gibbs.c unuran-1.8.1/tests/t gibbs.conf unuran-1.8.1/tests/t hinv.c unuran-1.8.1/tests/t hinv.conf unuran-1.8.1/tests/t hist.c unuran-1.8.1/tests/t hist.conf unuran-1.8.1/tests/t hitro.c unuran-1.8.1/tests/t hrb.c unuran-1.8.1/tests/t_hrb.conf unuran-1.8.1/tests/t hrd.c unuran-1.8.1/tests/t hrd.conf unuran-1.8.1/tests/t hri.c unuran-1.8.1/tests/t hri.conf unuran-1.8.1/tests/t info.c unuran-1.8.1/tests/t info.conf unuran-1.8.1/tests/t itdr.c unuran-1.8.1/tests/t itdr.conf unuran-1.8.1/tests/t mcorr.c unuran-1.8.1/tests/t mcorr.conf unuran-1.8.1/tests/t mixt.c unuran-1.8.1/tests/t mvstd.c unuran-1.8.1/tests/t mvstd.conf unuran-1.8.1/tests/t mvtdr.c unuran-1.8.1/tests/t ninv.c unuran-1.8.1/tests/t ninv.conf unuran-1.8.1/tests/t norta.c unuran-1.8.1/tests/t norta.conf unuran-1.8.1/tests/t nrou.c unuran-1.8.1/tests/t nrou.conf unuran-1.8.1/tests/t pinv



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Provider	Component	Licensing Information
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```
unuran-1.8.1/tests/t pinv.c
    unuran-1.8.1/tests/t srou.c
    unuran-1.8.1/tests/t srou.conf
    unuran-1.8.1/tests/t ssr.c
    unuran-1.8.1/tests/t ssr.conf
    unuran-1.8.1/tests/t stringparser.c
    unuran-1.8.1/tests/t stringparser.conf
    unuran-1.8.1/tests/t tabl.c
    unuran-1.8.1/tests/t tabl.conf
    unuran-1.8.1/tests/t tdr.c
    unuran-1.8.1/tests/t_tdr.conf
    unuran-1.8.1/tests/t tdr gw.c
    unuran-1.8.1/tests/t tdr gw.conf
    unuran-1.8.1/tests/t_tdr_ia.c
    unuran-1.8.1/tests/t tdr ia.conf
    unuran-1.8.1/tests/t tdr ps.c
    unuran-1.8.1/tests/t tdr ps.conf
    unuran-1.8.1/tests/t unif.c
    unuran-1.8.1/tests/t unif.conf
    unuran-1.8.1/tests/t_unur_error.c
    unuran-1.8.1/tests/t_unur_error.conf
    unuran-1.8.1/tests/t unur tests.c
    unuran-1.8.1/tests/t unur tests.conf
    unuran-1.8.1/tests/t urng.c
    unuran-1.8.1/tests/t urng.conf
    unuran-1.8.1/tests/t_utdr.c
    unuran-1.8.1/tests/t utdr.conf
    unuran-1.8.1/tests/t util matrix.c
    unuran-1.8.1/tests/t util matrix.conf
    unuran-1.8.1/tests/t vempk.c
    unuran-1.8.1/tests/t vempk.conf
    unuran-1.8.1/tests/t vnrou.c
    unuran-1.8.1/tests/t_vnrou.conf
    unuran-1.8.1/tests/t_x_gen.c
    unuran-1.8.1/tests/t x gen.conf
    unuran-1.8.1/tests/test_StdDistr.c
    unuran-1.8.1/tests/test StdDistr.m
    unuran-1.8.1/tests/test functionparser.c
    unuran-1.8.1/tests/test functionparser.m
    unuran-1.8.1/tests/testcounter.c
    unuran-1.8.1/tests/testdistributions/
Makefile.am
    unuran-1.8.1/tests/testdistributions/
Makefile.in
    unuran-1.8.1/tests/testdistributions/
c sawtooth contpdf.c
   unuran-1.8.1/tests/testdistributions/
c sawtooth discpdf.c
   unuran-1.8.1/tests/testdistributions/
c w pdf from logpdf.c
    unuran-1.8.1/tests/testdistributions/
c with multiple of pdf.c
    unuran-1.8.1/tests/testdistributions/
c wo logpdf.c
    unuran-1.8.1/tests/testdistributions/
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testdistributions.h unuran-1.8.1/tests/testdistributions/ vc_cauchy_RoU_ball.c unuran-1.8.1/tests/testdistributions/ vc_special_correlations_arl.c unuran-1.8.1/tests/testdistributions/	
vc_special_correlations_constantrho.c unuran-1.8.1/tests/testdistributions/ vc_w_marginals.c unuran-1.8.1/tests/testdistributions/ vc_wo_logpdf.c unuran-1.8.1/tests/testroutines.c unuran-1.8.1/tests/testunuran.h unuran-1.8.1/src/distr/deprecated_distr unuran-1.8.1/src/distr/deprecated_distr unuran-1.8.1/src/methods/deprecated_met unuran-1.8.1/src/methods/deprecated_met unuran-1.8.1/src/methods/deprecated_tdr unuran-1.8.1/src/methods/deprecated_vmt unuran-1.8.1/src/methods/deprecated_vmt unuran-1.8.1/src/methods/deprecated_vmt unuran-1.8.1/src/methods/deprecated_vmt unuran-1.8.1/src/parser/ stringparser_lists.ch.in UNU.RAN relies on a modified version of the library Cephes, see ./src/src/specfunct/ cephes_source.h	r.h thods.c thods.h rgw.h t.c t.h



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d) If a facility in the modified Library refers to a function or \boldsymbol{a}

table of data to be supplied by an application program that uses

the facility, other than as an argument passed when the facility

is invoked, then you must make a good faith effort to ensure that, $% \left(1\right) =\left(1\right) +\left(1\right)$

in the event an application does not supply such function or

table, the facility still operates, and performs whatever part of

its purpose remains meaningful.

(For example, a function in a library to compute square roots has

a purpose that is entirely well-defined independent of the $% \left(1\right) =\left(1\right) \left(1\right)$

application. Therefore, Subsection 2d requires that any

application-supplied function or table used by this function must

be optional: if the application does not supply it, the square

 $\begin{tabular}{ll} \begin{tabular}{ll} \beg$

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Section 6 states terms for distribution of such executables.

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Whether this is true is especially significant if the work can be linked without the Library, or if the work is itself a library. The threshold for this to be true is not precisely defined by law.

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Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

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of these things:

a) Accompany the work with the complete corresponding

machine-readable source code for the Library including whatever

changes were used in the work (which must be distributed under $% \left(1\right) =\left(1\right) +\left(1\right) +\left($

Sections 1 and 2 above); and, if the work is an executable linked $\$

with the Library, with the complete machine-readable "work that

uses the Library", as object code and/or source code, so that the $\,$

user can modify the Library and then relink to produce a modified $% \left(1\right) =\left(1\right) \left(1\right) +\left(1\right) \left(1\right) \left(1\right) +\left(1\right) \left(1\right)$

executable containing the modified Library. (It is understood

that the user who changes the contents of definitions files in the $% \left(1\right) =\left(1\right) \left(1\right) +\left(1\right) \left(1\right) \left(1\right) +\left(1\right) \left(1\right) \left(1\right) \left(1\right) +\left(1\right) \left(1$

Library will not necessarily be able to recompile the application

to use the modified definitions.)

b) Use a suitable shared library mechanism for linking with the $\,$

Library. A suitable mechanism is one that

(1) uses at run time a

copy of the library already present on the user's computer system,

rather than copying library functions into the executable, and (2)

will operate properly with a modified version of the library, if $% \left(1\right) =\left(1\right) \left(1\right) +\left(1\right) \left(1\right) \left(1\right) +\left(1\right) \left(1\right) \left(1\right) \left(1\right) +\left(1\right) \left(1\right)$

the user installs one, as long as the modified version is

interface-compatible with the version that the work was made with.

c) Accompany the work with a written offer, valid for at

least three years, to give the same user the materials $% \left(1,...,n\right) =\left(1,...,n\right)$

specified in Subsection 6a, above, for a charge no more

than the cost of performing this distribution.

d) If distribution of the work is made by offering access to copy

from a designated place, offer equivalent access to copy the above $% \left(1\right) =\left(1\right) \left(1\right)$

specified materials from the same place.

e) Verify that the user has already received



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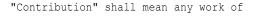
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The :mod:`!_random` C extension underlying the :mod:`random` module includes code based on a download from http://www.math.sci.hiroshima-u.ac.jp/~m-mat/MT/MT2002/emt19937ar.html. The following are the verbatim comments from the original code::

A C-program for MT19937, with initialization improved 2002/1/26.

Coded by Takuji Nishimura and Makoto Matsumoto.

Before using, initialize the state by using
init_genrand(seed)

or init_by_array(init_key, key_length).

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http://www.math.sci.hiroshima-u.ac.jp/~mmat/MT/emt.html

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Sockets

The :mod:`socket` module uses the functions, :c:func:`!getaddrinfo`, and :c:func:`!getnameinfo`, which are coded in separate source files from the WIDE Project, https://www.wide.ad.jp/. ::

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Modified by Jack Jansen, CWI, July 1995:

- Use binascii module to do the actual lineby-line conversion

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- Arguments more compliant with Python standard

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SipHash24

The file: `Python/pyhash.c` contains Marek Majkowski' implementation of Dan Bernstein's SipHash24 algorithm. It contains the following note::

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		strtod and dtoa
		The file: `Python/dtoa.c`, which supplies of functions dtoa and strtod for conversion of C doubles to and from
		strings, is derived from the file of the same name by David M. Gay, currently available
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The implementation of the hash table used by the :mod: `tracemalloc` is based on the cfuhash project::

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The C14N 2.0 test suite in the :mod: `test`



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		Modules: ************************************
		slf4j-api slf4j-simple
		slf4j-nop slf4j-jdk14
		slf4j-log4j12 slf4j-ext
		jcl-over-slf4j log4j-over-slf4j jul-to-slf4j
		osgi-over-slf4j integration

slf4j-site

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slf4j-migrator

4P Dependencies:

ch.qos.cal10n call0n-api
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====

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====

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